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Energy Efficient Flash ADC with PVT Variability Compensation through Advanced Body Biasing

Przemyslaw Mroszczyk, John Goodacre, and Vasilis F. Pavlidis, *IEEE* Member

Abstract—This paper presents the design of an energy efficient Flash analogue-to-digital converter (ADC) with Threshold Inverter Quantiser (TIQ) comparator employing advanced body biasing to compensate for the effects of parameter variability. The proposed calibration scheme is verified against process, voltage, and temperature (PVT) corners as well as random parameter variability (mismatch). Two proof-of-concept ADCs of 4- and 6-bit precision are designed and verified in simulations in 28 nm Fully Depleted Silicon on Insulator (FDSOI) technology. The 6-bit converter achieves sampling rate of 3 GS/s, energy efficiency per conversion step below 20 fJ, and precision of 5.2 effective number of bits (ENOB). The proposed ADC architecture is dedicated to high-speed and low-precision applications, such as communication transceivers and data acquisition systems where area and energy efficiency are paramount.

Index Terms—Flash analog-to-digital converter (ADC), offset calibration, threshold inverter quantiser (TIQ), body biasing.

I. INTRODUCTION

Flash analog to digital converters (ADC) are often considered in systems on chip (SoC) applied to high-speed communication interfaces, front-end readout circuits, and data acquisition systems [1], [2]. Due to the highly parallel architecture of a Flash ADC, the analogue input signal is instantaneously compared against all the quantization levels, thus the conversion speed is limited only by the slowest comparator in the array. As the circuit size (and, hence, the input capacitance and power consumption) grows exponentially with the bit-wise precision of the converter, the precision is typically limited to 4 – 6 bits [3].

One of the main challenges in Flash ADC circuits is to ensure correct operation under variability of process and environmental conditions. In particular, random process variability (mismatch) generates random offsets in the comparators degrading the linearity of a converter. The basic technique addressing mismatch, applicable to any CMOS circuit, employs device scaling [4]. This technique, however, is expensive in terms of silicon area and energy consumption. Several dedicated circuit design techniques have also been proposed, such as offset averaging (applicable only to comparators with pre-amplifier stage) [5], auto-zeroing (applicable only to clocked comparators with interleaved reset/calibration and evaluation cycles) [6], and redundancy [7].

Another approach to mitigate parameter variability is based on digitally controlled trimming. In this approach, a set of additional devices (transistors or capacitors) is collectively connected to the

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critical nodes of a comparator through digitally controlled switches [1], [8]. Alternatively, a digitally controlled bias can be used to achieve similar effect without using redundant devices employing circuit degeneration [9], [10] or body biasing [11].

A CMOS inverter as a high-speed comparator is known in the literature as the Threshold Inverting Quantiser (TIQ) [12], Threshold Modified Comparator Circuit (TMCC) [13], and Bias Inverter Quantiser [9], and its applications have been explored for several decades [6], [8]. The schematic diagram of a TIQ circuit, example transfer characteristic, and basic formulas describing the circuit operation assuming the standard square-law MOS transistor model are shown in Fig. 1a [12]. This circuit comprises a single CMOS inverter where the analogue input signal is compared with the inherent gate threshold V_{GTH} , depending on the parameters of the MOS transistors and the supply voltage V_{DD} .

TIQ-based comparators eliminate the need for external voltage references, operate well under very low supply voltage and exhibit excellent energy efficiency which is particularly attractive when several tens of comparators are needed in a Flash ADC. The main challenges, however, are the need for individual sizing (pre-programming) of the comparators, high sensitivity of the V_{GTH} to process corners, mismatch, and supply voltage variation. Several methods for V_{GTH} tuning other than the geometry scaling have been proposed employing circuit degeneration with resistors [10] or with transistors [9], as presented in Figs. 1b and c respectively, or using digitally controlled small-size switches, as shown in Fig. 1d [8].

In this paper, a fully autonomous trimming technique is proposed for the TIQ-based comparator through body biasing in Fully Depleted Silicon-on-Insulator (FDSOI) CMOS technology [14]. The proposed technique allows tuning V_{GTH} with a single bias voltage, eliminating the need for circuit degeneration (*thus, maximizing comparator speed*), the use of switches (*thus, minimizing the input capacitance*), and the use of bias voltages within the core supply range (*thus,*

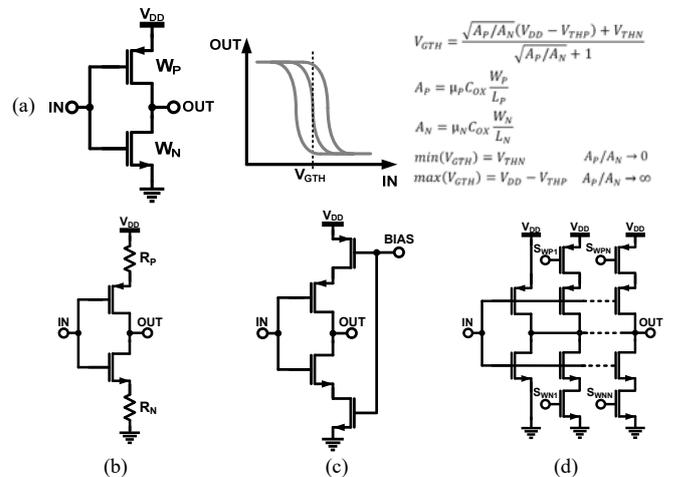


Fig. 1. Threshold Inverting Quantiser (TIQ): a) basic circuit [12], and V_{GTH} tuning techniques employing, respectively, b) resistors [10], c) transistors [9], and d) switches [8].

simplifying the design).

The proposed body biasing scheme realized in FDSOI technology is presented in Section II. The architecture of the Flash ADC with TIQ comparators and trimming circuitry is presented in Section III. The results and discussion are provided in Section IV and Section V concludes the paper.

II. BODY BIASING IN FDSOI TECHNOLOGY

From the circuit design perspective, the major benefit of the FDSOI technology is a wider range of body bias voltage and a higher body factor (i.e. the sensitivity of the threshold voltage to body bias voltage) reaching ~ 85 mV/V compared to only ~ 25 mV/V in a bulk technology [14]. This is because in the FDSOI technology the source, drain, and channel of a transistor are isolated from the substrate by the thick layer of buried oxide (BOX). As a result there are no diodes between the source/drain and the substrate, typical to bulk technologies, requiring reverse biasing thus limiting body bias range.

The FDSOI technology used in this work provides MOS transistors with regular (RVT) and low (LVT) threshold voltages in the Conventional Well (CW) and the Flip Well (FW) structures, respectively, as shown in Fig. 2 [14]. It can be observed, however, that in both configurations there is a parasitic n-well diode limiting the range of the body bias voltage. Using only the transistors in the isolated n-wells as complementary devices in inverter design, eliminates the parasitic n-well diodes, enabling interesting opportunities for body biasing.

Consequently, the idea proposed in this paper is to build the TIQ circuit using the p-MOS transistor from the CW structure with the n-MOS device from the FW structure (gray shade devices in Fig. 2). This approach allows treating these transistors as dual gate devices, where the second (buried) gate provides limited ability to control the channel. Nevertheless, this controllability is sufficient to shift the threshold voltage within the range needed for mismatch compensation.

The schematic of the proposed TIQ circuit is shown in Fig. 3a and example simulation results of trimming are presented in Fig. 4. Note that for increasing V_{BB} , the threshold of the n-MOS transistor

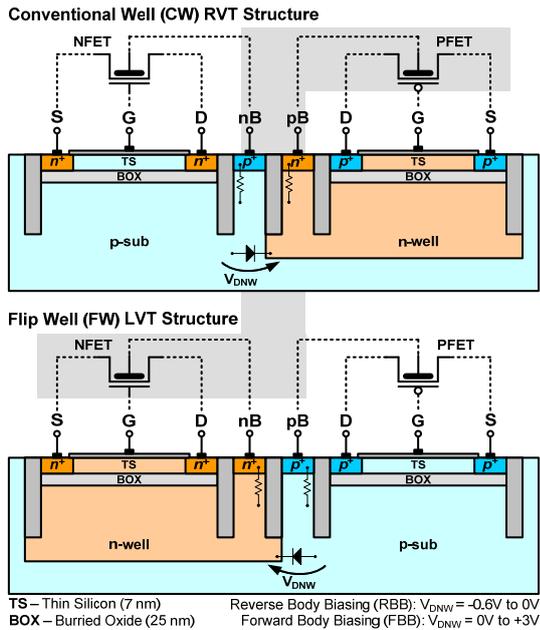


Fig. 2. Conventional and Flip Well configurations for RVT and LVT devices offered in FDSOI technology [18].

decreases while the threshold of the p-MOS transistor increases. This allows tuning of the V_{GTH} in a twice wider range than in any equivalent circuit in only CW or FW configuration. If, however, an even wider tuning range is required (e.g. to compensate for the V_{GTH} variability in different process corners), the circuit from Fig. 1d can be further adapted. The switches and the additional transistors are used for coarse adjustment of the switching threshold while body biasing is employed to fine tune V_{GTH} , as demonstrated in Fig. 3b.

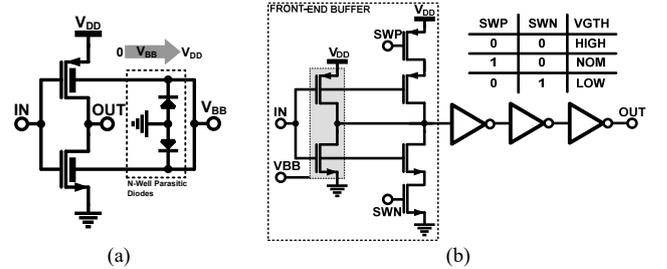


Fig. 3. a) The proposed TIQ circuit in Mixed-Well structure and b) TIQ comparator with coarse and fine tuning of V_{GTH} .

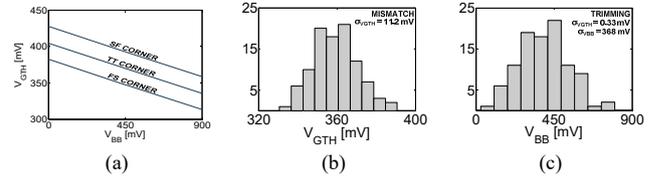


Fig. 4. Simulation results: a) V_{GTH} vs. V_{BB} , b) V_{GTH} variability resulting from parameter mismatch, c) V_{BB} variability after V_{GTH} trimming.

III. ARCHITECTURE AND TRIMMING

The top level diagram of the proposed Flash ADC is shown in Fig. 5. The architecture is scalable with the number of bits N determining the precision and the number of trimming steps K . There are two voltage reference circuits with resistor strings: ADC REF, generating $2^N - 1$ quantization levels for the analog-to-digital conversion within the full scale range $V_{FS} = V_{REF+} - V_{REF-}$, and BB REF, generating K steps from 0 to V_{DD} for the body biasing. There are two clocks: SYS CLK, used for trimming, and ADC CLK, used during normal operation and determining the sampling rate of the ADC. The calibration process is supervised by the TRIMMING CONTROLLER and performed during the system startup. During normal operation, in every ADC CLK cycle, a new sample is captured by the sample-and-hold module (S/H), discretized by the TIQ comparators, and converted to natural binary code by the ENCODER block.

The block diagram of the TIQ core module is illustrated in Fig. 6, including the TIQ comparator, two analog multiplexers, and a register with I/O module. The configuration bit ADC/TRIM selects the input for the TIQ comparator either from the S/H or from the ADC REF (during calibration only). The threshold V_{GTH} is fine-tuned by the body bias voltage V_{BB} selected from the BB REF set by the $K:1$ multiplexer with K analogue switches with one-hot addressing. The coarse tuning of the V_{GTH} (compensating for the asymmetric process corners FS and SF) is done by selecting the two auxiliary switches in the comparator. All the configuration bits and words are bundled into the CONFIG BUS used by the controller to activate a particular core for trimming, provide the required configuration bits and words, and monitor the TIQ output.

An example sequence demonstrating the trimming process of one TIQ comparator is depicted in Fig. 7. The input of the comparator is connected to the corresponding reference ADC REF. There are three sub-ranges for coarse tuning with low (L), nominal (N), and high (H) V_{GTH} . For each of these sub-ranges, a full sweep of V_{BB} is performed to fine tune V_{GTH} . Trimming starts with the H subrange (i.e. p-MOS switch is on in the comparator, see Fig. 3b). As V_{BB} increases, V_{GTH} decreases until the applied reference V_{REF} is crossed. Then the output of the comparator turns to the high state and the trimming terminates. If, however, TIQ OUT remains low, fine tuning is repeated for the next sub-range N (i.e. no switches are activated in the comparator). If TIQ OUT still remains low, fine tuning is repeated again for the last sub-range L. Note that for the calibration to be successful (i.e. TIQ OUT sets to '1'), the tuning range should cover the worst case process and mismatch variability range of the V_{GTH} . To ensure this requirement, additional switches for coarse tuning were added to the comparator circuit and scaled accordingly (see Fig. 3b).

IV. DESIGN CONSIDERATIONS AND SIMULATION RESULTS

In the following, several practical considerations related to the application of the TIQ comparator in ADC design are discussed. The full scale range V_{FS} is determined by the difference of the maximum and minimum V_{GTH} achieved through transistor scaling, as presented in Fig. 8. The threshold V_{GTH} is determined by the ratio of the transistor widths W_N/W_P and can be varied within the range denoted by the supply and the respective threshold voltages (see Fig. 1a). In order to increase V_{FS} , the end-most comparators require transistors with significantly different widths. A practical limitation in achieving large V_{FS} is the minimum technology feature size enforcing larger gate widths of the complementary device in the buffer leading in turn

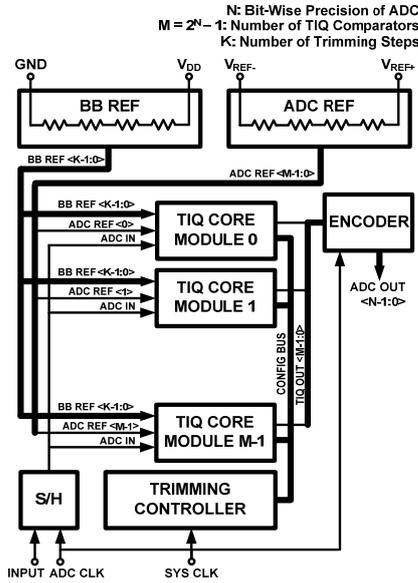


Fig. 5. Block diagram of the proposed Flash ADC.

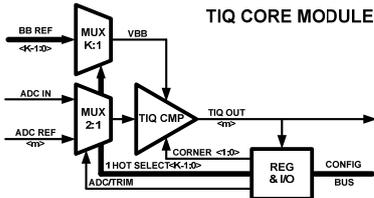


Fig. 6. Block diagram of the architecture of the proposed Flash ADC.

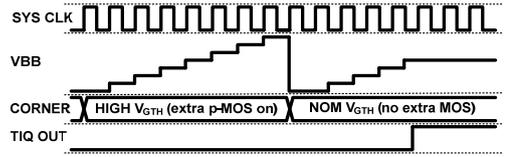


Fig. 7. Block diagram of the architecture of the proposed Flash ADC.

to larger input capacitance and effectively slower propagation delay of the comparators.

Example simulation results showing the worst case delay in the end-most comparators in terms of V_{FS} evaluated for 4-, 6-, and 8-bit Flash ADC configuration are shown in Fig. 9. Here we assume that the V_{FS} increases as a result of modifying the widths of the transistors starting from the nominal buffer size with equally sized devices, as presented in Fig. 8. The worst case delay is measured as the longest response time of the end-most comparators resolving the voltage difference equal to V_{LSB} while recovering from saturation. Since $V_{LSB} = V_{FS}/(2^N - 1)$, it decreases with N for a given V_{FS} , systematically, increasing the delay. The increase in the delay observed for larger V_{FS} , stems from the parasitic drain/source capacitance of the large devices driven by the complementary (small) device. For the smaller V_{FS} , the corresponding V_{LSB} reduces, hence the comparators require more time to resolve the input difference. The worst case delay is minimum for V_{FS} in the range of 100 mV – 200 mV for the chosen technology, supply, and transistor scaling scheme.

During normal operation when the input voltage stays within the conversion range of the ADC, the TIQ comparators continuously draw current from the supply. Note that this current is maximum for the input voltage equal to V_{GTH} of a respective comparator. In the Flash ADC, this current contributes to the energy loss and, due to its dependency on the input signal, it also degrades signal integrity through harmful (signal dependent) modulation of the supply voltage. Although this current cannot be eliminated, it can be reduced by

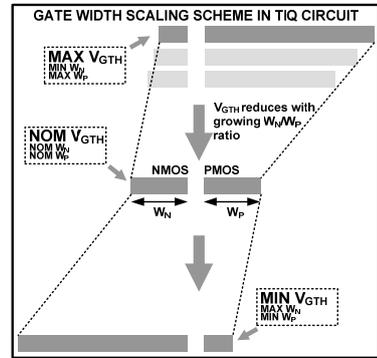


Fig. 8. TIQ front-end MOS transistor gate scaling scheme.

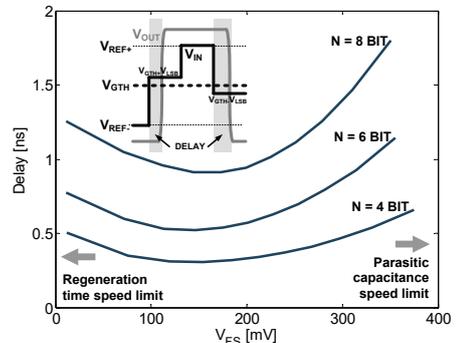


Fig. 9. Worst case delay vs. full scale range of the TIQ comparator in 4-, 6-, and 8-bit Flash ADC configuration.

geometry scaling and appropriate design of the power supply network. To address this issue, in the proposed scaling approach shown in Fig. 8, the geometry of the mid-range comparator is reduced such that the delay of this comparator is comparable with the worst case delay of the end-most comparators (see Fig. 9). Note that this delay matching approach allows minimizing the static power of the comparator array without compromising speed.

The average energy per comparator per conversion step in terms of the full scale range V_{FS} is plotted in Fig. 10. Note that the energy per conversion step gradually decreases with larger V_{FS} . As a result, the corresponding input voltage equal to $V_{GTH} \pm V_{LSB}$ remains further away from V_{GTH} (as V_{LSB} grows with V_{FS}) and the front-end buffer draws less current in between the signal transitions (refer to Fig. 9). Also the corresponding energy traces exhibit a systematic shift with N as V_{LSB} decreases with N , leading to higher steady state currents of the comparators. Note that the estimation of the energy of an N -bit ADC based on the simulated average energy of a TIQ comparator would rather be pessimistic since all the comparators in the array share a common input voltage, thus only one comparator can draw the maximum current.

The standard deviation of the V_{GTH} resulting from the random parameter variability (mismatch) with respect to the size of the V_{LSB} interval, after circuit calibration, is depicted in Fig. 11. In this analysis, the comparator with a nominal front-end buffer size and $K = 32$ trimming steps in the calibration process is used. Assuming without loss of generality that an ADC operates correctly if $\pm V_{LSB}/2 \geq \pm \beta \sigma_{VGTH}$, leading to $V_{LSB} \geq 2\beta \sigma_{VGTH}$. For example, $\beta = 3$ corresponds to the “three sigma” rule stating that over 99.7% of the comparators in the array will have the switching threshold not farther than $\pm V_{LSB}/2$ away from V_{GTH} (set as reference). Using the diagram in Fig. 11, a 4-bit ADC satisfies the “three sigma” rule for $V_{FS} > 60$ mV while a 6-bit ADC requires V_{FS} at least 250 mV. Note that increasing V_{FS} , requires larger devices and results in longer delays

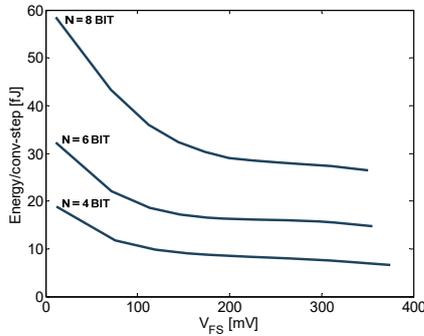


Fig. 10. Average energy per conversion step per TIQ comparator vs full scale range in 4-, 6-, and 8-bit Flash ADC configuration.

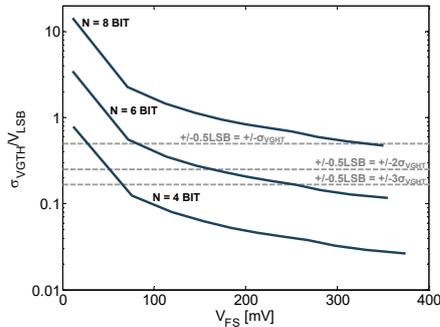


Fig. 11. The variability of the V_{GTH} with respect to V_{LSB} vs. full scale range in 4-, 6-, and 8-bit Flash ADC configuration.

reducing the conversion speed.

The results demonstrating the effectiveness of V_{GTH} trimming against process, voltage, and temperature (PVT) corners are shown in Figs. 12 and 13. In Fig. 12, the statistical parameters of V_{GTH} after compensation in terms of number of the trimming steps K , are illustrated assuming combined process and mismatch variability. Note that the effectiveness of trimming grows with K reaching $\sigma_{VGTH} \approx 300 \mu\text{V}$ for $K = 64$ which already approaches the input referred noise level [8]. The V_{GTH} after trimming for a constant reference and variable supply voltage V_{DD} is shown in Fig. 13a. The proposed calibration scheme can compensate for up to $\pm 10\%$ V_{DD} variability in the top-most comparator (where the absolute variability of V_{GTH} is the highest due to the resistor divider effect). The variability of V_{GTH} measured after trimming performed in different temperatures from -40 to 125°C is shown in Fig. 13b. Overall, trimming allows compensating for the variability of V_{GTH} due to supply voltage and temperature fluctuations keeping it within ± 1.5 mV around the desired reference, equivalent to $\pm 1/3$ LSB in a 6-bit ADC.

Two proof-of-concept Flash ADCs with 4- and 6-bit precision implementing the guidelines for energy efficient design are realized in the 28 nm FDSOI technology and characterized for performance. In the simulations, layout extracted models of the comparator and encoder circuits determine the speed and power. For the digital blocks, supervising the circuit calibration process, high level behavioral models in Verilog A are developed and used to reduce simulation time. Note that these blocks become inactive during normal operation providing only static configuration signals. The encoder employed in the ADC circuit is based on Wallace Tree architecture with full adders. Energy efficient encoder design is beyond the scope of this paper and related circuits can be found in [15]. In order to ensure maximum sampling rate, 3-stage pipelining is introduced at the S/H circuit and input and output registers in the encoder.

The static parameters such as integral and differential nonlinearity assuming only fabrication mismatch before and after calibration are shown in Fig. 14. Note that the 6-bit ADC is practically inoperable without calibration due to missing codes. The effective number of bits (ENOB) for different input signal frequencies up to Nyquist is illustrated in Fig. 15 [16]. Note that the accuracy of the 6-bit ADC

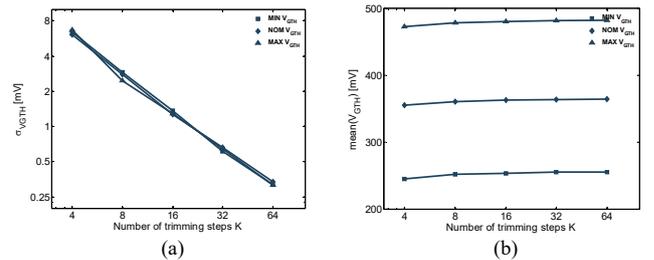


Fig. 12. Combined process and mismatch variability of V_{GTH} in terms of the number of trimming steps K : a) standard deviation and b) mean value.

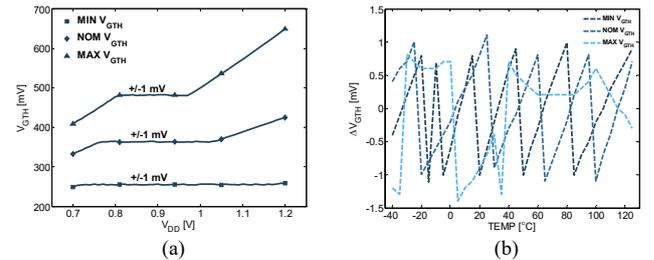


Fig. 13. The variability of V_{GTH} after trimming in terms of a) V_{DD} supply voltage, and b) temperature.

degrades quicker with the sampling rate mainly due to the longer delay of the comparators (see Fig. 9) and harmful supply voltage modulation through resistive power rails. Parameters of the ADC are summarized in Table I. A comparison to other designs based on energy efficiency employing Walden's figure of merit [17] is shown in Fig. 16. The simulation based performance of the Flash ADCs (with Wallace Tree encoders) is very promising with potential to push the performance envelope with more energy efficient encoder designs [15].

V. CONCLUSIONS

This paper presents a method to energy efficient Flash ADC design with TIQ comparators. The proposed calibration technique is fully autonomous and uses advanced body biasing in FDSOI technology to reduce the impact of PVT variability on the circuit operation without compromising performance. The proposed scheme is verified through the simulation of two proof-of-concept ADC designs achieving below 20 fJ per conversion step efficiency at 6-bit precision, thus finding applications in low-power transceivers and data acquisition systems.

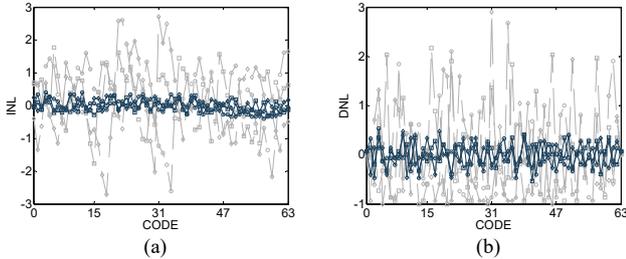


Fig. 14. a) Integral (INL) and b) differential (DNL) nonlinearity before (grey) and after trimming in the 6-bit Flash ADC.

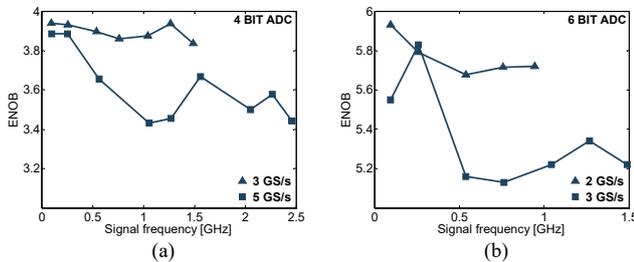


Fig. 15. Effective number of bits (ENOB) vs. input signal frequency at slow and fast sampling rate for a) 4- and b) 6-bit ADC.

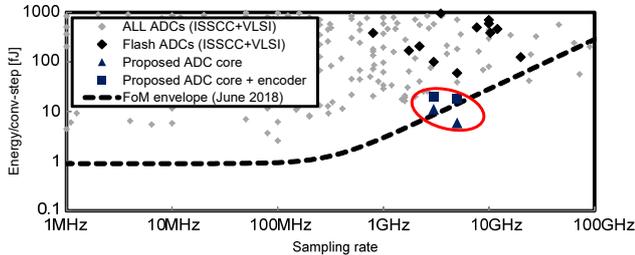


Fig. 16. Energy efficiency of the proposed solutions (simulations) compared to other designs based on Walden's Figure of Merit [17].

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TABLE I
PARAMETERS OF THE PROPOSED FLASH ADCS

	4-bit ADC	6-bit ADC
Technology	28 nm CMOS FDSOI	
Nominal supply	900 mV	
Input range	245 - 515 [mV]	250 – 500 [mV]
Input capacitance	0.12 [pF]	0.5 [pF]
Full scale range (V_{FS})	270 mV	250 mV
V_{LSB}	18 mV	4 mV
INL	± 0.8 LSB ¹	± 2.7 LSB ¹
	± 0.07 LSB ²	± 0.4 LSB ²
DNL	$+1.1/-0.9$ LSB ¹	$+2.9/-1$ LSB ¹
	± 0.12 LSB ²	± 0.5 LSB ²
Power (core/encoder/bias)	320/630/10 [μ W]	1230/990/10 [μ W]
Sampling rate	5 GS/s	3 GS/s
ENOB	3.4	5.2
SNDR	22.5 dB	33.1 dB
SFDR	30.5 dB	39.3 dB
FoM ³	6/12/0.2	11/9/0.1
(core/encoder/bias)	[fJ/conv-step]	[fJ/conv-step]

¹ Before trimming

² After trimming

³ Walden's FoM rated at the given sampling rate

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