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Complementary Integrated Circuits based on N- and P-Type Oxide Semiconductors for Applications beyond Flat-Panel Displays

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Abstract—Oxide semiconductors are highly attractive for fabrication of large-area thin-film electronics because of their high electrical performance, low process temperature, high uniformity, and ease of industrial manufacturing. N-type oxide semiconductors, such as InGaZnO, are highly developed and have already been commercialized for backplane drivers of flat-panel displays. To date, developing complementary metal-oxide-semiconductor (CMOS) technology is still an urgent issue in order to build low-power electronic circuits based on oxide semiconductors. In this work, various CMOS circuits, including inverters, NAND, NOR, XOR, d latches, full adders, and 7-, 11-, 21-, and 51-stage ring oscillators, are fabricated based on sputtered p-type tin monoxide (SnO) and n-type InGaZnO. The inverters show rail-to-rail output voltage behavior, low average static power consumption of 8.84 nW, high noise margin level up to ~40% supply voltage, and high uniformity with negligible standard deviation. The NAND, NOR, XOR, d latches, and full adders show desirably ideal input-output characteristics. The performances of ring oscillators indicate small stage delay of ~1 μ s, extremely high uniformity and high yield which are essential for large-area thin-film electronics. This work may inspire constructions of low-power, large-area, large-scale, and high-performance transparent/flexible CMOS circuits fully based on oxide semiconductors for applications beyond flat-panel displays.

Index Terms—Oxide semiconductor, thin-film transistor (TFT), CMOS, integrated circuit (IC)

I. INTRODUCTION

Complementary metal-oxide-semiconductor (CMOS) technology is widely applied to integrated circuits (ICs) because of its lower static power consumption, higher logic-swing output, and higher noise margin compared with its unipolar n-type MOS or p-type MOS counterparts. Oxide semiconductors have been widely studied in the past few years [1]–[5]. Their unique advantages, including low cost, low fabrication temperatures, scalable deposition methods, higher

carrier mobilities than amorphous-Si and most organics, and excellent transparency in visible region, are ideal for various flexible and transparent electronics applications [1]–[3], [5]–[8].

For oxide semiconductors, an urgent issue for low-power electronic circuits is to develop CMOS technology. IGZO TFTs have already been commercialized for backplane drivers of flat-panel displays [1], [2], [8]. Many circuits based on IGZO TFTs have also been studied [1]–[3], [8]–[12]. In the last few years, p-type organics and carbon nanotubes have been hybridized with IGZO to create low-power CMOS inverters and ICs [13]–[15]. However, the incompatible preparation technologies of organic semiconductors, carbon nanotubes, and oxide semiconductors result in rather complex fabrication process for ICs. On the other hand, CMOS ICs based on high-performance n- and p-type oxides would not suffer from such problems.

Extraordinary efforts have been made for developing p-type oxide materials and TFTs which are comparable to their n-type counterparts in performance [6], [7], [16]–[20]. To date, ternary Cu-bearing oxides, binary copper oxides, tin monoxide (SnO), spinel-type oxides, NiO, etc. have been known as p-type oxides [6]. Among these p-type oxides, SnO is one of the most promising because of its native p-type conductivity and high hole mobility [7], [21]–[23]. CMOS inverters based on n-type oxides such as In₂O₃ [24], SnO₂ [25], [26], IGZO [27]–[31], and ZnO [32], [33], and p-type SnO have been reported. However, systematic study on CMOS circuits based on oxide semiconductors is still limited to date.

In this work, we present the realization of various CMOS circuits based on n-type IGZO and p-type SnO. Both IGZO and SnO were deposited at room temperature using the radio-frequency magnetron sputtering method, which is highly industrial compatible for large-area film deposition. The highest process temperature is 225 °C, making it possible to fabricate the CMOS ICs on flexible substrates such as

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polyimide. The performances of the fabricated TFTs, inverters, NAND, NOR, XOR, d latches, full adders, and ring oscillators are systematically analyzed.

Fig. 1. Transfer characteristics of (a) an IGZO TFT and (b) a SnO TFT. Output characteristics of (c) the IGZO TFT and (d) the SnO TFT.

II. OXIDE-BASED TFTS AND CMOS INVERTERS

A. Oxide-Based TFTs

Figs. 1(a) and 1(b) show the transfer characteristics of an IGZO TFT and a SnO TFT, respectively. The field-effect mobilities (μ), threshold voltages (V_{th}), subthreshold swings (SS), and on/off ratios for the IGZO TFT are 10.22 and 10.23 $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$, 4.47 and 3.51 V, 0.66 and 0.66 Vdec^{-1} , and 7.48×10^6 and 3.00×10^7 with drain voltages (V_D) of 1 and 10 V, respectively. The μ , V_{th} , SS , and on/off ratios for the SnO TFT are 0.87 and 0.87 $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$, -3.39 and -1.54 V, 1.45 and 1.55 Vdec^{-1} , and 3.55×10^4 and 1.88×10^4 with V_D of -1 and -10 V, respectively. Figs. 1(c) and 1(d) show the output characteristics of the IGZO and SnO TFTs, respectively, both indicating ideal saturation characteristics and ohmic contacts between the source/drain electrodes and channel layers.

Fig. 2. (a) Three-dimensional schematic diagram of the IGZO/SnO CMOS inverter. (b) Output voltages (V_{out}) and (c) gains of the CMOS inverter as functions of input voltages (V_{in})

with supply voltages (V_{DD}) of 4 , 6 , 8 , and 10 V. (d) Crossing currents (I_{DD}) of the CMOS inverter with V_{DD} of 4 , 6 , 8 , and 10 V.

B. Oxide-Based CMOS Inverters

Fig. 2(a) shows the three-dimensional schematic diagram of the IGZO/SnO CMOS inverter. The geometric aspect ratio is 6 . Fig. 2(b) demonstrates the voltage transfer curves (VTCs) of the CMOS inverter with supply voltages (V_{DD}) of 4 , 6 , 8 , and 10 V. The VTCs show sharp switching with rail-to-rail output voltage (V_{out}) behavior. The transition voltages (V_{tr}) of the inverter where input voltage (V_{in}) equals V_{out} are ideally close to $V_{DD}/2$ due to the balanced performance of IGZO and SnO TFTs (Fig. 1). The voltage gains of the CMOS inverter are 42.69 , 92.77 , 115.60 , and 131.57 with the V_{DD} of 4 , 6 , 8 , and 10 V, respectively (Fig. 2(c)). Fig. 2(d) shows the crossing currents (I_{DD}) of the CMOS inverter as functions of V_{in} and V_{DD} . The I_{DD} when $V_{in} = 0$ V is around 40 pA. The I_{DD} when $V_{in} = V_{DD}$ is around 4.38 nA. Thus, the average static power consumption is as low as 8.84 nW when $V_{DD} = 4$ V. The gate leakage current flowing through the dielectric is another key issue for making low-power ICs and was also measured as shown in Fig. 2(d). It is lower than 40 pA, which, actually, is close to the detection limit of our probe station, indicating negligible leakage current. The low static current and negligible leakage current guarantee the capability of IGZO/SnO CMOS inverter for compact and large-scale ICs.

Fig. 3 demonstrates statistics of the voltage gains, V_{tr} , and noise margins (NM) of the tested seven CMOS inverters. The NM depends on the lower value between noise margin high (NM_H) and noise margin low (NM_L). The average voltage gains with standard deviation are 42.61 ± 2.20 , 87.19 ± 7.30 , 105.99 ± 10.15 , and 117.46 ± 11.27 with V_{DD} of 4 , 6 , 8 , and 10 V, respectively. The average V_{tr} values with standard deviation are 2.32 ± 0.07 , 3.08 ± 0.03 , 3.80 ± 0.02 , and 4.45 ± 0.03 with V_{DD} of 4 , 6 , 8 , and 10 V, respectively. The average values of NM with standard deviation are 1.37 ± 0.07 , 2.52 ± 0.02 , 3.26 ± 0.02 , and 3.76 ± 0.02 V with V_{DD} of 4 , 6 , 8 , and 10 V, respectively. The low standard deviations of voltage gains ($< 10\%$), V_{tr} ($< 3\%$), and NM ($< 5\%$) indicate very high uniformity of the inverter performances. It is worthy to note that the inverters show very large NM ($\sim 40\%$ V_{DD}) as a result of the ideal V_{tr} close to $V_{DD}/2$ and high gains. Such a large NM is essential for the reliable performances of ICs based on these inverters.

Fig. 3. Statistics of (a) voltage gains, (b) transition voltages (V_{tr}), and (c) noise margins (NM) of the CMOS inverters with V_{DD} of 4 , 6 , 8 , and 10 V.

III. OXIDE-BASED CMOS BASIC LOGIC GATES

Logic gates are basic building blocks for ICs. Figs. 4(a), 4(b), and 4(c) show the circuit symbols, photographs, and schematic circuit diagrams of the NAND, NOR, and XOR gates, respectively. The layouts of these logic gates were thoughtfully designed considering the convenience of further integration of more sophisticated circuits. Input signals were applied on the electrode A and the electrode B for the NAND, NOR, and XOR gates. The high level of the input signal treated as logic “1” equals V_{DD} . The low level of the input signal treated as logic “0” equals 0 V. The truth tables of the NAND, NOR, and XOR gates are included in Fig. 4(d). For the NAND gate, the output is “0” only when both of the input signals are set to “1”, while for the NOR gate, the output is “1” only when both of the input signals are set to “0.” For the XOR gate, the output signal is “0” when the input signals are the same, and the output signal is “1” when the input signals are different. The black, red, blue, and green lines demonstrate the input-output characteristics of the logic gates with the V_{DD} of 4, 6, 8, and 10 V, respectively. All of the fabricated logic gates exhibit correct logic functions with rail-to-rail outputs, owing to the robust CMOS mode as shown in Fig. 3.

Fig. 4. Circuit symbol (top), photograph (middle), and schematic circuit diagram (bottom) of the (a) NAND, (b) NOR, and (c) XOR gate. (d) Input-output characteristics of the NAND, NOR, and XOR gates with V_{DD} of 4, 6, 8, and 10 V.

IV. OXIDE-BASED CMOS D LATCH AND FULL ADDER

Digital logic circuit can be divided into combinational logic circuit and sequential logic circuit. Outputs of the combinational logic circuit are the functions of only the present input signals, while outputs of the sequential logic circuit depend not only on the present inputs but also the historic inputs. To construct digital ICs, both the combinational logic circuits and sequential logic circuits are required. The d latch is one of the most widely used sequential logic circuits and plays an essential role for data storage in ICs [34]. The adder is a typical combinational logic circuit and one of the most important arithmetic circuits, which is essential for various digital logic ICs such as the central processing unit (CPU). However, the successful fabrication of sophisticated circuits such as the d latch and full adder requires inverters with high uniformity, high yield, and large NM . To date, sophisticated CMOS ICs fully based on oxide semiconductors have not been reported yet. Here, the CMOS d latch and one-bit full adder based on p-type

SnO and n-type IGZO were designed and fabricated successfully for the first time.

A. Oxide-Based CMOS D Latch

The d latch is constructed using four NAND gates and an inverter, containing 18 TFTs, as shown in Figs. 5(a) and 5(b). As described in the truth table shown in Fig. 5(c), the output signal Q equals the input signal D when the clock signal CLK is “1,” while the output signal Q maintains its previous state (the logic value just before the falling edge of CLK) when the CLK is “0.” The Q of the fabricated d latch shows correct and rail-to-rail output voltage with V_{DD} of 4, 6, 8, and 10 V (Fig. 5(d)).

Fig. 5. (a) Layout, (b) circuit diagram, (c) truth table, and (d) input-output characteristics of the d latch. (e) Circuit diagram, (f) layout, and (g,h) input-output characteristics of the one-bit full adder.

B. Oxide-Based CMOS Full Adder

The one-bit full adder is composed of three NAND and two XOR gates, containing 36 TFTs, as shown in Fig. 5(e). Fig. 5(f) shows the layout of the one-bit full adder. The layout area of the fabricated full adder is as small as $700 \mu\text{m} \times 500 \mu\text{m}$ although the interconnect width is relatively large ($10 \sim 20 \mu\text{m}$). Such a small area is comparable to that of carbon nanotube (CNT)-based CMOS full adder fabricated using electron beam lithography and much smaller than printed CNT- or organic-based full adder [35]-[37]. The S_i , A_i , B_i , C_{i-1} , and C_i are the binary signal of sum, addend, augend, carry from previous addition, and carry for next addition, respectively. The input signals A_i and B_i were applied using a signal generator, while the input signal C_{i-1} was applied using source/measure unit, because our signal generator has only two outputs. “ $C_{i-1} = 1$ ” means that the applied voltage of the C_{i-1} equals V_{DD} , and “ $C_{i-1} = 0$ ” means that the applied voltage of the C_{i-1} is set to 0 V. Figs. 5(g) and 5(h) show the input-output characteristics of the full adder with C_{i-1} equals “1” and “0”, respectively. The black, red, blue, and green lines indicate the input-output characteristics of the full adder with the V_{DD} of 4, 6, 8, 10 V, respectively.

The desirably ideal input-output characteristics of the d latch and full adder indicate that our oxide semiconductors have the

capability to construct complicated CMOS ICs for various applications in flexible and transparent electronics.

V. OXIDE-BASED CMOS RING OSCILLATORS

7-, 11-, 21-, and 51-stage ring oscillators (ROs) based on IGZO/SnO CMOS configuration were fabricated to systematically evaluate the speed, uniformity, and yield of our CMOS circuits. Fig. 6(a) shows the schematic circuit diagram of RO, where an odd number of CMOS inverters are connected in series with an additional inverter as an output buffer. Fig. 6(b) shows layouts of 7-, 11-, 21-, and 51-stage ROs.

Fig. 6. (a) Schematic circuit diagram and (b) photographs of the 7-, 11-, 21-, and 51-stage ring oscillators. (c) Output characteristics of the 7-stage ring oscillator with V_{DD} of 1 and 2 V. (d) Output characteristics of the 7-stage ring oscillator with V_{DD} of 4, 6, 8, and 10 V. (e) Statistics of the oscillation frequencies and the corresponding stage delays of five 7-stage ring oscillators as functions of V_{DD} . (f) Output characteristics of the 51-stage ring oscillator with V_{DD} of 1 and 2 V. (g) Output characteristics of the 51-stage ring oscillator with V_{DD} of 4, 6, 8, and 10 V. (h) Statistics of the oscillation frequencies and the corresponding stage delays of five 51-stage ring oscillators as functions of V_{DD} . (i) Oscillation periods as functions of stage number with V_{DD} of 1 and 2 V. (j) Oscillation periods as functions of stage number with V_{DD} of 4, 6, 8, and 10 V. (k) Peak-to-peak voltages as functions of stage number with V_{DD} of 1, 2, 4, 6, 8, and 10 V.

A. Speed of Oxide-Based CMOS Circuits

The speed of the ROs were measured with different V_{DD} . The ROs started to oscillate with 1 V V_{DD} . The outputs of the 7-stage RO with V_{DD} of 1 and 2 V are shown in Fig. 6(c), and the outputs of the 7-stage RO with V_{DD} of 4, 6, 8, and 10 V are shown in Fig. 6(d). The delay time of each inverter, τ , can be calculated using:

$$\tau = 1/(2 \cdot n \cdot f), \quad (1)$$

where n and f are the stage number and the oscillation frequency of the RO, respectively. The statistics of oscillation frequencies and corresponding stage delays of five 7-stage ROs are shown in Fig. 6(e) as functions of V_{DD} . The average τ values with standard deviation are 93.29 ± 15.31 , 24.70 ± 1.51 , 6.12 ± 0.18 , 2.90 ± 0.04 , 1.73 ± 0.02 , and 1.20 ± 0.02 μ s with V_{DD} of 1, 2, 4, 6, 8, and 10 V, respectively. The outputs of the 51-stage RO with V_{DD} of 1 and 2 V are shown in Fig. 6(f), and the outputs of the 51-stage RO with V_{DD} of 4, 6, 8, and 10 V are shown in Fig. 6(g) (Data of 11- and 21-stage ROs are not shown here.). The 51-stage RO is the first reported all-oxide-based ROs with rail-to-rail oscillation waveforms [27], [30], [32], [33]. The statistics of oscillation frequencies and corresponding stage delays of five 51-stage ROs are shown in Fig. 6(h). The average τ values with standard deviation are 71.81 ± 16.63 , 20.06 ± 3.41 , 5.10 ± 0.32 , 2.48 ± 0.15 , 1.40 ± 0.08 , and 0.96 ± 0.01 μ s with V_{DD} of 1, 2, 4, 6, 8, and 10 V, respectively. These stage delay values are approximately 1 ~ 2 orders of magnitude better than those of the reported oxide-based ROs with the same V_{DD} [27], [30], [32], [33]. Such a small stage delay of ~ 1 μ s is highly attractive for some newly emerging applications where the need for speed is intrinsically limited by biology [38]. The oscillation frequency of the CMOS RO depends on the transit frequency of the TFT, which is proportional to $\mu/[L_{ch}(L_{ch}+L_{ol})]$, where μ , L_{ch} , and L_{ol} represent the mobility, the channel length, and the length of the total overlapping area between the source/drain electrodes and the gate electrode, respectively [27]. Here, the total overlapping length between the source/drain electrodes and the gate electrode of the inverter is 10 μ m for reliable alignment. The τ is expected to be further improved if the parasitic capacitance caused by the overlap can be reduced.

B. Uniformity and Yield of Oxide-Based CMOS Circuits

The uniformity can be demonstrated by analyzing the output characteristics of 7-, 11-, 21-, 51-stage ROs. For RO,

$$1/f = 2 \cdot \tau \cdot n, \quad (2)$$

where $1/f$ should be linearly dependent on n because τ is constant for ROs based on uniform oxide semiconductor thin films with fixed V_{DD} . The linear dependences of $1/f$ on n with different V_{DD} are shown in Figs. 6(i) and 6(j). It is worthy to note that there are 940 TFTs in the tested ROs over a large sample area of 1.5 cm $\times$ 1.5 cm. It is obvious that our CMOS circuits exhibit extremely high uniformity. Fig. 6(k) shows the peak-to-peak voltages (V_{pp}) of ROs as functions of n . The V_{pp} increases as the n increases and equals the V_{DD} when n is 51. In addition, the 51-stage RO composed of 104 TFTs (52 IGZO TFTs and 52 SnO SnO TFTs) is the first medium-scale CMOS circuit fully based on oxide semiconductors, indicating the high yield of our oxide-based CMOS technology.

VI. CONCLUSION

Sputtered n-type IGZO and p-type SnO are employed to construct various CMOS circuits. The fabricated CMOS circuits include inverters, NAND, NOR, XOR, d latch, full adder, and 7-, 11-, 21-, 51-stage ring oscillators.

The fabricated CMOS inverters show rail-to-rail output voltage, high gain up to 131.57, high noise margin of ~40% V_{DD} , low average static power consumption (8.84 nW when V_{DD} = 4 V), and high uniformity with negligible standard deviation.

The main feature of the basic logic gates, d latch, and full adder is rail-to-rail outputs. The d latch and full adder are typical sequential logic circuit and combinational logic circuit, respectively. The desaiably ideal input-output characteristics of the d latch and full adder indicate that our oxide semiconductors have the capability to construct complicated CMOS ICs for various applications in flexible and transparent electronics.

Finally, 7-, 11-, 21-, and 51-stage ring oscillators are presented to systematically evaluate the speed, uniformity, and yield of our CMOS circuits. The stage delay is ~ 1 μ s with a supply voltage of 10 V, which is highly attractive for some newly emerging applications such as human-machine interfacing. The linear dependence of the oscillation period on stage number of ring oscillator indicates the extremely high uniformity and yield over a large sample area of 1.5 cm $\times$ 1.5 cm.

The experimental data confirm that it is highly potential to build low-power, large-area, large-scale, and high-performance transparent/flexible CMOS circuits fully based on oxide semiconductors for applications beyond flat-panel displays.

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