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Bandwidth-to-Area Comparison of Through Silicon Vias and Inductive Links for 3-D ICs

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Abstract—Three-dimensional (3-D) integration is a promising technology that can mitigate the deleterious effects of the increased interconnect length in modern ICs by vertically stacking dies. Through silicon vias (TSVs) and AC coupling have been proposed as communication interfaces between multiple stacked dies. This paper investigates these communication schemes for 3-D systems where the link bandwidth is treated as a constraint rather than an objective. A frequency dependent RC model for the TSV and the redistribution layer is employed. A first order delay analysis between the two schemes shows comparable performance, but a better area efficiency for the TSV. Considering, however, a multiplexing scheme shows that TSVs with a pitch lower than $20\ \mu\text{m}$ exhibit better bandwidth-to-area efficiency without multiplexing, while the inductive link demonstrates higher bandwidth-to-area efficiency ratio in comparison to TSVs with a pitch larger than $20\ \mu\text{m}$ for a 12 : 1 multiplexing ratio.

I. INTRODUCTION

High performance interfaces have appeared recently with the introduction of three-dimensional integration, such as Wide I/O 2 [1] and the Hybrid Memory Cube (HMC) [2], [3]. These interfaces exploit the low TSV latency to achieve high bandwidth communication for stacked memory dies supporting a bandwidth of up to $3.8\ \text{Tbps}$.

Additional manufacturing complexity, however, can limit the broad application of the TSV interfaces. Any mainstream CMOS process must be altered with the introduction of further processing steps, such as thinning, TSV etching, and copper filling [4]. The result is increased cost and potentially lower yield, factors that can hinder the high volume manufacturing of 3-D systems [5].

Alternatively, wireless interfaces based on inductive links can be solely manufactured by conventional 2-D processes without additional masks being deployed. The transmitter and receiver inductors can be concentrically placed in two back end of line (BEOL) interconnect layers while the supporting circuitry can be placed in the silicon area underneath. Since the inductive link is a current driven scheme, relatively long communication distances can be supported across a 3-D stack.

Recent works on TSV signalling and bandwidth optimisation [6], [7], as well as the aforementioned Wide I/O and HMC demonstrate that TSVs can achieve very high data rates. Nevertheless, an inductive link is capable of achieving comparable performance to the TSV. Additionally, TSVs occupy both silicon and wiring area, while the inductive links require primarily interconnect resources. Consequently, the

area occupied by each interface should also be considered to provide a fairer comparison.

This work focuses on performance and area metrics for the two interconnect interfaces. A comparison is made between a TSV link comprising TSVs along with the redistribution layer (RDL) and an inductive link scheme, including both the on-chip inductor and the necessary receiver and transmitter circuits. Signal multiplexing is also considered for the two interfaces, investigating the related area and bandwidth trade-offs.

The paper is organised as follows. The frequency dependent TSV model used in this analysis is introduced in Section II. The inductive link transceiver is described along with the CMOS planar spiral inductor model in Section III. Simulation results concerning the performance of the interfaces are presented in Section IV. Some conclusions are offered in the last section.

II. FREQUENCY DEPENDENT TSV MODEL

In this section the frequency dependent electrical models of the TSV and the RDL are described. Also, a TSV array is introduced, including the capacitive TSV to TSV coupling.

A TSV is modelled as a cylindrical copper wire, surrounded by a liner as shown in Fig. 1. The TSV geometry incorporates the landing pads [8].

Fig. 1: Physical TSV model, including the landing pads [8].

Based on the given geometry, the RC model of the TSV is extracted. The total resistance and capacitance, respectively, are $R_{TSV} = R_{pillar} + 2 \times R_{bump}$ and $C_{TSV} = C_{ox} + 2 \times C_{bump}$ assuming that the size and geometry for each bump is the same. For the resistance R_{TSV} , a frequency dependent model is considered to describe the skin effect. The expressions used

for the resistance are based on [8]. The TSV pillar is modelled as a MOS capacitor and therefore the capacitance C_{ox} is determined from [9]. The capacitances of the bumps are also given in [8].

For the redistribution layer, the resistance R_{RDL} , is also modelled as frequency dependent based on [8]. Furthermore, closed-form expressions from [10] are employed to model the ground and coupling capacitances of the RDL. The overall capacitance is denoted as C_{RDL} . The length of the RDL wires depends on the size of the TSV array and can have a significant impact on the overall interconnect performance.

The circuit used in Spectre simulations to evaluate the delay of an inter-tier wire is depicted in Fig. 2. A 90 nm technology is assumed [11]. The driving strength m_x of the driving buffer is equal to $m_x = 32$, the largest assumed buffer size for this technology. This size is chosen to ensure signal integrity along the interconnect. A nominal load of $C_L = 5 \text{ fF}$ is chosen for the simulations. The assumed length for the wire used in a $N \times M$ array is $\frac{N}{2} \times \frac{M}{2} \times \text{pitch}_{TSV}$, although the exact length depends on the routing algorithm and the design of the circuit. This assumption, however, can be considered valid for a first order analysis. The bandwidth of a TSV interface for an array of $N \times M$ TSVs is [6]

$$BW = \frac{N \times M}{\tau_d}, \quad (1)$$

where τ_d is the 50% delay of the propagated signal. The $1/\tau_d$ provides an upper limit of the communication scheme bandwidth that can be achieved by a single TSV.

Fig. 2: Electrical circuit for an inter-tier wire.

A TSV array with $N = M = 3$ is shown in Fig. 3, where the coupling between the TSVs is also depicted. Any larger $N \times M$ array is assumed to have the same square like topology as the plotted 3×3 array. Contributions of farther TSVs to the capacitance of the TSV in the centre are of second order and consequently are ignored. The delay of the central TSV is considered as the baseline to determine the bandwidth of the overall array. The capacitive coupling, $C_{coupling}$ is modelled with expressions from [8], with the distance between two adjacent TSVs being pitch_{TSV} . The distance between diagonal TSVs is $\sqrt{2}\text{pitch}_{TSV}$ and $C_{Coupling,diag}$ is the corresponding capacitance. The overall coupling capacitance depends on the number of neighbouring TSVs.

III. INDUCTIVE LINK MODEL

An on-chip planar spiral inductor model is described in this section. The receiver and transmitter circuit are also introduced. The used technology is based on the PTM models [11] with $V_{dd} = 1V$.

A first order model of an on-chip spiral inductor model is assumed to describe the RLC characteristics of the inductor, as depicted in Fig. 4. Rectangular inductor geometry

Fig. 3: A 3×3 TSV array illustrating the capacitive coupling between neighbouring TSVs.

is considered. The current sheet approximation expression is used to determine the self inductance of the structure [12]. Furthermore, expressions from [13] are used to determine the parasitic capacitance. The parasitic capacitance includes both the area and periphery of the structure. The resistance is determined based on the same model also used for the resistance of the RDL.

Fig. 4: Electrical model of the inductor.

To design the inductor, certain guidelines are followed. The inductor inner diameter is at least $5 \times w$, where w is the width of the spiral turns. This diameter is required because there should be sufficient area for the magnetic flux to flow. In addition, the spacing between adjacent turns of the inductor is also minimum, thereby maximising the magnetic flux [14].

The voltage input data to the transmitter is converted into a current flowing through the inductor of the transmitter. This current induces magnetic flux to the coupled inductor of the receiver. A hysteresis comparator in the receiver detects the induced voltage and converts this voltage into the data pulse. The receiver inductor is tapered with the voltage bias, V_b , to facilitate the successful recovery of the signal. The voltage bias V_b is set to $V_{dd}/2$.

Simulations are performed to verify the operation of the transceiver circuit up to a data rate of 20 Gbps, using (1) and $N \times M = 1$. Different inductors have also been implemented, including the parasitics R_s and C_{ox} as shown in Fig. 4.

IV. RESULTS

Simulation results concerning the performance of a single TSV, a TSV array, and an inductive link array are presented in Subsection IV-A. A comparison between the two interfaces is presented in Subsection IV-B. The effect of multiplexing on the interface bandwidth-to-area ratio is investigated in Subsection IV-C.

A. Performance Analysis

The delay τ_d for the TSV interface is shown in Table I. The increasing TSV diameter has a negative effect on the delay,

because of the increased capacitance. In low frequencies, the TSV is capacitance dominated and thus the increased capacitance leads to an increase in delay, although the resistance decreases.

However, the situation is different when a TSV array is considered. To investigate the effect of both the TSV and the RDL, TSVs with diameters of $5\ \mu\text{m}$, $10\ \mu\text{m}$ [15], and $7.5\ \mu\text{m}$ [16] and pitch of $20\ \mu\text{m}$, $30\ \mu\text{m}$, and $40\ \mu\text{m}$, respectively, are assumed. TSV technologies from [15] are closer to the state-of-the-art, while [16] demonstrates a developmental fabrication process. The performance of several TSV arrays is also listed in Table I where the results in columns 3 and 4 indicate that as the size of the array increases, the effect of the RDL on τ_d dominates over the TSV delay.

TABLE I: TSV Array Delay for Different TSV Pitches.

TSV Count	TSV Delay [ps]		
	20 μm	30 μm	40 μm
1	35.4	50.9	45.6
4×4	38.7	55.7	51.8
8×8	44.4	63.9	63.0
16×16	55.9	80.5	85.5

A comparison between a single TSV and one TSV within an array demonstrates the overall effect of the RDL on the interface performance. The bandwidth is decreased by 57.6% in the case of a $20\ \mu\text{m}$ and a 16×16 array. Equivalently, a decrease in bandwidth of 87.5% is shown when the pitch is $40\ \mu\text{m}$.

Alternatively the delay of the inductive link is almost constant at $50\ \text{ps}$, indicating a bitrate of up to $20\ \text{Gbps}$ per link. Two inductors are deployed to verify this assumption. Inductor I with an inductance of $3.4\ \text{nH}$ and outer diameter of $84\ \mu\text{m}$, has a delay of $49.7\ \text{ps}$. Inductor II has characteristics of $3.6\ \text{nH}$ and $87\ \mu\text{m}$, respectively, and a delay of $51\ \text{ps}$. Inductor I demonstrates a slightly lower delay due to reduced parasitics. The selected inductors can support signal transmission for distances similar to the length of the investigated TSV technologies allowing a fair comparison between the two schemes.

B. Performance Comparison

As discussed in the previous subsection, the performance for both interfaces is comparable. However, the area must also be considered to investigate the interface communication density. The area of a single TSV is $\text{area}_{TSV} = \text{pitch}^2$, while the inductive link occupies an area of $\text{area}_{IL} = d_{out}^2$.

Nevertheless, the silicon area and the interconnect area differ for each interface. A TSV based on a via-last process occupies both silicon and interconnect area, and therefore $\text{area}_{s,TSV} = \text{area}_{TSV}$ and $\text{area}_{i,TSV} = l \times \text{area}_{TSV}$, where $\text{area}_{s,TSV}$ and $\text{area}_{i,TSV}$ are the silicon and interconnect area, respectively, and l the number of metal layers. Alternatively, the silicon area occupied by the inductive link is equal to that of the transceiver ($TxRx$) circuit, $\text{area}_{s,IL} = \text{area}_{TxRx}$. The interconnect area is $\text{area}_{i,IL} = 2 \times \text{area}_{IL}$, as only the topmost 2 layers are used.

Subsequently, a comparison can be made using a bandwidth per unit area efficiency metric,

$$\text{eff}_x = \frac{BW_x}{\text{area}_x}, \quad (2)$$

where x denotes either TSV or IL for the inductive link. The bandwidth area efficiency for each interface is listed in Table II, where $l = 6$ layers are considered. As the TSV pitch increases from $20\ \mu\text{m}$ to $40\ \mu\text{m}$, the overall efficiency eff_x drops by 80.6%. Nonetheless, eff_{TSV} remains nearly 4 times larger than eff_{IL} , indicating a greater performance.

TABLE II: Interface Bandwidth-to-Area Efficiency.

Interface [μm]	$\text{eff}_{s,x}$ [Mbps/ μm^2]	$\text{eff}_{i,x}$ [Mbps/ μm^2]	eff_x
TSV, 20 μm	71.2	11.8	71.2
TSV, 30 μm	21.7	3.6	21.7
TSV, 40 μm	13.8	2.3	13.8
IL, 84 μm	2.7×10^3	1.4	2.8

As for the interconnect area efficiency, $\text{eff}_{i,x}$, the same conclusion can be drawn that the TSV interface performs better than the inductive link, despite using all the metal layers. However, the silicon area efficiency, $\text{eff}_{s,x}$ leads to a different result. Because the silicon area used by the transceiver circuit of the inductive link is 0.01% of the minimum wiring area required, the $\text{eff}_{s,IL}$ is an order of magnitude larger than $\text{eff}_{s,TSV}$. This situation implies that the added silicon area is available to be used for signal multiplexing or other circuits, decreasing the overall area overhead of the inductive link.

C. Interface with Multiplexing

To investigate the effect of multiplexing on bandwidth-to-area ratio, a $90\ \text{nm}$ mux-demux is considered, from [17]. The 4:1 multiplexer has an area of $540\ \mu\text{m}^2$, while the 1:4 demultiplexer an area of $1160\ \mu\text{m}^2$, respectively. The communication clock is assumed at $1\ \text{GHz}$.

Multiplexing affects the silicon area a TSV link requires in addition to limiting the data rate due to the latency imposed by the multiplexer-demultiplexer circuit. Depending on the diameter of the TSV and the multiplexer size, the area efficiency of the TSV interface departs from the bounds mentioned previously. For the inductive link, however, a considerable silicon area is available. This area can be reserved for multiplexing without incurring any additional area cost as compared to the TSV link. A trade-off between the multiplexing size and the performance-area efficiency of the interfaces is explored to determine the highest area efficiency.

A multiplexing size of up to 12:1 can be implemented using the multiplexer from [17]. The interface efficiency is depicted in Fig. 5 for each scheme. For the TSV interface, two trends can be observed. For TSV pitches less than $20\ \mu\text{m}$, the interface performs better without multiplexing and as the multiplexing size increases, the efficiency drops. However, for TSVs with pitches greater than $30\ \mu\text{m}$, multiplexing increases the system efficiency. As shown in Fig. 5, eff_{TSV} moves asymptotically towards $1.5\ \text{Mbps}/\mu\text{m}^2$.

This behaviour occurs as the area of the multiplexing circuits demand more silicon area compared to TSVs. For a

data rate of 1 Gbps and no multiplexing, the interface size is equal to the area occupied by the TSVs. A decreasing TSV diameter would lead to a quadratic increase in the area efficiency of the interface. However, including signal multiplexing this behaviour changes. As the multiplexing ratio increases, the efficiency of the interface saturates to a value, depending on the ratio between the pitch of the TSV and the area of the multiplexer.

Fig. 5: Efficiency for a TSV and inductive link interface with increasing multiplexing density.

On the contrary, eff_{IL} exhibits an almost linear increase up to a 12:1 multiplexing ratio. The reason is that the silicon area beneath a single inductor can fit the multiplexing circuits, without adding to the overall area. Increasing the multiplexing density, the interface efficiency increases, reaching 1.7 Mbps/μm² proving a better solution than the TSV interface for TSV pitch either 30 μm or 40 μm.

An area projection for increasing bandwidth is depicted in Fig. 6. The best case scenario for each interface has been considered. The vertical lines in the figure are the bandwidths of Wide I/O [1], HMC I [2], and HMC II [3] depicted with the dashed, dotted, and dashed-dotted lines, respectively. If the TSV pitch is smaller than 20 μm, no multiplexing produces a higher performance. The added silicon area due to the multiplexer-demultiplexer degrades the bandwidth-to-area efficiency as the multiplexing density increases. Alternatively, if the pitch is larger than 30 μm, the increasing multiplexing density increases also the bandwidth-to-area efficiency.

An inductive link, alternatively, exhibits a better bandwidth-to-area efficiency with signal multiplexing, particularly in comparison to larger TSVs. Specifically, when the multiplexing ratio increases over 8:1, the inductive link has a better bandwidth-to-area efficiency over a TSV interface. However, the linear increase in the inductive link efficiency diminishes as soon as the available silicon area under the inductor is taken up by the mux-demux circuits. As high density placement of the inductors can be achieved [18], an inductive link can substitute a TSV interface as a high density communication scheme under these circumstances.

V. CONCLUSIONS

This work compares the bandwidth-to-area efficiency for TSV and inductive links. The maximum performance both interfaces can deliver is comparable, however, TSVs occupy

Fig. 6: Die area for TSV and inductive coupling links when multiplexing is used.

significantly less area per signal. However, if signal multiplexing is implemented the area consumption of the two interfaces is similar with the inductive link supporting more efficiently multiplexing ratios greater than 8:1.

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