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Advanced Circuit Interface for Maintaining Performance in Systems with Multiple Voltage Domains

Harry Kalargaris, John Goodacre, and Vasilis F. Pavlidis
Advanced Processor Technologies Group
School of Computer Science, University of Manchester
{*charalampos.kalargaris, john.goodacre, vasileios.pavlidis*}*@manchester.ac.uk*

***Abstract*—Multi-level voltage scaling is one of the most effective techniques for reducing power without sacrificing speed in an integrated circuit (IC). However, additional circuitry is required at the interfaces of the circuit blocks which operate at different voltage levels. These circuits impose a significant delay overhead and restrict the use of multi-voltage scaling at blocks where critical paths traverse their interfaces. A by-pass circuit is proposed to alleviate these timing issues under specific operation conditions. The new circuit results in significant performance improvements of up to 89% and power reduction up to 52% compared to a traditional feedback-based level-up shifter in a 32 nm technology node. Furthermore, greater performance and power savings are demonstrated when more cells are being by-passed, such as the isolation cells.**

I. Introduction

A traditional challenge for the semiconductor industry is the reduction of power dissipation without compromising the performance of a system. Various methodologies have been proposed for decreasing power, such as clock [1] and power gating [2], gate level power optimization [3], multi-voltage supply (multi-V_{dd}) [4], multi-threshold logic [5] and power sequencing [6]. Multi-V_{dd} and power sequencing are the most efficient techniques for reducing power consumption due to the quadratic dependency of dynamic power on supply voltage. Additionally, multi-voltage is a technique where performance is considered alongside power, as in modern SoCs, different blocks have different performance objectives and constraints [4].

However, several challenges arise in the design process for multi-V_{dd} and power sequencing systems, notably at the interfaces of the blocks. The primary difficulty of utilizing these techniques in a system, is the necessity of additional circuitry at the interfaces between blocks which operate on different voltage supplies. Signals should propagate between blocks that utilize different power rails. Therefore, additional circuits are required to scale up/down signal voltage and retain the previous state or clamp signals to a specific state when a circuit block is powered down [6]. These interface circuits, particularly level-up shifters that translate the signal from a low voltage to a high voltage, add significant delay on those paths where these level shifters are employed. Therefore, research effort has been placed to improve the performance of these cells [7]-[10]. A traditional feedback-based level-up shifter is adopted at 0.35 μm technology node in [7] to support "by-passing" functionality by employing pass transistors. Furthermore, multi-threshold cells are employed to improve the power and the performance of level-up shifters in [5]. However, in deep submicrometer technologies, the supply voltage headroom is smaller than the voltage threshold, therefore pass transistors drive weak signals not able to support voltage conversion. In addition, in a multi-threshold CMOS technology, the available threshold voltages are limited to few discrete values, thus decreasing the effectiveness of the proposed design in [5].

Furthermore, the additional delay of these cells hinders the timing closure for a circuit. This behavior limits the use of multi-voltage scaling at blocks where critical paths traverse their interfaces. A typical example of this situation can be observed in cached CPUs [6], where a core can usually operate at a lower voltage than level 1 (L1) cache[1] to yield further power reduction. However, the timing critical paths often include the interconnections between the core and the cache. To enable different power supplies between the cache and the core, voltage interface circuits should be added which entail considerable delay penalty. Consequently, to avoid a performance loss the power supply remains the same for both the L1 cache and core and is scaled less aggressively. This situation leads, in turn, to limited power savings.

To mitigate this issue, an advanced interface circuit for maintaining performance in systems with multi-level power voltages is presented. The novelty of this design is based on the principle that in a multi-voltage scaling environment, different blocks can have the same voltage in specific operation conditions, thus the additional circuitry can be by-passed. This circuit interfaces different voltage domains and is suitable for by-passing several cells, such as level shifters, clamp/isolation cells, and retention flops employed in multi-V_{dd} and power sequencing techniques. The performance of the circuit is investigated in several operating conditions, typically employed in systems with multi-voltage scaling power supplies. In addition, as several types of circuits can be by-passed, depending on the complexity of the interface, the merit of employing the proposed circuit across all these scenarios is evaluated.

The paper is organized as follows. In Section II, the proposed circuit is described and a discussion about which additional circuits can be by-passed is presented. In Section III, the simulation setup and results on the performance and

[1]The voltage required for stable operation in memory elements is typically higher than standard logic cells [6].

power of the proposed circuit are discussed. Some conclusions are offered in Section IV.

II. By-Pass Circuit Design

In this section, the design of the by-pass circuit is described. The proposed interface circuit is based on the notion that in a multi-voltage scaling environment, different blocks will have the same voltage in specific (e.g. high performance) operating conditions. Hence, the required additional circuitry required by multi-V_{dd} and power sequencing techniques can be circumvented. The proposed by-pass circuit comprises 3 transmission gates and an $NMOS$ transistor around the additional cells, as illustrated in Fig. 1. The first two transmission gates ($TG1$ and $TG2$) operate as a demultiplexer which takes a single data input and using the control signal (Sel) outputs the data accordingly to one of the two paths. The transmission gate ($TG3$) ensures that no current flows through the by-passed circuit. Furthermore, the $NMOS$ transistor ($MN1$) strongly pulls low the input of the interface circuit, thereby avoiding undesirable switching and leakage due to a weak ground at the $Node\ 1$, which can result when $TG1$ is off.

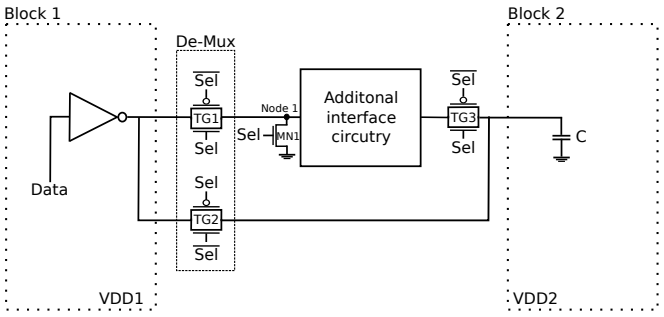

Fig. 1. Proposed circuit at the block interface to by-pass the additional cells used to support multi-level power supply.

In the simplest scenario, where only one interface cell, such as a level-up shifter, needs to be by-passed, the circuit operates as follows. If the voltage domains operate at different voltages, Sel is set high and the level shifter is employed to amplify the signal. If the voltage domains are at the same voltage, Sel is set low and the fast path is utilized to by-pass the level shifter. In addition, $MN1$ is enabled to ground the output of the $TG1$ and the $TG3$ is turned off to prevent current flowing backwards.

The by-passing circuit is oblivious to the type of the interface employed, thus being applicable to all types of interfaces circuits, such as isolation cells and retention flops in addition to voltage shifters. Furthermore, latches that synchronize the interface between blocks in two different voltage domains can be by-passed in high performance mode where the frequency ratio between these blocks is 1:1. In the case where the interface is complex and contains several components connected in-series [6], the benefits from by-passing this interface are higher. Alternatively, for signals with multiple fan-out, a demultiplexer with a higher demultiplexing can be employed, extending the present circuit by flanking each interface circuit with two transmission gates and maintaining the low latency by-pass path for the iso-power supply operating conditions.

In a circuit with multiple power supplies, different strategies of multi-V_{dd} lead to different methods of generating the control signals. In a multi-level voltage scaling (MVS) system, where a few and fixed, voltage levels are supported for different operating conditions, the power management unit can be programmed to generate these signals [6]. In the same manner, select signals can be generated in a dynamic voltage and frequency scaling (DVFS) environment. The details of generating the selection signals from the power management unit is beyond the scope of this work. Furthermore, in an adaptive voltage scaling scheme (AVS), where a control loop is used to adjust the voltage of different blocks, the proposed circuit in [11] can be utilized for generating the control signal(s).

III. Speed and Power Analysis

The simulation setup and the effectiveness of the proposed circuit in terms of propagation delay and power are presented in this section. The by-pass interface circuit is simulated with HSPICE® [12] at a 32 nm technology node [13] and pre-designed circuits for level conversion and isolation states are obtained from the Synopsys® 32 nm generic library [15]. The nominal operating voltage for 32 nm CMOS technology is 1 $Volt$ [13]. Therefore, a typical $-/+0.2\ Volt$ swing from nominal supply voltage ([14]) is considered for low-power/high-performance conditions in a multi-voltage environment. The proposed circuit is simulated in a variety of operating scenarios listed in Table II. Blocks 1 and 2 can be considered as the core and the L1 caches, respectively. The first three scenarios (A, B, C), represent the situation where the core operates in reduced voltage as compared to L1 to maximize power savings. Alternatively, scenarios D and E represent nominal, and high performance modes respectively of the same voltage for both blocks.

TABLE I. Simulated Scenarios of the Proposed Circuit.

Operating Scenarios			**Supply Voltage [V]**	
Mode	Objective	Notation	Block 1	Block 2
Level Shifting	Power Savings	A	0.8	1
		B	0.8	1.2
		C	1	1.2
By-Pass	Nominal Performance	D	1	1
	High Performance	E	1.2	1.2

A. Performance Analysis

As mentioned in the previous section, systems supporting multi-V_{dd} and power sequencing require additional cells to ensure the correct operation at the boundaries of blocks that operate at different supply voltages. The components that pose the greatest propagation delay on the path of the interface are the level-up shifters. Therefore, the feedback-based level-up shifter (FLS) [16], which is broadly used [6], [15], is utilized in our by-pass design for performance characterization.

The performance traits of the proposed interface circuit (PC) in a multi-voltage scaling system are illustrated in Fig. 2. At the same operating voltages, the propagation delay is decreased, on average (D and E), by 86%, where level shifters are by-passed. In the case where the blocks are supplied by the highest voltage assumed for the employed technology node, which indicates that the highest speed mode is enabled (E), the

delay decreases by 89%. Therefore, potential timing issues due to the considerably delay of the level shifters can be effectively alleviated. In contrast, if the interconnected blocks operate at different voltages (A, B, C), there is an overhead in delay of 10.7%. However, this overhead is negligible for the entire path as these modes represent the power saving modes of a multi-level voltage scaling system. Therefore, timing closure is less of an issue at these low-speed modes. Furthermore, if isolation cells are also connected in-series with the shifters, the performance improvements are further increased, on average (D and E), by 92% while the delay overhead at low-speed modes (A, B, C) remains low, on average, at 9.5% (see Fig. 3).

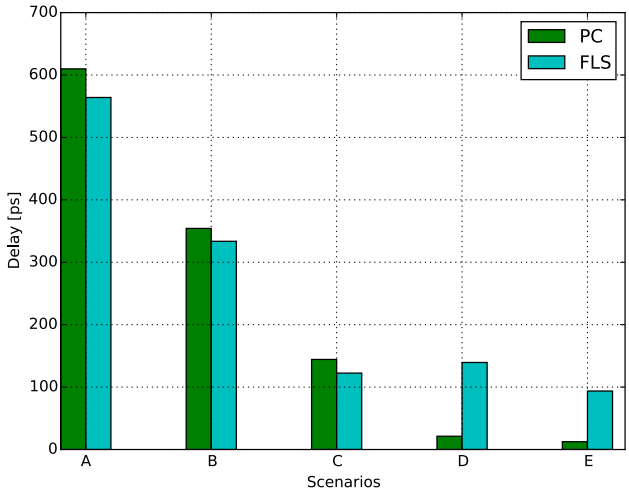

Fig. 2. Delay of the proposed by-pass circuit compared to traditional level-up shifters.

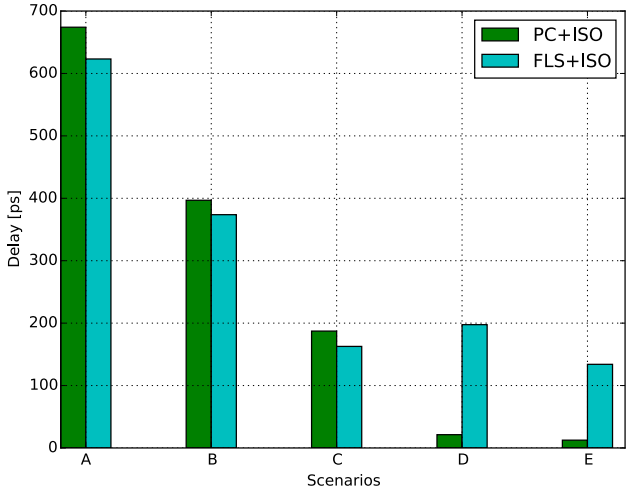

Fig. 3. Delay of the proposed circuit as compared when isolation cells are connected in series with level-shifters.

Moreover, paths, which traverse critical blocks in two industrial circuits (Ind 1 and Ind 2), are simulated at high performance mode (see Table II) to capture their latency on a variety of additional interface circuits. The results are listed in Table III. In the case where level shifters are utilized, the latency of these paths is increased by 4.8% and 9.7% for Ind 1 and Ind 2, respectively, as compared to where no additional circuit is employed. Furthermore, the delay increased even more, if isolation cells are also connected in-series with the shifters, by 7.7% for paths in Ind 1 and 13.8% for Ind 2. However, the additional delay of the proposed circuit is negligible as the latency of these paths is increased by 0.69% for Ind 1 and 2% for Ind 2. This behavior demonstrates that traditional timing obstacles at the critical interfaces of blocks are effectively alleviated in high performance conditions at multi-V_{dd} systems by employing the proposed circuit. Note also, that latches are utilized in the first industrial circuit path. Hence, in the case where the proposed circuit by-passes the latches in high performance mode, 5% decrease is observed to the latency of this path.

TABLE II. MAXIMUM LATENCY FOR THE INVESTIGATED PATHS AT HIGH PERFORMANCE MODE.

Interface Circuit	**Latency [ps]**		**Performance Losses [%]**	
	Ind 1	Ind 2	Ind 1	Ind 2
No Interface	1154	700	-	-
By-Pass	1162	715	0.69	2.1
LS	1210	768	4.8	9.7
LS+ISO	1243	797	7.7	13.8

B. Power Analysis

In this subsection, the power consumed by the proposed circuit is investigated. Multi-level voltage scaling and power sequencing are the most efficient techniques for reducing power consumption due to the quadratic dependency of dynamic power on supply voltage. The power improvements of utilizing these techniques are orders of magnitude greater ($\sim W$) as compared to the power losses ($\sim \mu W$) of the additional interface circuits [6]. In spite of that situation, handling carefully these cells can further decrease power.

The proposed circuit dissipates up to 52% less power by employing the by-pass path where the same supply voltage is applied to both interfaced circuits (D, E), as depicted in Fig. 4. In contrast, an overhead (average 6.8%) exists when the level shifters are employed (A, B, C), due to the transmission gates. In addition, this power overhead drops, on average (A, B, C), to 5% where more cells are being by-passed, such as isolation cells, as illustrated in Fig. 5. In this situation, the power improvements are greater (up to 58.2%), where the same voltage is applied to both blocks (D, E). Hence, the operating scenarios must be considered alongside the number of the additional cells in the design process in order to minimize the power consumption for this proposed circuit.

C. System Level Savings

Modern mobile cached CPUs spend most of the operating time ($\sim$ 70%, [17]) in the idle state, where the same lowest voltage, defined by L1 caches, is applied to both core and L1 caches. In an ARM11 cached CPU at 90 nm technology node, the 86% of power is dissipated on core where the remaining 14% on L1 caches [18]. Hence, reducing the voltage of core even lower than L1 caches can result to huge power savings.

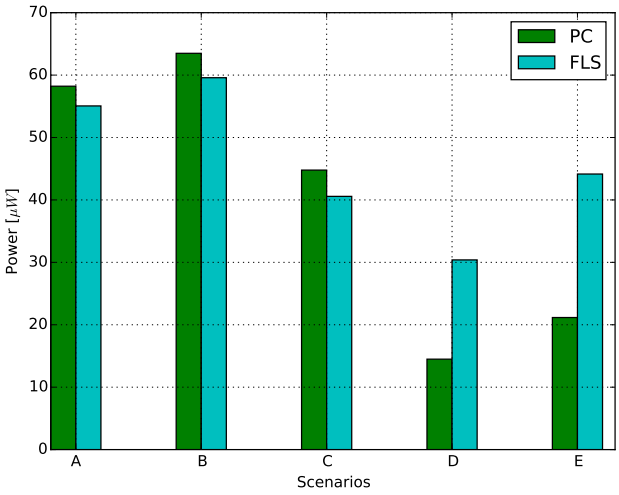

Fig. 4. Power dissipation of the proposed by-pass circuit compared to traditional level-up shifters.

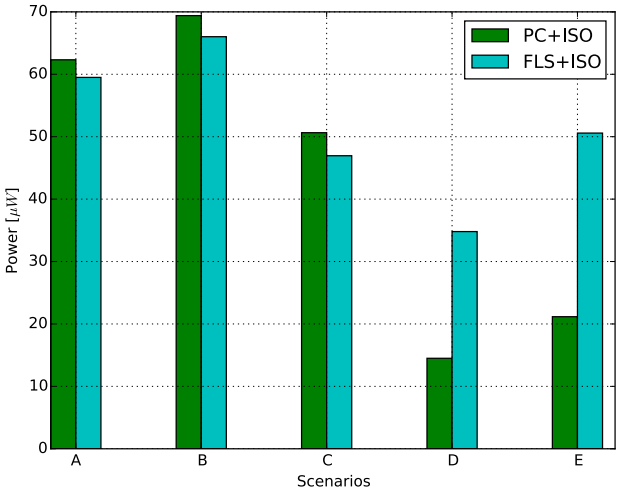

Fig. 5. Power dissipation of the proposed circuit compared to traditional level conversion circuits where isolation cells are also connected in series with the shifters.

However, due to the additional circuits, timing issues arise on the interfaces of these blocks on high demand workload, limiting the applicability of multi-V_{dd} to these blocks. Therefore, the proposed circuit can efficiently enable assignment of multi-V_{dd} to these to blocks and maximize the power savings by reducing even lower the voltage of the core. This is due to its capability of alleviating the timing issues from the interfaces at high performance states and employing the additional circuits at power saving modes.

IV. Conclusions

In this paper, a by-pass circuit for multi-voltage scaling systems is presented. The key idea is that in a multi-voltage scaling environment, different blocks will have the same voltage in specific operating conditions. Consequently, the interface circuits can be detoured to avoid performance losses where high speed operation is required. The proposed circuit is simulated under different operating scenarios at a 32 nm technology node. The proposed by-pass circuit is compared with the traditional feedback-based level-up shifter, where speed is enhanced by up to 89% and power consumption is decreased up to 52% where the blocks operate at the same supply voltage. In the case where the proposed circuit is utilized in critical paths of industrial circuits the frequency reduction is negligible (0.69% and 2.1%) as compared to paths frequency where no additional circuit is employed. This behavior demonstrates that traditional timing obstacles at the critical interfaces of small blocks are effectively alleviated in high performance conditions at multi-V_{dd} systems by employing the proposed circuit. Thus, enabling assignment of multi-V_{dd} in smaller blocks (e.g core and L1 caches) in order to maximize power savings. Furthermore, greater performance and power savings are demonstrated if more cells are being by-passed, such as the isolation cells.

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