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Half-Volt Operation of IGZO Thin-Film Transistors Enabled by Ultrathin HfO₂ Gate Dielectric

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Amorphous indium-gallium-zinc oxide (a-IGZO) thin-film transistors (TFTs) enabled by an ultrathin, 5 nm, HfO₂ film grown by atomic-layer deposition were fabricated. An ultra-low operation voltage of 1 V was achieved by a very high gate capacitance of 1300 nF/cm². The HfO₂ layer showed excellent surface morphology with a low root-mean-square roughness of 0.20 nm and reliable dielectric properties, such as low leakage current and high breakdown electric field. As such, the a-IGZO TFTs exhibit desirable properties as low power devices, including a small subthreshold swing of 75 mV/decade, a low threshold voltage of 0.3 V, and a high on/off current ratio of 8×10^6 . Furthermore, even under an ultralow operation voltage of 0.5 V, the on/off ratio was also up to 1×10^6 . The electron transport through the HfO₂ layer has also been analyzed, indicating the Poole-Frenkel emission and Fowler-Nordheim tunneling mechanisms in different voltage ranges.

Recently, there are emerging applications of thin-film transistors (TFTs), such as wearables electronics¹, sensors², and thin-film circuits³. However, these devices are challenged by limited battery lifetime, therefore low-voltage operations are highly desirable and even necessity. Among various TFTs channel materials, wide band gap oxide materials are naturally suited to battery-operated electrics due to the very low off current. In 2004, Hosono et al.⁴ first reported room-temperature fabrication of TFTs using amorphous indium-gallium-zinc oxide (a-IGZO). After that, a-IGZO has received much attention because of its excellent performance, including high electron mobility, low off current, excellent uniformity, surface flatness, stability, optical transparency, large-area production, and wide process temperature.^{5,6} As such, a-IGZO TFTs have started replacing amorphous-silicon transistors in large-area displays.^{7,8} However, large voltages are often needed for a-IGZO TFTs to achieve high mobility and high on/off current ratios.

To reduce the operation voltage of TFTs, large gate capacitance is a necessity. Reducing the thickness of gate dielectric layer is one of the methods to increase the capacitance, but the thickness reduction of the conventional SiO₂ gate dielectric is limited by the tunneling current. Fortunately, using high-dielectric-constant (high-*k*) materials to replace SiO₂ as gate layer can simultaneously enable a low leakage current and a low-voltage operation. Various high-*k* materials, e.g., Y₂O₃⁴, Al₂O₃,^{9,10} HfO₂,^{2,11} Ta₂O₅,¹² HoTiO₃,¹³ HfLaO,^{14,15} LaLuO₃,¹⁶ LaAlO₃,¹⁷ have been reported for a-IGZO TFTs. However, for high-*k* materials, there is a general phenomenon that the band gap decreases with the increase of the *k* value.¹⁸ Therefore, to avoid a large leakage current, a high-

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quality dielectric layer with a large enough band gap is necessary. Among these high- k candidates, Al_2O_3 has a large band gap ($E_g = 8$ eV), and in our previous work we have demonstrated that ultrathin Al_2O_3 film can be a highly reliable dielectric in a-IGZO TFTs enabling a 1 V operation.¹⁹ However, the k value of Al_2O_3 is only ~ 9.0 . Robertson *et al.* reviewed different high- k materials.¹⁸ They pointed out that among various high- k materials, HfO_2 and Hf-silicate are preferred oxide due to the high enough k value ($k = 20\sim 25$), thermal stability, kinetic stability, and low bulk defect density.¹⁸ Chun *et al.* also proposed that HfO_2 and HfO_2 -based materials are the most promising gate dielectrics.²⁰ HfO_2 -based high- k materials have been employed as a gate dielectric since 45 nm CMOS logic circuits in the industry.²¹⁻²⁴ In this work, due to the large k value, the IGZO TFTs enabled by an ultrathin 5 nm HfO_2 gate dielectric are able to operate at 0.5 V, half that of our previous work.¹⁹ Importantly, HfO_2 has thicker physical thickness than Al_2O_3 for the same capacitance or the same equivalent oxide thickness (EOT), which can suppress the leakage current significantly. The thicker dielectric makes the TFTs much more stable and reliable, and is much more desirable than 5 nm Al_2O_3 considering substrate roughness. The HfO_2 film is usually grown by atomic-layer deposition (ALD) which can precisely control the film thickness with angstrom precision. However, very thin gate dielectrics have been found to show different dielectric properties from thick ones.^{19,25,26} So, it is worth exploring the characteristics of devices based on ultrathin high- k materials.

In this work, a-IGZO TFTs with an ultrathin 5 nm HfO_2 layer as the gate dielectric were fabricated. The HfO_2 films were grown by ALD at 150 °C using alternating precursors of tetrakis (ethylmethylamino) hafnium (TEMAH) and H_2O vapor at a deposition rate of approximately 0.11 nm per cycle. The carrier gas was N_2 and the pressure in chamber was 0.02 Torr during the deposition. The 5-nm HfO_2 film has been experimented to explore possible use in a-IGZO TFTs. We are able to show that even an ultrathin 5 nm HfO_2 film can be a highly reliable dielectric. The obtained TFTs exhibit excellent properties for low-voltage operations, including a small subthreshold swing (SS), a low threshold voltage (V_T), a high mobility (μ), and a high on/off current ratio ($I_{\text{on}}/I_{\text{off}}$). In particular, our a-IGZO TFTs can be operated at an extremely low voltage of half volt. This is, to the best of our knowledge, the lowest operating voltage reported to date, which may have useful implications for wearables or other low-power electronics based on thin film technology.

A schematic structure of the fabricated a-IGZO TFTs is shown in Fig. 1(a). A 5 nm HfO_2 layer was grown by ALD on an n-type heavily doped Si ($\text{n}^+\text{-Si}$) wafer. By using radio-frequency (RF) sputtering technology, a 10-nm a-IGZO was deposited through a shadow mask at room temperature to form the active layer. The fraction ratio of the $\text{In}_2\text{O}_3\text{:Ga}_2\text{O}_3\text{:ZnO}$ target is 1:1:1 mol. %. The RF sputtering power and Ar pressure were maintained at 90 W and 3.65 mTorr, respectively. Finally, Al source and drain contact electrodes were formed by thermal evaporation through a shadow mask. The active channel length (L) and channel width (W) of TFTs are 60 and 2000 μm , respectively. Upon completion of the contacts deposition, the devices were coated with a 400 nm PMMA (950 K, 4.5 wt. %) layer and then annealed in air at 150 °C for 0.5 h in order to reduce oxygen vacancies in a-IGZO film and suppress the H_2O adsorption.^{5,19} The capacitive properties of the HfO_2 gate

dielectric were investigated by metal-insulator-semiconductor (MIS, Al/HfO₂/p-Si) capacitors prior to a-IGZO TFTs fabrication. These devices were characterized by capacitance-voltage (C - V) and current-voltage (I - V) measurements using an E4980A Precision LCR Meter and Agilent B2900 Precision Source/Measure Unit (SMU). For a better understanding of the vertical carrier transport mechanism (related to leakage current), we applied large voltages to the MIS (Al/HfO₂/n⁺-Si) capacitors and fitted the leakage current curves by different modes. To further confirm the quality of HfO₂ layer, we investigated the surface morphology of the HfO₂ film by atomic-force microscopy (AFM).

Fig. 1. (a) Schematic diagram of the a-IGZO TFTs. (b) Transfer characteristics of device before and after thermal annealing. Output (c) and transfer (d) characteristics of a-IGZO TFTs with 5 nm HfO₂ gate dielectric.

Figure 1(b) shows the transfer characteristics of device before and after thermal annealing. The as-fabricated device could operate under 1 V with a large on/off ratio. However, the device needs to be turned off at a gate voltage of -0.7 V. Unlike chemically ALD-deposited HfO₂ films, sputtered-IGZO films often have unbalanced stoichiometry due to the high-energy ion bombardment.¹⁹ In general, oxide films deposited through sputtering contain a large number of oxygen vacancies causing a high conductivity. Thermal annealing in air is an effective method to reduce such vacancies.⁵ After annealing treatment, V_T was found to shift to 0.3 V as shown in Fig. 1(b), which indicates that oxygen vacancies in the a-IGZO film were reduced efficiently. The experimental results at different temperatures (not shown here) revealed that 150 °C was the optimum annealing temperature for maintaining a good carrier mobility and high on/off ratio. Furthermore, very little hysteresis is observed in the drain current versus gate voltage (I_D - V_G) transfer curve. This indicates that no significant mobile charges are present and that the density of slow interface traps is low, confirming a high quality of HfO₂ dielectric.¹⁷ Figure 1(c) shows the output characteristics of an a-

IGZO TFT with a 5 nm HfO₂ gate dielectric after 150 °C annealing treatment, exhibiting a well-defined pinch-off behavior. Figure 1(d) shows the transfer characteristics of a-IGZO TFTs with 5 nm HfO₂ gate dielectric under different drain voltages after 150 °C thermal annealing. The TFTs exhibit desirable properties including a low threshold voltage of 0.3 V, a small subthreshold swing of 75 mV/decade, and a high on/off current ratio of 8×10^6 . The low *SS* value in the 5 nm HfO₂ TFT is a result of the large gate capacitance. Importantly, we have realized 1 V operation of our a-IGZO TFTs by using the ultrathin 5 nm HfO₂ dielectric layer.

Fig. 2. (a) *C-V* characteristics and schematic diagram (inset) of an Al/HfO₂(5 nm)/p-Si MIS capacitor. AFM images of the (b) Si Wafer and (c) 5 nm HfO₂ film.

For TFT devices, large gate capacitance is very crucial to reduce the operation voltage. Researchers have showed that the properties of ultrathin gate dielectrics may be different from thick ones.^{25,26} The accurate value of gate dielectric capacitance (C_{ox}) plays a vital part in the calculation of carrier mobility and interface trap density (N_t), and thus MIS capacitors were made to confirm the capacitance of the thin HfO₂ layer. Figure 2(a) and the inset show the *C-V* characteristics and schematic cross-sectional view of an Al/HfO₂ (5 nm)/p-Si capacitor, respectively. A very high capacitance of $C_{ox} = 1300$ nF/cm² is determined, and this is capacitance of an equivalent SiO₂ dielectric of 2.6 nm. Such a thin SiO₂ dielectric, however, would be vulnerable to leakage current.

The performance of a-IGZO TFTs is known to directly associate with the interfacial quality between gate dielectrics and channel layer. The 5 nm HfO₂ dielectric film shows excellent surface morphology with a very low root-mean-square (RMS) roughness of 0.20 nm as shown by the AFM image in Fig. 2(c). The surface morphology of the Si substrate (RMS = 0.1 nm) is shown in Fig. 2(b). In addition, the quality of gate dielectric can also be manifested by the TFT subthreshold swing. Under 1 V operation voltage, the 5 nm HfO₂-based a-IGZO TFT exhibits a very low *SS* of 75 mV/decade, which is quite desirable to turn on the transistor effectively at low voltages. Furthermore, a high mobility μ of 4.6 cm²/Vs was achieved. The extremely small hysteresis in Figs. 1(b) and (d) indicate very low N_t at the gate dielectric interface, which also correlates well with the low HfO₂ surface roughness. The value of N_t can be determinate by:

$$SS = \frac{k_B T \ln 10}{q} \left[1 + \frac{q^2}{C_{ox}} N_t \right] \quad (1)$$

where k_B is Boltzmann's constant, T is the temperature in Kelvin, and q is the electron charge. Taking the SS value of the 5 nm HfO_2 IGZO TFTs, the interface trap density N_t is found to be $2.0 \times 10^{12} \text{ eV}^{-1} \text{ cm}^{-2}$, which is among the lowest values in reported HfO_2 TFTs to date.^{27,28}

The reproducibility and uniformity are challengeable for IGZO TFTs with such ultrathin gate dielectrics. Only a slight defect on the substrate or in the gate insulator should deteriorate the gate leakage current. We have repeated our experiments and fabricated a-IGZO TFTs on three n^+ -Si substrates (denoted as Samples A, B and C, respectively). We selected six TFTs on each sample randomly. The transfer curves of these devices are shown in Figure S1. From the graph our TFTs show good reproducibility and uniformity. The statistical distributions of a-IGZO TFTs characteristics of three samples are summarized in Table SI.

Fig. 3. Transfer (a) and output (b) characteristics of a-IGZO TFTs with 5 nm HfO_2 gate dielectric layer under 0.5 V operation voltage.

We further tested the TFTs based on 5 nm HfO_2 under lower operation voltages. Figures. 3(b) and (c) show the transfer and output characteristics of a-IGZO TFTs under 0.5 V operation voltage. A high $I_{\text{on}}/I_{\text{off}}$ ratio and well-behaved transistor output characteristics were still achieved. The mobility is $1.5 \text{ cm}^2/\text{Vs}$, somewhat lower than that at 1 V ($4.6 \text{ cm}^2/\text{Vs}$). This is not unusual because carrier trapping by interface states becomes more dominated at low gate voltages.¹⁹ Importantly, even under such low operation voltage, the on current is still about 6 orders of magnitude higher than the off current.

TABLE I. Comparison of our a-IGZO TFTs with those in the literature with different gate dielectrics.

Gate dielectrics	T_{ox} (nm)	V_{ON} (V)	V_T (V)	SS (mV/dec)	μ (cm^2/Vs)	$I_{\text{on}}/I_{\text{off}}$
Al_2O_3 ⁹	100	5	0.4	100	8	6×10^7
HfO_2 ²	60	0.8	0.2	90	5.9	2.4×10^7
HoTiO_3 ¹³	60	8	0.1	160	21.4	1.3×10^8
HfLaO ¹⁵	40	1.5	0.1	180	22.1	2×10^5
LaLuO_3 ¹⁶	20	2	0.3	310	6.6	1×10^3
HfO_2 ¹¹	20	2	0.2	109	8.1	1×10^7
LaAlO_3 ¹⁷	15.5	1.4	0.4	68	4.1	1×10^5

Al ₂ O ₃ ¹⁹	5	1	0.3	100	6.3	1.2×10^7
(This work)	5	0.5	0.1	75	1.5	1×10^6
	5	1	0.3	75	4.6	8×10^6

In Table I, we have compared the key device parameters of our a-IGZO TFTs with previously reported devices in which the thickness of gate dielectric (T_{ox}) is thinner than 100 nm. V_{ON} represents the operation voltage. Our devices show the lowest operating voltages in oxide semiconductor TFTs, which is favorable for wearables or other low-power electronics based on thin-film technology.

Fig. 4. (a) Breakdown tests (main graph) and schematic diagram (inset) of for Al/HfO₂/n⁺-Si MIS devices with 5 nm HfO₂ layer. The liner fitting for leakage current by (b) P-F emission and (c) F-N tunneling models.

To test the robustness of the 5-nm-thin HfO₂ and for deep analysis of the vertical carrier transport mechanism (related to leakage current), we applied large voltages to the MIS (Al/HfO₂/n⁺-Si) capacitors and fitted the leakage current curve by different modes. The breakdown voltage of 5 nm HfO₂ is found to be about 4.5 V as shown in Fig.4 (a). The breakdown electric field strength is comparable to other reports about HfO₂.^{29,30} There are a few possible electron transport mechanisms including direct tunneling, Poole-Frenkel (P-F) emission, Fowler-Nordheim (F-N) tunneling, and Schottky emission, etc.

The P-F emission is due to emission of trapped electrons into the conduction band. The I - V curves follow

$$I \propto V \exp\left[\frac{q}{k_B T} (2a\sqrt{V} - \phi_o)\right] \quad (2)$$

where a is a constant, ϕ_o is the barrier height.³¹

The F-N tunneling current is given by

$$\frac{J}{E^2} = C_1 e^{-C_2/E} \quad (3)$$

where J is the current density and E is the electric field across the oxide. C_1 and C_2 are given by

$$C_1 = q^3 m / 16\pi^2 \hbar m_{\text{ox}} \phi_o \quad (4)$$

$$C_2 = \frac{4}{3} \frac{(2m_{\text{ox}})^{1/2}}{q\hbar} \phi_o^{\frac{3}{2}} \quad (5)$$

where m and m_{ox} are the electron mass in free space and in the oxide, respectively, and $2\pi\hbar$ is Planck's constant.³²

Figures 4 (b) and (c) show **linear** fittings of 5 nm HfO₂ leakage current according to Eq. 2 in the low voltage range (1-2.5 V) and Eq. 3 in the high voltage range (2.5-4 V), respectively. The dotted lines are the experiment results and the red solid lines are the fittings. Other transport models do not provide such a good agreement. The inset images in Figs. 4 (b) and (c) are schematic energy-band diagrams showing conduction mechanisms of P-F emission and F-N tunneling. The fitting results indicate that under a lower E , most carriers get through the films via shallow traps, and when E is strong enough, the carriers can obtain enough energy and tunnel through the barrier.

In summary, a-IGZO TFTs enabled by an ultrathin 5 nm HfO₂ gate dielectric have been demonstrated to be capable of operating not only at 1 V but also even at half volt. Importantly, TFTs also exhibit other desirable properties including negligible hysteresis, a steep subthreshold slope, and high $I_{\text{on}}/I_{\text{off}}$ ratio. We also discovered that the 5 nm-thin HfO₂ layer showed excellent surface morphology and good dielectric properties. The breakdown voltage of the HfO₂ film is as high as 4.5 V and the electron transport mechanisms through the HfO₂ layer have been analyzed. The results indicate that the half-volt operation of the a-IGZO TFTs may have a great promise for future wearables or other low-power electronics.

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