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Design, Construction and Testing of a Modular Multilevel Converter with a Distributed Control Architecture

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Abstract

Many simplified modular multilevel converter prototypes have been developed over the past few years, typically in order to demonstrate high level control schemes. Many of these prototypes are based on conventional centralised control strategies and are therefore unable to address concerns regarding scalability and the limitations imposed by hardware delays when using distributed control strategies. This paper presents an overview of common control architectures along with the design, construction and initial findings from industrially representative control hardware.

1 Introduction

Multilevel converters have been applied in a number of high-voltage direct-current (HVDC) projects worldwide, especially in offshore wind applications [1-3], and while different topologies exist, such as the Cascaded Two-Level Converter (C2LC) [4], Alternate Arm Converter (AAC) [5] or Modular Multilevel Converter (MMC) [6], they often share similar constraints. As the market for voltage-source converters (VSCs) continues to grow [7], so will the need for knowledge of the design, application and control of these devices.

Many reduced-scale prototypes of VSCs in academia use a single, centralised station controller to manage system operation. This simplicity in design and construction allows for a research platform that is quick to develop and easy to adapt for follow-on researchers. However these hardware prototypes do not address the limitations placed on control by communications and computational hardware when up-scaled to a full-size converter [8].

This paper provides an introduction into the differences between centralised and distributed control, and the design, construction and initial testing of a reduced-scale prototype MMC with distributed control hardware. The system comprises 48 half-bridge (full-bridge capable) submodules, 12 partitioned (x4) System-on-Chip (SoC) based Distributed Control Units (DCUs), 1 partitioned (x3) Field Programmable Gate Array (FPGA) based phase controller unit (PCU) and 1 soft-core processor based Station/Central Control Unit (CCU). An industrially representative converter of this design will facilitate a comparison between hardware and simulation to assess the fidelity and suitability of power systems models.

2 Modular Multilevel Converter

An MMC is an efficient module-based multilevel AC/DC converter. A basic structure for a single-phase MMC is shown in Fig. 1a [9]. A converter leg/phase is split into 2 arms, each consisting of a number of submodules (SMs) and a reactor connected in series. A typical half-bridge SM is shown in Fig. 1b comprising two insulated-gate bipolar transistors (IGBTs) ($S1$, $S2$) with anti-parallel diodes ($D1$, $D2$) and a capacitor (C_{sm}) charged to a nominal voltage (V_{cap}). The arm voltages (V_{ua} , V_{la}) can be controlled by connecting or bypassing the SMs in each arm respectively. This is possible through control of the gate voltages applied to $S1$ and $S2$ as in Fig. 1c. By modulating the switching action at a chosen frequency, an AC voltage waveform can be approximated (V_a). This circuit can be replicated and connected in parallel across the DC link (V_{dc}) to create a three phase system. For further detail, including equivalent diagrams see [10, 11].

An MMC requires multiple loops of cascaded control to operate. The loops of interest in this research can be separated into power, current and voltage. The power loop uses vector control to calculate dq current references; these are compared against phase-locked loop measurements in the current loop to determine voltage set-points which are fed into the voltage loop. The voltage loop includes a number of controllers such as: Circulating Current Suppression Control (CCSC), Capacitor Balancing Control (CBC) and Nearest Level Control (NLC), which determine SM switching signals [12].

Fig. 1. Single-phase MMC (A) with basic half-bridge SM (B) and nominal switch signals (C) [9]

3 Centralised vs. Distributed Control

Improvements in control hardware and Insulated Gate Bipolar Transistor (IGBT) technology, has enabled the development of VSCs with hundreds of levels. As the number of levels rises the complexity of control increases therefore placing a greater requirement on hardware. For example, the INELFE link uses 401-level MMCs [13], requiring at least 2400 half-bridge SMs per converter. To control a system of this size with a single centralised controller would be challenging and creates a single point of failure. Due to this the converters designed by industry distribute the system operation across a number of controllers in order to reduce the hardware requirements of the station control.

The architectural differences between a centralised control structure and a distributed control structure for an MMC are clear, and while there is only one method of system management when using a centralised structure, there are many different methods when using a distributed structure. The following subchapters discuss these differences in detail.

3.1 Centralised Control Architecture

An overview diagram for a centralised structure can be seen in Fig. 2. For this architecture all control is managed by a single station controller/CCU which is optically or galvanically isolated from the SM power electronics (PE). The SMs may have a receiver circuit to decode switch signals and manage dead time, or this can also be controlled by the CCU. The SM will have a voltage-to-frequency converter (or similar) to return analogue measurements of submodule voltages to the CCU for digital conversion and control.

This architecture is made possible using a fast controller such as an FPGA and/or Digital Signal Processor (DSP) with a large number of analogue and digital I/O, but is still limited to controlling small numbers of SMs. Hardware examples for this method of control are discussed in [14-19].

Figure 2: Centralised Control Structure

Figure 3: Distributed Control Structure

3.2 Distributed Control Architecture

An overview diagram for a fully distributed control structure is presented in Fig. 3. For this architecture each SM is managed by a dedicated DCU, which transmits and receives optically isolated signals to and from an arm controller which in turn transmits and receives control signals to and from the CCU. In a ‘basic’ distribution method the SM FPGAs measure and convert capacitor voltages, control the dead-time and switching of the IGBTs and manage any local protection mechanisms. The arm controllers, or partitioned PCUs, manage capacitor balancing, and modulation, while the CCU limits circulating current and determines the arm voltages required to meet power requirements. This method of control splits the main I/O tasks for the CCU across the PCUs, reducing the centralised hardware requirements but still relies on high speed FPGAs or DSPs. Hardware prototypes using partially distributed control are discussed in [20-22].

Recent publications discuss delegating tasks such as capacitor balancing control to the DCUs, in order to further reduce the control requirements on arm controllers and the CCU. These methods allow for considerably improved scalability in design, but have so far only been tested on bespoke hardware prototypes [8, 23]. The MMC designed and constructed during this research has the potential to compare control methods in order to assess the implications of fully distributed control. The results presented in this paper are generated using the ‘basic’ method of distributed control applied to the hardware prototype for initial validation. But future work surrounds the more ‘complex’ distribution methodologies.

4 Hardware System

A reduced scale, hardware prototype of an MMC has been designed and constructed during this research. The system has a focus on distributed control and communications while maintaining industrially representative operation. The hardware system ratings are presented in Table 1.

4.1 Submodule Design

As described in Section 2 an MMC is made up of a number of SMs connected together. The design and operation of the SM is a critical part of the whole system. The chosen SM design, in standard Eurocard size is shown in Fig. 4.

The SMs are reconfigurable into half-bridge and full-bridge modes. Given the significantly reduced voltage ratings of this hardware, low on-resistance metal-oxide-semiconductor field-effect transistors (MOSFETs) are used instead of IGBTs to give representative voltage drops during operation. All incoming/outgoing signals are isolated using optocouplers or isolated gate-drivers. Reduced scale operation also leads to auxiliary power requirements for local circuitry (which would be harvested from the SM capacitor in full-scale systems [3]); this is supplied by either a dedicated 24 V unit or the DCU. Each SM has 4 isolated DC/DC regulators, 3 for the gate-drivers and 1 for the measurement electronics.

Each SM has three 10-bit ADCs to measure capacitor and switch voltages. A 10 Mbps serial-peripheral interface (SPI) is used by the DCU to control these devices. A SM capacitance of 3 mF was chosen based on the method in [11].

Description	Value
AC Voltage (MMC)	120 V (L-L, RMS)
DC Voltage (MMC)	± 100 V
Apparent Power (MMC)	1.8 kVA
Submodule Voltage	25 V
Submodule Capacitance	3 mF
Submodule Topology	HB/FB reconfigurable
Arm Inductance	10 mH
Number of Submodules (6N)	48
Number of DCU	12

Table 1: Nominal Operation Ratings

Figure 4: Submodule Implementation

4.2 General Configuration

The full MMC hardware prototype is shown in Fig. 5. The Eurocard size allows for simplified mounting within a 19-inch server rack. Absolute maximum system ratings are given in Table 2.

Description	Value
Rated AC Voltage (MMC)	260 V (L-L, RMS)
Rated DC Voltage (MMC)	± 220 V
Apparent Power (MMC)	6.6 kW
Submodule Voltage	57 V

Table 2: Absolute Maximum Ratings

Figure 5: MMC Experimental Test Rig

5 Simulation System

Models of varying fidelity are presented in literature. These are generally categorised into 8 distinct ‘types’. From Type-1 full-physics based models, through to Type-8 average power flow models [26, 27]. A Type-3 model, also known as a Traditional Detailed Model (TDM), uses two-state resistances to represent switches and diodes [28]. This method offers a quicker simulation time to a Type-2 full detailed model at the expense of loss of fidelity on switching action. A single phase Type-3 model has been developed in PSCAD/EMTDC using component parameters taken from the hardware system.

Phase-Shifted Pulse-Width Modulation (PS-PWM) is a non-typical modulation method for industrial scale MMCs however it offers a simple to understand and quick to implement control mechanism suitable for validating hardware. A 50 Hz sinusoidal reference voltage is compared against twelve 1950 Hz phase-shifted carriers, as described by [14], generating PWM signals for the SM switches.

6 Experimental Comparison

Two different modulation methods are presented: PS-PWM and NLC. In the case of PS-PWM, results from hardware are compared against results from the simulation model described in Chapter 5. In the case of NLC, results from hardware are compared against results from a mathematical model of NLC, following the method described in [29].

Figure 8: 13-level voltage outputs using PS-PWM control from the simulation (A) and in hardware (B) (30 V DC)

Figure 9: 13-level voltage outputs using NLC from the mathematical model (A) and in hardware (B) (100 V DC)

Figures 8a and 8b present output graphs from simulation and hardware respectively for PS-PWM control. The simulation has been set to plot a staircase waveform with an update frequency of 10 kHz, equal to the bandwidth of the internal voltage loop for the hardware system. UART channels from the PCU to the DCUs operate in parallel, but the DCUs are not synchronised; therefore delays caused by hardware nonlinearities, varied optical fibre lengths and switch dead-time causes SM changes to occur out of sequence. This switching action creates unwanted voltage transitions which can be seen on Figure 8b. Figures 9a and 9b present output graphs from the model and hardware respectively for NLC. Switching occurs when a level change is required or if SMs should be swapped for voltage balancing (CBC); the frequency of switching is typically much lower than with PWM methods. The hardware results closely match the simulation results for both modulation methods; however the delays, voltage overshoot and nonlinearities neglected in the simulation models are present and significant in hardware.

7 Conclusion

A comparison between control architectures presently used on MMC systems in academia and industry has been made along with a more detailed breakdown of the architecture used in a new, industrially representative, hardware prototype. The prototype behaviour closely matches that of simulation. Future research will make use of the prototype for model fidelity assessment and distributed control studies.

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