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Estimation of intrinsic and extrinsic capacitances of graphene self-switching diode using conformal mapping technique

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Abstract

Due to a very high carrier concentration and low band gap, graphene based self-switching diodes do not demonstrate a very high rectification ratio. Despite that, it takes the advantage of graphene's high carrier mobility and has been shown to work at very high microwave frequencies. However, the AC component of these devices is hidden in the very linear current-voltage characteristics. Here, we extract and quantitatively study the device capacitance that determines the device nonlinearity by implementing a conformal mapping technique. The estimated value of the

nonlinear component or curvature coefficient from DC results based on Shichman-Hodges model predicts the rectified output voltage, which is in good agreement with the experimental RF results.

1. Introduction

The unique band structure of graphene, where sp^2 -bonded carbon atoms are densely packed in a two-dimensional honeycomb structure [1], demonstrates a quasi-linear dispersion relation between energy and wave number so that charge carriers lose their effective mass and can be described by a massless Dirac equation [2]. As a result, graphene is a semi-metal with a finite minimum conductivity and zero bandgap as its valence and conduction bands are cone shaped and degenerate at the corners (known as K points) of the hexagonal Brillouin zone. This zero band gap makes it impossible to completely switch off graphene based devices limiting the on/off current ratio of graphene transistors [3]. Several approaches such as tailoring the graphene film in one dimension, i.e., narrow graphene nanoribbon [4–7], unzipping carbon nanotubes [8], reduction of graphene oxide [9], biasing bilayer graphene [10–12], applying strain to graphene [13, 14], irradiation of graphene with an ionized atom [15], and graphene growth on MgO [16] have been investigated to open up a sizable bandgap for the realization of such devices. The ultra-high mobility ($\sim 200,000 \text{ cm}^2/\text{V.s}$) [17], and high carrier velocity ($\sim 4.5 \times 10^7 \text{ cm/s}$) [18], in addition to the electric-field induced ambipolar carrier conduction enables graphene as a promising material to design and develop novel nanorectifiers called self-switching devices (SSD) [19] that do not necessarily require any sizable bandgap and/or multi-layer architecture. Moreover, the single-layered architecture of the SSD makes graphene an ideal candidate for use as the active layer. The graphene SSD can be considered as a graphene nanochannel based double side-gated transistor that is connected as a diode by short circuiting the drain and both gates together [20]. Such a strategic placement of lateral side gates electrostatically modulates the carrier density in the

channel inducing a novel rectifying behavior in contrast to the conventional multilayered devices that require p - n junction or Schottky barriers. The active part of SSD includes two L-shaped insulating grooves which can be fabricated using nanolithography in only a single step. SSDs have been demonstrated in a wide variety of semiconductor materials such as two-dimensional electron gases (2DEGs) in InGaAs [19, 21–23], GaAs [24], InAs [25], AlGaAs [26], silicon-on-insulator [27], monolayer molybdenum disulphide [28], and both organic [29] and metal-oxide thin films [30, 31]. The room temperature detection of THz signals [24, 32] and numerical simulations [33, 34] showing SSD’s capability as a THz emitter may lead to the development of a compact, cost-effective THz system. Very recently, SSDs have been realized in epitaxial graphene on Silicon Carbide as zero-bias microwave detectors up to the frequency of 67 GHz [35, 36] supporting theoretical studies based on the extended Huckel (EH) method and nonequilibrium Green’s function (NEGF) formalism [37, 38]. Graphene SSDs have demonstrated almost linear current-voltage (I - V) characteristics due to very high carrier concentration and zero bandgap. However, AC component hidden in the device I - V characteristic can be predicted by extracting the nonlinearity or curvature coefficient (γ) from the DC response. Here, we extract and quantitatively study device capacitances that cause the nonlinearity using a conformal mapping technique. The values of the nonlinear component or curvature coefficient that are estimated using the Shichman-Hodges model [39], predict the rectified DC output and are in good agreement with the experimental results.

2. Methods

The standard mechanical exfoliation technique is used to deposit single layer graphene onto a thermally grown 290 nm thick silicon oxide (SiO_2) on a silicon substrate. The charge carrier concentration in the SSD channel is controlled by applying a back-gate voltage (V_{BG}) to highly

doped *p*-type silicon substrate which tunes the Fermi energy of the device. The optical contrast method is utilized to identify the graphene flakes on the substrate [40]. The hall bar geometry (used to characterize the graphene itself) and SSD structure are patterned by employing electron beam lithography (EBL), utilizing polymethyl methacrylate (PMMA) as the e-beam resist, and low power oxygen-plasma etching. The contacts are defined with e-beam lithography and Cr/Au (3 nm/40 nm) is deposited with an e-beam evaporator on graphene in order to form ohmic contacts, followed by the lift-off process performed in hot acetone. The neutrality point or Dirac point (V_{DP}) of the fabricated Hall bar structure is observed at a back-gate voltage of -4 V indicating little extrinsic doping, approximately $2.9 \times 10^{11} \text{ cm}^{-2}$. A field-effect mobility of 1572 and 1810 $\text{cm}^2/\text{V.s}$ is estimated from the slopes of the conductivity as a function of V_{BG} for holes and electrons, respectively, which is typical on untreated SiO_2 substrates [41]. The scanning electron microscopic (SEM) image of a typical SSD fabricated from monolayer graphene is shown in figure 1(a). The channel width and length of the fabricated device are 90 and 880 nm, respectively. The schematic of a diode in the inset of figure 1(a) demonstrates the preferred direction of current flow considering electrons as majority charge carriers in the SSD channel. The two terminals of the device are isolated by wider trenches than that of along the channel boundaries in order to reduce the capacitive coupling which in turn improves the device cut-off frequency, hence the operating speed [42]. The trenches along the channel not only induce an asymmetry in the channel but also insulate the device from the side electrodes [19].

Figure 1. (a) Scanning electron micrograph of a typical SSD fabricated from monolayer graphene on SiO₂. The channel width and length of the device are 90 nm and 880 nm, respectively. Inset shows the schematic of the diode depicting preferred direction of current flow when electrons are the majority carriers. (b) The room temperature current-voltage characteristic of the SSD at back-gate voltage of 0 V fits well to the quadratic fitting. The extracted nonlinearity from DC I - V characteristics which translates to curvature coefficient and, hence, voltage responsivity is given in the inset.

3. Results and discussion

The operation of an SSD is based on the asymmetric nanochannel which utilizes the intriguing properties of a graphene nanochannel with a side-gate scheme producing a nonlinear current-voltage (I - V) characteristic [20]. The broken symmetry of the device is ensured by extending the trenches to the device boundary which allows current to only flow through the channel. Figures 2(a) and (d) are the atomic force micrographs of a graphene SSD and show the bias connections when the electrons and holes are the majority carriers in the channel, respectively. When electrons are the majority carriers and there is a negative voltage ($V < 0$ V), the negative charges around the channel repels the electrons out of the channel, thus resulting in the device becoming more resistive

as depicted in figure 2(b). However, a positive voltage ($V > 0$ V) increases the positive charges around the trenches, which attracts electrons into the channel, making it more open and conductive as shown in figure 2(c). Therefore, the device favours current flow only in one direction and as a result nonlinear I - V characteristic similar to that of a conventional diode is obtained [19]. In addition, this device does not require any p - n junction or Schottky barrier along the direction of current conduction.

Figure 2. (a) The atomic-force micrograph of a typical SSD fabricated from graphene. (a) and (d) shows the bias connections at the two terminals of the device for electrons and holes transport regime, respectively. The effective channel width decreases (b) and (e) for the negative bias $V < 0$ V. However, a positive bias $V > 0$ V (c) and (f) increases the channel width, which in turn gives rise to diode-like characteristic as shown in Figure 1b.

The above described mechanism, which leads to a preferred direction of current flow, is referred to as the self-switching effect of the device. Correspondingly for positive charge carriers (holes) [27], opposite voltages have to be applied across the device to obtain a similar self-switching effect as illustrated in figures 2(d)-(f). This operation does not require any ballistic or quasi-ballistic transport of charge carriers, since the device dimensions are an order of magnitude larger than the mean-free path length. Hence, SSDs differ from the recently reported graphene based nanorectifiers called ballistic rectifiers [43–46].

The room temperature I - V characteristic of a typical single SSD fabricated from monolayer graphene is shown in figure 1(b). The measurements are performed at the back-gate voltage of 0 V that is to the right of the neutrality point (i.e. $V_{DP} = -4$ V) where electrons are the majority carriers. Hence, the field-effect induced electrons movement inside the channel has played an important role in obtaining the nonlinear I - V characteristic as shown in the inset of figure 1(b). The operation of a graphene SSD can be analysed as a standard metal-oxide-semiconductor field-effect transistor (MOSFET) but connecting the drain and the gate together using Shichman-Hodges model [39], the current I can be given as

$$I = zWJ = zWqnv_d = zWQv_d \quad (1)$$

here z is thickness of the channel, W is width of the channel, J is current density, q is carrier charge, and n is the carrier density. $Q = -C(V_G - V_T - V(y))$ is the charge induced on side walls of graphene channel, where C represents the gate induced capacitance per unit area, V_G is the side-gate voltage, V_T is the threshold voltage and $V(y)$ represents the potential in the channel as a

function of y along the channel. The drift velocity in terms of mobility (μ) can be evaluated as

$$v_d = -\mu \frac{dV(y)}{dy}. \text{ Thus, } I \text{ becomes}$$

$$I = \mu z C (V_G - V_T - V(y)) \frac{dV(y)}{dy} \quad (2)$$

The continuity implies $\int Idy = IL$, where L is the channel length. Hence, by integrating between 0 and the drain voltage V_D on the $V(y)$ side results in equation (3).

$$I = \frac{\mu z C}{L} \left((V_G - V_T) V_D - \frac{V_D^2}{2} \right) \quad (3)$$

In the case of monolayer graphene, in the intrinsically doped regime, V_T will be 0 since there is no bandgap. For the SSD, $V_G = V_D = V$ and the capacitance per unit area $C = C_{SSD}$ will be mainly due to the horizontal trenches along the channel. Thus, equation (3) simplifies to a square-law:

$$I = \frac{\mu z C_{SSD}}{L} \frac{V^2}{2} = KV^2 \quad (4)$$

Here, $K = \mu z C_{SSD} / L$ is a fitting parameter. C_{SSD} can be extracted from the measured I - V characteristic by fitting to equation (4), as the mobility, thickness and length of the device are the known parameters.

The operation of SSD relies on the field effect of bias induced charges around the nanochannel. Changes in the applied voltage move charges both within the channel and in both sides of trenches which isolate the two terminals of the device. As a result, the device exhibits the intrinsic (C_H) and extrinsic (C_V) capacitances caused by the horizontal and vertical trenches

Figure 3. (a) Possible equivalent circuit of the SSD illustrating the intrinsic C'_H and extrinsic capacitances C'_V due to the horizontal and vertical trenches, respectively. (b) Simplified equivalent circuit suggests that both the capacitances are in parallel to each other and SSD channel resistance.

around the channel, respectively, as shown in figure 3(a). Simplified equivalent circuit in figure 3(b) illustrates that the total capacitance C_{SSD} of an SSD can be obtained by evaluating C_H and C_V . The extrinsic capacitances, also referred to as parasitic capacitances, do not contribute to the nonlinear property of the I - V characteristics [47], hence should be minimized by making wide trenches as in figure 1(a). Because of the planar geometry of the device structure, it is expected that extrinsic capacitances are smaller to that of a conventional vertical diode of same size [19]. In contrast, the intrinsic capacitances of SSD are mainly due to the horizontal trenches and play a key role in the device nonlinearity. Fitting the measured results in figure 1(b) to equation (4) yields $C_{SSD} = 16.17 \times 10^{-17}$ F for a typical graphene channel thickness of about 0.335 nm.

The technique of conformal mapping [48] is employed to theoretically evaluate both the capacitances considering in-plane geometry of trenches in perfectly conducting sheet of graphene.

Figure 4(a) shows a schematic of in-plane geometry of a trench, which consists of two conducting infinitely long coplanar graphene strips having a width of s and separated by a trench of width d . Atomically thin graphene strips can be considered as embedded in the dielectric medium with a relative dielectric constant $\epsilon_r = (3.9+1)/2$, where 3.9 and 1 are the dielectric constants of SiO₂ and air, respectively, as depicted in figure 4(b). For symmetry, the upper half-plane t in figure 4(c) is transformed conformally onto a rectangle by the elliptical integral as shown in figure 4(d) implementing Schwarz-Christoffel mapping [49]. The capacitance of two neighbouring conducting graphene strips at both sides of one vertical trench can be calculated

Figure 4. (a) Schematic illustration of a trench in a graphene sheet, used to calculate the extrinsic capacitance. (b) In order to calculate the extrinsic capacitance, atomically thin graphene strips (thickness of about 0.335 nm) are considered as embedded in a dielectric medium with relative dielectric constant ϵ_r . (c) The upper half-plane with graphene sheet as coplanar strips. (d) Equivalent rectangular geometry of (c) after applying the conformal mapping. (e) Schematic illustration of horizontal trenches of SSD used for the calculation of intrinsic capacitances. The structure can be viewed as a coplanar waveguide.

analytically as $C'_V = \varepsilon_0 \varepsilon_r K'(k)/K(k)$. For $t = 1$, $K(k)$ and $K'(k) = K(k')$ are the complete integrals of modulus $k = d/(2s + d)$ and complementary modulus $k' = \sqrt{1 - k^2}$, respectively. The logarithmic approximation $k \approx 4 \exp(-\pi K'/K)$ for wide strips of graphene sheets ($s \gg d$) yields C'_V as [50]:

$$C'_V = \varepsilon_0 \varepsilon_r \frac{K'(k)}{K(k)} = \varepsilon_0 \varepsilon_r \frac{1}{\pi} \ln \frac{4}{k} \approx \varepsilon_0 \varepsilon_r \frac{1}{\pi} \ln \left(8 \frac{s}{d} \right) \quad (5)$$

In the most relevant range $10^{-2} < d/s < 1$, the expression for the extrinsic capacitance in equation (5) can be further simplified by an approximation of zeroth order and the total capacitance per unit length amounts to $\sim 2\varepsilon_0 \varepsilon_r$. However, equation (5) needs to be evaluated to obtain a more accurate value. The overall extrinsic capacitance $C_V = 2C'_V$ of a single device in figure 3(a) is due to two vertical trenches connected in parallel.

On the other hand, intrinsic capacitance of the SSD is mainly due to the horizontal trenches. Figure 4(e) shows the cross-sectional view of a graphene SSD channel of width W separated from two side gates of s' width at both the sides by two horizontal trenches of width d' . Considering only one quarter of the plane due to symmetry, the total capacitance of whole structure can be evaluated from the resultant pair of graphene strips in the upper half-plane as [48]:

$$C_H = 4\varepsilon_0 \varepsilon_r \frac{K(k_1)}{K'(k_1)} \quad (6)$$

where, $k_1 = \frac{a}{b} \sqrt{\frac{c^2 - b^2}{c^2 - a^2}}$ is given in terms of $a = W/2$, $b = (W/2 + d')$ and $c = (W/2 + d' + s')$ as shown

in figure 4 (e). The intrinsic capacitance (per unit length) can be further simplified to $\sim 4\varepsilon_0 \varepsilon_r$ for the

typical values of W/d' in the range of 1-10, where $K/K' \approx 1$. For the device shown in figure 1(a), equations (5) and (6) yielded $C_V = 2.76 \times 10^{-17}$ F and $C_H = 10.6 \times 10^{-17}$ F. The measured value of SSD capacitance, i.e. 16.17×10^{-17} F, is well in accordance with the theoretically calculated value of 13.36×10^{-17} F and is an order of magnitude lower than that of earlier reported values for Si SSDs (250×10^{-17} F) [51].

Being a nonlinear device, the graphene SSD can be used to rectify an AC signal analogous to conventional multilayered rectifiers which, however, require either a p - n junction or a Schottky barrier along the direction of electrical current. The built-in electric field in these latter devices requires an applied bias potential to overcome the threshold voltage in order to ensure a significant current flow. On the other hand, the graphene SSD has no intrinsic turn-on or threshold voltage as shown in figure 1(b). This is due to the broken symmetry of the device inducing zero-threshold non-linear operation. The I - V characteristic of the graphene SSD is analyzed as a low level detector analogous to a diode [50]. In a square-law operation, the nonlinear component called zero-bias curvature coefficient $\gamma = \left[(d^2 I / dV^2) / (dI / dV) \right]_{V=0}$ can predict the rectified DC output from the device [53]. As a microwave/RF detector, SSD is typically being driven by a source with an impedance (R_s) of 50 Ω , hence, the voltage responsivity, also known as detection sensitivity, can be estimated as $\beta_V = 2 R_s \gamma$ [35]. The measured results in figure 1(b) yield a $\gamma = 0.686$ V⁻¹, accordingly $\beta_V = 68.6$ V/W, and these values are well in accordance with previously reported values for similar devices [36]. The intrinsic cut-off frequency ($f = 1/2\pi RC$) of 0.16 THz is estimated for the fabricated graphene SSD from the zero-bias resistance (36 k Ω) and extrinsic capacitance (2.76×10^{-17} F), that can be improved further by employing wider vertical trenches which in turn reduces the extrinsic capacitance.

Figure 5. (a) The microscopic image of 22 SSDs connected in parallel fabricated from CVD-grown graphene. (b) The atomic-force micrograph of two SSDs connected in parallel shows the lithographic channel width and length of about 180 nm and 1 μm. The schematic of a diode illustrates the direction of current conduction in the hole transport regime. (c) Room temperature I - V characteristic of the array of 22 SSDs connected in parallel fabricated from CVD-grown monolayer graphene on SiO_2 at different back-gate voltages ranging from -30 to 30 V. The inset shows the calculated nonlinear output and fits well to the quadratic fitting (dashed line) as described by equation (4). (d) The rectified DC output in RF measurements (only up to 2 MHz due to Si substrate) is in good agreement with the extracted voltage responsivity from nonlinear component of I - V characteristics in (c). The inset in (d) shows a typical electrical contact (in G-S-G Configuration) used for RF measurements.

The planar geometry of an SSD allows the realization of simple circuits without interconnection layers minimizing the parasitic elements. Figure 5(a) demonstrates an optical microscopic image

of a linear array of 22 SSDs connected in parallel fabricated by simply placing individual SSDs next to each other. The fabrication of an SSD array not only reduces the overall impedance of the device but also increases charge carriers responsible for the current conduction, thus reducing the thermal noise and averaging out the impact of $1/f$ or flicker noise [24, 54]. The large area monolayer graphene film used in these experiments is grown using chemical vapor deposition (CVD) technique on copper foil and later transferred using wet-etching to a thermally grown 300 nm thick SiO_2 on a highly p -doped Si substrate. In order to characterize the rectification properties of the SSD, RF contacts (in G-S-G configuration) are patterned onto CVD-grown graphene using standard photo-lithography and oxygen-plasma etching. The fabricated devices exhibit p -type doping with neutrality point far away to the right of 0 V (i.e. $V_{DP} \approx 80$ V). The field-effect mobility of about $644 \text{ cm}^2/\text{V.s}$ is estimated for these devices. Adsorbents/residues left behind by photo-lithography fabrication processes are the main reason for having such low mobility [55]. An atomic-force micrograph of two SSDs connected in parallel is shown in figure 5(b). The lithographic channel width and length of a single SSD are 180 nm and 1 μm , respectively. The room temperature I - V characteristics of the SSD array at different back-gate voltages varied from -30 to 30 V in figure 5(c) exhibit a very small quadratic nonlinearity attributed to the wide channel of individual SSDs as shown in the inset. However, device capacitance C_{SSD} of 5.61×10^{-15} F extracted from the nonlinear component of measured results is on the same order of magnitude obtained from quantitative analysis using conformal mapping technique. This translates into a similar curvature coefficient in the range of 0.064 to **0.089 V^{-1}** for different back-gate voltages from 30 to -30 V, respectively. Accordingly, estimated voltage responsivity up to 8.9 V/W matches well to that of RF measurements performed only up to 2 MHz (due to Si substrate) in figure 5(d).

4. Conclusion

In summary, we have discussed and analyzed nonlinear characteristics of graphene self-switching diode using Shichman-Hodges model. The extracted value of device capacitances from measured I - V characteristics that determines the device nonlinearity or curvature coefficient are in good agreement with the values obtained quantitatively implementing conformal mapping technique. In addition, the predicted curvature coefficient or nonlinear component from a graphene SSD which translates directly into voltage responsivity, is in accordance with the measured RF results. Considering Fermi velocity of charge carriers in graphene ($\sim 10^6$ m/s), an intrinsic cut-off frequency of up to a terahertz can easily be achieved by fabricating SSDs having optimized channel dimensions from graphene transferred to a suitable substrate such as boron nitride (BN), quartz etc. to avoid back-gate induced capacitive problems.

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