Mismatch Compensation Technique for Inverter-Based CMOS Circuits

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Mismatch Compensation Technique for Inverter-Based CMOS Circuits

Przemyslaw Mroszczyk
Advanced Processor Technologies Group
School of Computer Science, The University of Manchester, Manchester, UK

Vasilis F. Pavlidis
Advanced Processor Technologies Group
School of Computer Science, The University of Manchester, Manchester, UK

***Abstract*—Inverter-based CMOS circuits are often considered in the front-end modules for optical and wireline communication, A-D conversion, and analogue computation. Due to parameter variability (mismatch), the performance of such circuits is usually degraded. This paper presents a mismatch compensation technique employing a set of redundant switches to trim the switching threshold of inverter-based CMOS circuits. Over 10× better parameter matching is observed at no additional energy cost or significant gate area increase, compared to "traditional" geometry scaling. The efficiency of the mismatch compensation is investigated across a broad design space considering the number and size of the switches, and the size of the inverter, using models from a 65 nm CMOS technology. The case study of a comparator circuit is further investigated in terms of the reliability, energy, and area, and compared against the geometry scaling approach.**

Keywords—parameter variability; mismatch; trimming; CMOS inverter; comparator

I. INTRODUCTION

A CMOS inverter is perhaps the simplest structure commonly used in integrated circuit design. In addition to digital systems, inverters are often present at the heart of many functional blocks, such as high speed amplifiers, comparators, delay lines, and are also used in analogue computation and neuromorphic circuits [1]-[5]. Due to the very simple topology of this two transistor push-pull amplifier, the area and energy requirements of an inverter are usually minimal with respect to the high gain bandwidth and speed of an inverter-based circuit. Therefore, a CMOS inverter is frequently considered the most efficient circuit in a given technology [6].

An inherent shortcoming of a CMOS process is a certain level of random variability of the circuit parameters known as manufacturing mismatch. As a result, the key parameters of an inverter such as gain, propagation delay, and switching threshold cannot be precisely determined at the design stage. This uncertainty often favors "tried-and-tested" solutions using less efficient and more complex circuits than an inverter, significantly trading area, energy efficiency, and speed for reliability [7].

The method most commonly used to mitigate mismatch is geometry scaling. This approach is based on the fact that the variability of the physical and electrical parameters in CMOS technologies reduces as the device area increases [8]. However, parameter matching improves only with the square root of the device area, and the required size (and gate capacitance) of an inverter, resilient to process variability, is prohibitively large. Therefore, applications of these circuits are limited to high-speed front-end amplifiers in optical and radio frequency (RF) transceivers, where large devices are typically used to meet gain bandwidth and high driving strength requirements [1].

One of the most area efficient approaches aiming at random offset voltage cancellation, resulting from parameter mismatch, employs auto-zero compensation. However, this technique is limited to circuits allowing discrete time operation [3], [4]. The majority of applications, where the inherent area and power efficiency of an inverter is of a great advantage, usually require continuous time circuits.

Another technique used to improve parameter matching, applicable both to the continuous and discreet time circuits, employs trimming. In this approach, a set of redundant devices (e.g. transistors or resistors) is selectively connected or disconnected from the circuit, "trimming" its operation to counteract mismatch. Despite the proven efficiency of this technique in mismatch mitigation, circuit benchmarking and search for the optimum solution across a large space of possible circuit configurations is required. Due to the high complexity, the trimming processes are usually conducted externally increasing the implementation cost and limiting the flexibility of the designed system. Therefore, trimming is usually considered in applications where energy efficiency and precision are paramount [9], [10].

Recognizing the advantages of the trimming technique, this paper presents the application of trimming for mismatch compensation in inverter-based circuits. Rather than enlarging transistors to reduce the variability of the gain, propagation delay, and switching threshold, a set of redundant, small size MOS switches is used to "balance" the strengths of the pull-up and pull-down networks, thereby counteracting the effects of the mismatch. Addressing the aforementioned challenges, the proposed trimming technique autonomously finds the best circuit configuration while requiring only a shift register. The approach offers superior mismatch compensation compared to "traditional" geometry scaling. The paper explores the effect of the number and size of the additional drivers on mismatch compensation in the inverters with different transistor widths.

The paper consists of five sections. The proposed trimming technique is presented in Section II. The related simulation results are discussed in Section III. The example comparator

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circuit is described in Section IV. Conclusions are provided in Section V.

II. INVERTER TRIMMING

This section presents the proposed trimming technique, the circuit implementation, and a dedicated test circuit used in a mixed-signal simulation environment.

A. Technique

The schematic diagram of the inverter with the circuit allowing switching threshold adjustment is illustrated in Fig. 1. The switching threshold V_{ST} is defined here as the crossover point on the DC transfer characteristic of an inverter where the input and output voltages are equal, also known as the point of the highest inverter sensitivity. The circuit consists of an inverter comprising transistors M_N and M_P and a set of additional drivers (M_{N1}-M_{N8} and M_{P1}-M_{P8}) with individual switches (M_{SN1}-M_{SN8} and M_{SP1}-M_{SP8}). These additional transistors are selectively used to "balance" the driving strength of the M_N and M_P networks for a given reference voltage V_{REF}. The trimming procedure aims at finding a configuration of switches ensuring that the point of the highest sensitivity occurs for a given input bias V_{REF}, such that $V_{ST} = V_{REF}$. The additional drivers are set to the minimum size while their strength is controlled through geometry of the switches. This choice enables keeping the input capacitance of the inverter to the minimum.

The transfer characteristic of the circuit is shown in Fig. 2. Note that the input voltage is constant (V_{REF}) while the output voltage changes as a result of altering the logic states of the signals controlling the switches. For all the signals set to logic "1" (defined as CODE = 0), the n-MOS switches are in the ON state, the p-MOS switches are in the OFF state. With this configuration, the driving strength of the M_N network is the highest, the driving strength of the M_P network is the lowest, and the output voltage reaches the minimum value V_{LOW}. By turning signals S_{N1}-S_{N8} successively to logic "0", the corresponding n-MOS drivers switch off, gradually decreasing the strength of the M_N network increasing the switching threshold V_{ST} of the inverter. The encoding scheme showing the relation between the codes and the configurations of the switches [S_{N1} … S_{N8}, S_{P1}, … S_{P8}], is listed in Table I. Note that this encoding scheme ensures a monotonic shift of the V_{ST}, despite the parameter mismatch, while the consecutive codes are generated and stored in a shift register, which significantly simplifies the circuit realization.

B. Circuit implementation

The schematic diagram of the trimming circuit is shown in Fig. 3, and the waveforms are depicted in Fig. 4. The circuit consists of an amplifier with 4 cascaded inverters and a 16-bit shift register used for code generation. Prior to trimming, all the bits are set to "1", equivalent to the first configuration, i.e. CODE = 0. The consecutive codes are generated on each rising edge of the CLK signal and the output voltage (see Fig. 2) of the first inverter in the amplifier increases. Once this voltage crosses the switching threshold of the second inverter, the output states of the remaining inverters change accordingly. As

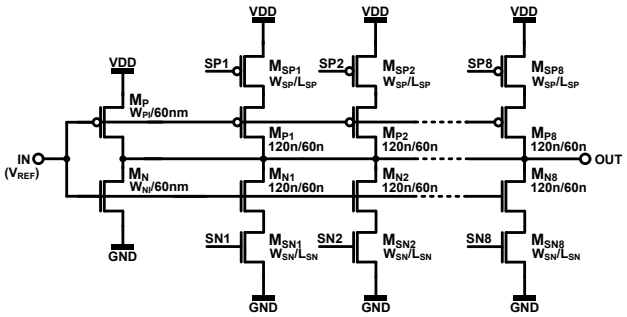

Fig. 1. The schematic diagram of an inverter with 8 trimming stages.

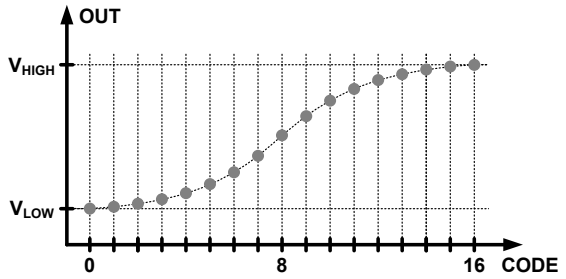

Fig. 2. The output voltage of the inverter in response to the monotonic sweep of the trimming codes.

TABLE I. ENCODING SCHEME OF THE CONFIGURATION SWITCHES

CODE	Vector [S_{N1} … S_{N8}, S_{P1}, … S_{P8}]
0	[11111111 11111111]
1	[01111111 11111111]
2	[00111111 11111111]
8	[00000000 11111111]
15	[00000000 00000001]
16	[00000000 00000000]

a result, the output of the amplifier will transition from the high to the low logic state, disabling the clock input of the D-type flip flops and, hence, locking the current code. If V_{REF} is beyond the trimming range, the circuit locks on the first or on the last code always minimizing the difference between V_{REF} and the actual value of V_{ST}. Note that the trimming is applied only to the first inverter stage. This feature has practically negligible impact on the trimming efficiency since the

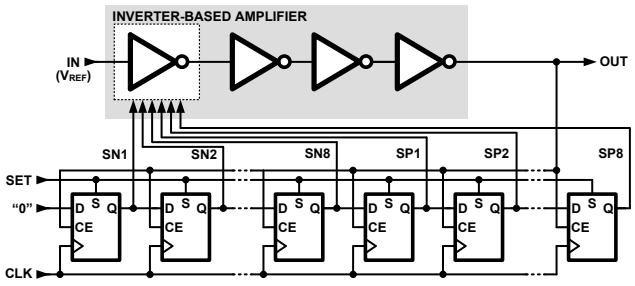

Fig. 3. Schematic diagram of the trimming circuit with amplifier.

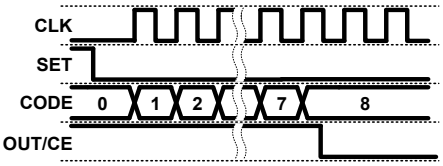

Fig. 4. Signal waveforms of the trimming process.

amplitude of the signal quickly increases far beyond the variability of the switching threshold of the inverters in the chain.

C. Test circuit

The circuit used in the simulations is depicted in Fig. 5. The inverter-based amplifier is implemented in a 65 nm CMOS technology with layout-estimated parasitics. The configuration of the switches is determined by the digital controller based on the state of the amplifier output (MODE 0). Once the trimming is complete, the analogue multiplexer and 16-bit rail-to-rail DAC are used in the evaluation of the switching threshold V_{ST} employing the successive approximation method (MODE 1). Note that the multiplexer and DAC are used for the quick V_{ST} estimation and are part of the testbench, thus Verilog-AMS models are preferred to shorten the simulation time. In MODE 2, the amplifier is used for performance tests (see Section IV).

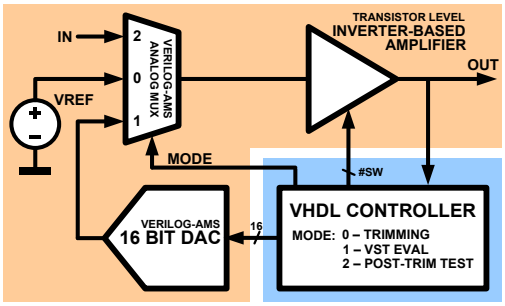

Fig. 5. The block diagram of the test circuit.

III. Simulation Results

This section presents the Monte Carlo simulation results of the V_{ST} variability of the inverter-based amplifier designed for $V_{ST} = V_{DD}/2 = 600$ mV. The reference values of the circuit parameters are listed in Table II. The trimming sequence and the V_{ST} are simulated assuming parameter mismatch at nominal operating conditions (TT process corner, $V_{DD} = 1.2$ V, T = 25°C). Note that, the systematic shift of the V_{ST} in other process, voltage, and temperature (PVT) corners can be compensated for by the circuit as long as a sufficiently large trimming range is ensured.

The trimming efficiency in terms of the size of the input stage transistors M_N and M_P for different number of trimming stages is shown in Fig. 6. The trimming efficiency is defined as the ratio $\sigma_{VST\text{-}G}/\sigma_{VST\text{-}T}$. The $\sigma_{VST\text{-}T}$ is the standard deviation of the V_{ST} of the amplifier with trimming (Fig. 3). The $\sigma_{VST\text{-}G}$ is the standard deviation of the V_{ST} of the same circuit without trimming stages but with the geometry (width) of the M_P (M_N) enlarged accordingly to ensure the same total gate area of the input stage as in the circuit with trimming. Note that the maximum trimming efficiency occurs only for a specific size of the input stage transistors. When W_P (W_N) is small, the effect of the additional drivers on M_P (M_N) is higher, the intervals between the neighboring codes expand (the trimming granularity increases), and the trimming precision degrades increasing $\sigma_{VST\text{-}T}$ which reduces the ratio $\sigma_{VST\text{-}G}/\sigma_{VST\text{-}T}$ (see the left hand side slopes of the traces in Fig. 6). When W_P (W_N) is larger, the impact of the additional drivers on M_P (M_N) becomes less significant and $\sigma_{VST\text{-}T}$ converges to $\sigma_{VST\text{-}G}$ (see the right hand side slopes of the traces in Fig. 6).

TABLE II. Reference Values of the Circuit Parameters

Parameter	Value
W_P/W_N	3µm/1µm
W_{SP}/L_{SP}	120nm/200nm
W_{SN}/L_{SN}	120nm/2µm
V_{REF}/V_{DD}	600mV/1.2V

The simulation results of a circuit with a fixed number of 8 trimming stages and different driving strengths are presented in Fig. 7. Note that the efficiency trace "shrinks" or "expands" along the W_P (W_N) axis as the strength of the trimming stages changes. Thus, the maximum efficiency occurs for a specific ratio of the W_P (W_N) strength and the strength of the trimming stages and, hence, can be decided by adjusting this ratio at the design stage, e.g. by appropriate sizing of the switches.

The absolute values of the standard deviation ($\sigma_{VST\text{-}T}$) and the mean value ($\mu_{VST\text{-}T}$) in terms of V_{REF} in the range 580 mV - 620 mV are shown in Fig. 8 and 9 respectively. Note that increasing the number of trimming stages the trimming range also extends. While an amplifier with 6 trimming stages allows

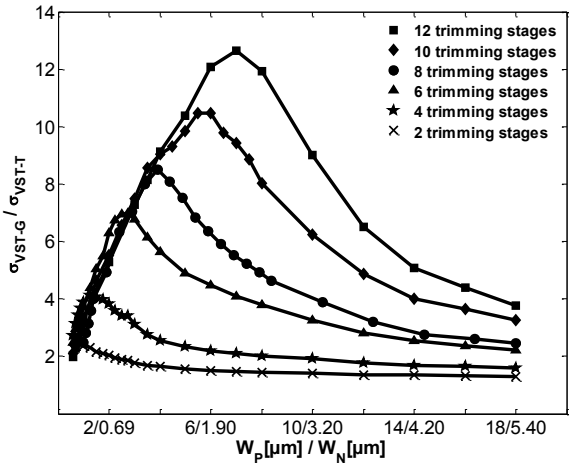

Fig. 6. Trimming efficiency in terms of the size of the input stage transistors M_P and M_N for different number of trimming stages.

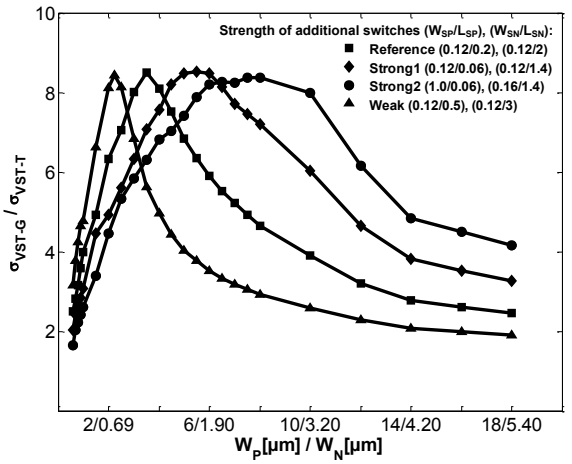

Fig. 7. Trimming efficiency in terms of the size of the input stage transistors M_P and M_N for different sizes of the switches in the input stage amplifier.

$\sigma_{VST-T} \approx 750$ µV only for $V_{REF} = 600$ mV, the same amplifier with 12 stages can be trimmed in the range of V_{REF} +/- 10 mV.

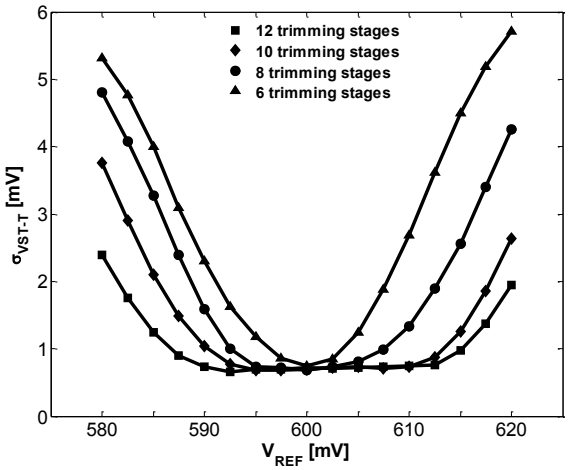

Fig. 8. Standard deviation of the V_{ST} after trimming in terms of the reference V_{REF} for different number of switches of the input stage amplifier.

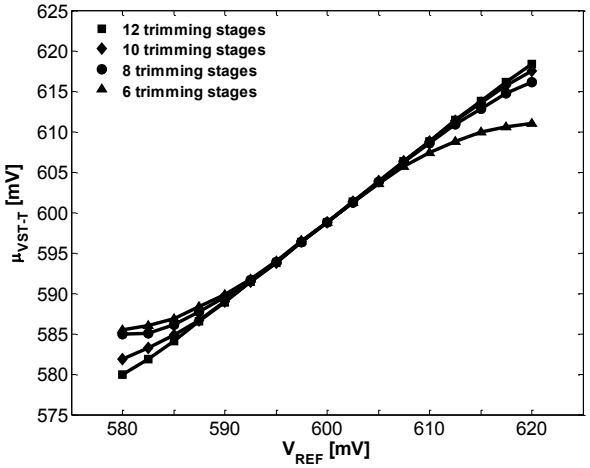

Fig. 9. Mean value of the V_{ST} after trimming in terms of the reference V_{REF} for different number of switches of the input stage amplifier.

IV. INVERTER-BASED COMPARATOR

This section presents an application of the inverter-based amplifier (Fig. 3) as a high speed comparator. The test circuit used in the simulations is shown in Fig. 10. It consists of the inverter-based amplifier with 8 trimming stages with reference circuit parameters from Table II, the pseudo-random bit stream generator (PRBS), and the bit error rate test module (BER). The PRBS generates a bit sequence at 1 Gb/s speed around the reference V_{REF} +/-ΔV_{IN}. The BER test module compares the input and output signals of the comparator on bit-to-bit bases and counts the number of encountered errors. The output of the comparator is recognized as logic "0" or "1" when the sampled output voltage (100 ps prior to the next bit) is below 300 mV or over 900 mV, respectively, otherwise an error is recorded. The bit error rate for a given input swing ΔV_{IN} is estimated based on 100 Monte Carlo simulation runs including trimming and test (MODE 2) with a random sequence of 1000 bits. The BER in terms of ΔV_{IN} is shown in Fig. 11. For comparison, BER of three comparators with no trimming and increased size of the

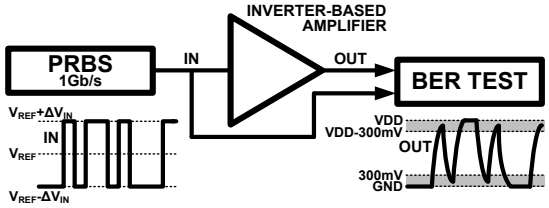

Fig. 10. Test circuit used in the simulation of the inverter-based comparator.

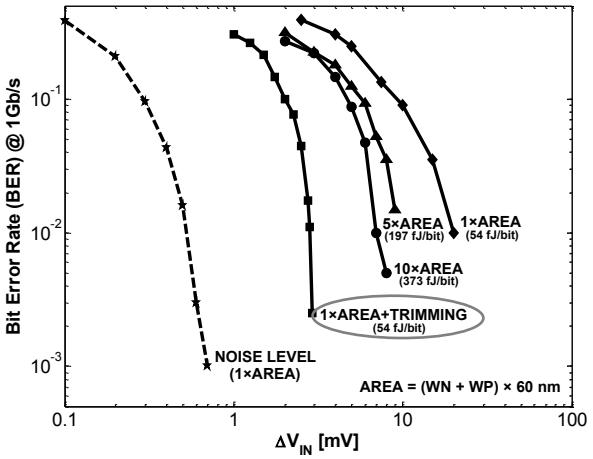

Fig. 11. Bit error rate vs. ΔV_{IN} voltage of the inverter-based comparator illustrating performance under mismatch, noise and geometry scaling.

input stage transistors by 1×, 5×, and 10× the reference area from Table II are provided. Noise induced BER is evaluated in transient noise simulations of the same test circuit for 20 GHz bandwidth assuming no variability.

The proposed trimming technique achieves about 10× lower BER than the same circuit without trimming, at no additional energy cost. Moreover, the performance of the proposed circuit cannot be achieved through geometry scaling without a significant increase in the area and power of the comparator. Note that 10× the area increase in the scaling approach entails 7× higher power consumption while reducing BER only by factor of 3. Further BER reduction is possible by using more trimming stages, however, limited by noise when ΔV_{IN} < 1mV. The energy efficiency of the circuit can be improved by reducing the size of the input stage transistors and by implementing other low power techniques (e.g. supply voltage reduction) [3]. In addition, inverter-based comparators exhibit very small kickback [11] due to a low voltage gain of the first stage. Also, the information about the switching threshold is stored in the shift register and the reference can be powered off after the trimming, which is beneficial to some applications with low power requirements such as Flash ADCs.

V. CONCLUSIONS

In this paper, a novel approach to mitigate mismatch in inverter-based CMOS circuits is presented. The proposed technique achieves significantly better parameter matching at no additional energy cost. Due to the small gate area, small input capacitance, and high energy efficiency, the inverter-based circuits with trimming are suitable for a variety of applications such as dc-coupled sensor amplifiers, front-end receivers, and low power ADCs.

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