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Highly Optimised Complementary Inverters Based on p-SnO and n-InGaZnO with High Uniformity

Jin Yang, Yiming Wang, Yunpeng Li, Yuzhuo Yuan, Zhenjia Hu, Pengfei Ma, Li Zhou, Qingpu Wang, Aimin Song, Senior Member, IEEE, and Qian Xin

Abstract—Oxide semiconductors are desirable for large-area and/or flexible electronics. Here, we report highly optimised complementary inverters based on n-type indium gallium zinc oxide and p-type tin monoxide thin-film transistors. Oxide-based inverters with a record voltage gain of 142 have been achieved. The switching point voltage has also been tuned to reach the ideal value, namely half value of the supply voltage. A narrow transition width of 1.04 V (13% of the supply voltage) is achieved which offers a strong anti-jamming ability to avoid logic errors. Rail-to-rail output voltage swing has been achieved. The inverters still maintain high performance at a low supply voltage of 6 V. A very large number of inverters have been fabricated and showed excellent uniformity in a working area of 1 cm × 1 cm. The switching point voltage and transition width show very small standard deviations of only 0.55% (0.022 V) and 2.3% (0.024 V), respectively, demonstrating promising performance for large-scale circuit integration.

Index Terms—Complementary inverter, indium gallium zinc oxide (IGZO), tin monoxide (SnO), thin-film transistor (TFT), uniformity, static voltage gain, noise margin.

I. INTRODUCTION

OXIDE semiconductors are highly attractive due to their unique advantages of high carrier mobility (~1–100 cm²/V·s) in comparison to amorphous silicon and organic semiconductors, visible light transparency, and large-area and low-temperature processability [1, 2]. Oxide-based inverters, which are the basic building blocks in both digital and analog circuits, have been intensively studied for phase reversals, amplifications, wave shaping, etc. Up to date, most reported inverters based on oxide semiconductors were composed by two n-type oxide thin-film transistors (TFTs) [3-8], due to the lack of high-performance p-type oxide TFTs. These inverters generally show a low voltage gain mainly due to their weak ability of logic pull-up. However, high voltage gain is critical for integrated circuits such as amplifiers, 6-transistor SRAM, high-order ring oscillators, etc. Complementary inverters have advantages of low power consumption, high voltage gain, good noise immunity, and wide output voltage swing, which are crucial in real applications. Recently, complementary inverters based on n-type oxides and p-type organic [9-17] or carbon nanotubes [18, 19] were fabricated. In these complementary inverters, low operation voltage (~3 V) [9, 12, 14] and an extremely high voltage gain of 890 [15] have been achieved. However, stability and/or processing compatibility for large-scale integration are still big challenges.

Recently, several complementary inverters based on all oxide semiconductors have been demonstrated [2, 20-28]. Dindar et al. reported a complementary inverter employing n-type IGZO and p-type Cu₂O [25]. The inverter showed a high voltage gain of 120, but the switching point voltage was far from the half value of supply voltage. Chiu et al. have realized a complementary inverter based on n-type ZnO and p-type SnO with a high noise margin level, but the voltage gain is as low as 17 [24]. Overall, it is still challenging to simultaneously achieve high voltage gain, high noise margin level and satisfactory switching point voltage, which would require significant improvement of the on-off ratio, mobility, and subthreshold swing of p-type oxide TFTs. In addition, the uniformity of the reported oxide based inverters has hardly been tested in previous reports, but uniformity and reproducibility are extremely important for the large-scale integration and mass production. Furthermore, the environmental stability and bias stress stability should also be studied. Among the reported limited numbers of p-type oxide materials, SnO has been regarded as the most promising one due to its high hole mobility originated from the Sn delocalized 5s nature at the valence band maximum (VBM) [29]. By optimising the performance of p-type SnO TFTs [30], we have recently realized complementary inverters based on n-type IGZO and p-type SnO with a high voltage gain of 112 [31]. In this letter, we further improve the overall performance.
including higher voltage gain, better matching of switching point voltage, and higher noise margin level. More importantly, excellent uniformity reproducibility over a 1 cm × 1 cm area has been demonstrated.

II. EXPERIMENTAL

Figure 1(a) shows a schematic diagram of a complementary inverter composed of an n-type IGZO and a p-type SnO TFT. First, a 5-nm-thick Ti layer for adhesion and a 30-nm-thick Au layer as the gate electrode were deposited on a Si/SiO₂ substrate by electron-beam evaporation. A 30-nm-thick Al₂O₃ was then deposited as the gate dielectric by atomic-layer deposition at 150 °C. A p-type SnO layer with a thickness of 20 nm was deposited by radio-frequency magnetron reactive sputtering at room temperature [31]. The SnO films were annealed in the ambient air at 225 °C for 2 hours. A 24-nm-thick n-type IGZO layer was then deposited by RF magnetron sputtering at room temperature [32]. Ti (50 nm) /Au (30 nm) were deposited as source/drain ohmic contacts by electron-beam evaporation. Finally, the sample was annealed at 150 °C for 1 hour in the ambient air. The electrode and channel layers were patterned by UV lithography and lift off. The Al₂O₃ layer was patterned by UV lithography and inductively coupled plasma reactive ion etching. The electrical characteristics of TFT devices and complementary inverters were measured using a source/measure unit (Agilent B2902A) and oscilloscope (Keysight MSOX6004A) in dark at room temperature.

III. RESULTS AND DISCUSSION

Figures 1(b) and (c) show the transfer characteristics of the p-SnO and the n-IGZO TFTs at the drain-source voltage (V_DS) of -0.1 V and 0.1 V, respectively. The p-type TFT has an on/off current ratio of 2.6 × 10⁴, which is, to the best of our knowledge, the highest value in the reported complementary oxide-based inverters [2, 20-28], a high linear mobility of 0.7 cm²V⁻¹s⁻¹, and a threshold voltage (V_TH) of -4.8 V. Subthreshold swing (SS) was 1.4 V/dec, extracted from the linear portion of the log (I_DS) versus V_GS plot. The IGZO TFT has an on/off current ratio of 10⁸, a linear mobility of 8.2 cm²V⁻¹s⁻¹, a V_TH of 3.9 V, and an SS of 0.48 V/dec. The better SS than what we reported before [31] is achieved by applying annealing at a higher temperature of 150 °C enabling a lower defect density in the channel. In addition, the TFTs show steady IV characteristics after being kept in ambient air for 4 months as shown in Figs. 1(b) and (c), indicating a high environmental stability despite having no encapsulation layer. The output curves of the SnO and IGZO TFTs indicate good Ohmic contacts between Ti and SnO and IGZO, plotted in Figs. 1(d) and (e).

To optimise the matching between the n- and p-type TFTs, we have optimised the geometric aspect ratio, N, defined as the width-to-length ratio of SnO TFT (W/L)ₚ divided by the width-to-length ratio of IGZO TFT (W/L)ᵣ. The results of inverters with N ranging from 6 to 9 at a supply voltage (V_DD) of 8 V are shown in Fig. 2(a). With the increase of N, the ability of logic pull-up by the SnO TFT becomes stronger. As a result, the static voltage transfer characteristics (VTCs) of the inverters move to the higher voltage direction. The optimised value of N is 8, since the curve of N = 8 at 8 passes through the intersection point of V_out = V_in and V_out = Vin/2.

Figure 2(b) shows the static VTCs of inverters with N = 8 at different V_DD of 6, 7, and 8 V. The inverter performance is shown in Table I. The input-low voltage (V_IN) and the input-high voltage (V_HI) are the input voltage values at the points where dV_OUT/dV_IN = -1. The output-low voltage (V_LO) and the output-high voltage (V_HI) reach 0 V and V_DD, respectively, thus achieving rail-to-rail output voltage swing. For V_DD = 8 V, the static voltage gain (dV_OUT/dV_IN), derived from the VTC, was 137, which is to the best of our knowledge, the highest gain among complementary oxide-based inverters up to date. It was
In this work, complementary inverters composed of n-type IGZO TFT and p-type SnO TFT were fabricated on a Si/SiO₂ substrate via a low-temperature process which can be directly applied to flexible substrates such as polyimide. To the best of our knowledge, these inverters have achieved the highest voltage gain at the lowest supply voltage, most optimised switching point voltage at half value of supply voltage, and very high noise margin level. Importantly, these inverters exhibit excellent uniformity over a large sample area of 1 cm × 1 cm. Our results indicate that complementary technology based on all oxide semiconductors is highly competitive and has great potential in future large-scale flexible and/or transparent integrated circuits.

### IV. Conclusion

TABLE II

<table>
<thead>
<tr>
<th>Channel materials</th>
<th>V_{in}(V)</th>
<th>Gain</th>
<th>NM_H(V)</th>
<th>NM_L(V)</th>
<th>Year</th>
</tr>
</thead>
<tbody>
<tr>
<td>n-In_{2}O₃</td>
<td>100</td>
<td>11</td>
<td>40</td>
<td>22</td>
<td>2008[20]</td>
</tr>
<tr>
<td>p-SnO₂</td>
<td>120</td>
<td>11.68</td>
<td>6.01</td>
<td>2011[21]</td>
<td></td>
</tr>
<tr>
<td>n-IGZO</td>
<td>17</td>
<td>4.2</td>
<td>6.5</td>
<td>2011[22]</td>
<td></td>
</tr>
<tr>
<td>p-CuInO₃</td>
<td>15</td>
<td>1.7</td>
<td>1.1</td>
<td>2012[2]</td>
<td></td>
</tr>
<tr>
<td>n-SnO₂(X&lt;2)</td>
<td>17</td>
<td>4.9</td>
<td>9.8</td>
<td>2013[23]</td>
<td></td>
</tr>
<tr>
<td>p-SnO₂(X&lt;2)</td>
<td>10</td>
<td>17</td>
<td>4.29</td>
<td>4.35</td>
<td>2014[24]</td>
</tr>
<tr>
<td>n-ZnO</td>
<td>10</td>
<td>3</td>
<td>2.7</td>
<td>1.2</td>
<td>2014[25]</td>
</tr>
<tr>
<td>p-SnO</td>
<td>40</td>
<td>102</td>
<td>7.3</td>
<td>14.9</td>
<td>2015[26]</td>
</tr>
<tr>
<td>n-ZnO</td>
<td>12</td>
<td>12</td>
<td>6.2</td>
<td>3.8</td>
<td>2016[27]</td>
</tr>
<tr>
<td>p-SnO</td>
<td>40</td>
<td>24</td>
<td>20</td>
<td>14.4</td>
<td>2017[28]</td>
</tr>
<tr>
<td>n-IGZO</td>
<td>8</td>
<td>142</td>
<td>3.6</td>
<td>3.4</td>
<td>Our work</td>
</tr>
</tbody>
</table>

In Fig. 3, the transfer curves of (a) eight IGZO TFTs (W/L = 30 μm/10 μm) and (b) eight SnO TFTs (W/L = 240 μm/10 μm) at different drain-source voltages, showing the mean value and standard deviation of V_{TH}.

Fig. 4. Static voltage transfer characteristics (a) and Static voltage gains (b) of 12 inverters with different n-type- and p-type-IGZO TFTs and N = 8 at a V_{DD} of 8 V. The values of static voltage gain (c), switching point voltage (d), and transition width (e) of these 12 inverters.

Calculated that the noise margin high (NM_H = V_{OH} - V_{IL}) was 3.55 V, which is 44% of V_{DD}, and the noise margin low (NM_L = V_{IL} - V_{OL}) was 3.43 V, around 43% of V_{DD}. The large values suggest that the inverter can withstand a high noise level, and offer a strong anti-jammering ability to avoid logic errors. This is vitally important for reliable work of large-scale integrated circuits. The inverter shows a small hysteresis with V_{SP} at 3.98 V, an ideal value close to V_{DD}/2, in the forward scan, and 4.46 V in the reverse scan at V_{DD} = 8 V. Importantly, even if V_{DD} is as low as 6 V, the inverter still maintains the V_{SP} at V_{DD}/2 and relatively high voltage gain of 75.

The transfer curves of eight IGZO TFTs and eight SnO TFTs randomly selected in an area of 1 cm × 1 cm under different V_{OS} values up to 8 V are characterized as shown in Fig. 3, demonstrating that these n-type- and p-type-IGZO TFTs have a high uniformity and almost constant V_{TH}. Figures 4(a) and (b) display the static VTCs and voltage gains of 12 inverters with different width-to-length ratios of IGZO TFTs, (W/L)n, and N = 8 at a V_{DD} of 8 V. These inverters are randomly selected in a 1 cm × 1 cm sample area. The 12 inverters show nearly uniform VTCs, as shown in Fig. 4(a). The results demonstrate not only robustness of the design at different channel lengths but also excellent uniformity over a large sample area. Figure 4(c) shows that the maximum gain is 142. In Fig. 4(d), the V_{SP} is 4 V in average, equal to the ideal value, with extremely small standard deviation (S.D.) of 0.022 V. The transition width is 1.04 V (13% of V_{DD}) in average with very small S.D. of 0.024 V, indicating high noise margin level with high uniformity, as shown in Fig. 4(e). The inverters show relatively low power consumption, and the average power is 4 μW when V_{in} increases from 0 to 8 V to complete a logic inversion operation at V_{DD} = 8 V. A summary of the performance of complementary inverters based on all oxide semiconductors in recent years and our work is shown in Table II, showing that most key parameters are the best among complementary inverters based on all oxide semiconductors to date.

### REFERENCES


