Complementary Integrated Circuits Based on p-type SnO and n-type IGZO Thin-Film Transistors

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Abstract—Oxide semiconductors are highly attractive for the new-generation transparent/flexible electronics. In this letter, logic gates (inverter, NAND and transmission gates) and 3-stage ring oscillators based on n-type indium-gallium-zinc-oxide (IGZO) thin-film transistors (TFTs) and p-type tin monoxide (SnO) TFTs are presented. The IGZO TFTs show a mobility of 10.05 cm²/Vs and a threshold voltage of 5.00 V. The SnO TFTs exhibit a mobility of 1.19 cm²/Vs and a matched threshold voltage of -5.05 V. At a supply voltage of 10 V, the complementary inverters show an extremely high gain of 112 with a geometric aspect ratio of 5. The dynamic responses of the logic gates based on n-type IGZO and p-type SnO TFTs are also examined. The delay time of the inverter measured from dynamic response is 27.75 µs at a supply voltage of 10 V. The inverter, NAND, and transmission gates all exhibit ideal rail-to-rail output voltage behavior. At a supply voltage of 20 V, the 3-stage ring oscillators are able to operate at 32.87 kHz, and the stage delay is 5.07 µs.

Index Terms— Complementary inverter, logic gates, ring oscillator, tin monoxide (SnO), indium-gallium-zinc-oxide (IGZO), thin-film transistor (TFT).

I. INTRODUCTION

Oxide semiconductors have received much attention due to a number of advantages including low cost, low fabrication temperatures, high carrier mobilities, good transparency in visible region, mechanical flexibility, as well as scalable deposition methods compared with amorphous silicon[1-4]. Under the advantages mentioned above, oxide semiconductors have been regarded as one of the most promising candidates for transparent/flexible electronics[2, 3].

So far, n-type oxides, such as indium-gallium-zinc-oxide (IGZO), are highly researched and even some of them have been commercialized [4]. For instance, IGZO thin-film transistors (TFTs) have started to replace amorphous silicon TFTs for backplane drivers of flat-panel displays[1]. Flexible IGZO Schottky diodes operating beyond 2.45 GHz have already satisfied the principal frequency of smart phones[5]. Subthreshold Schottky-barrier IGZO TFTs have been demonstrated to be useful for sensor interface circuits in wearable electronics[6]. On the another hand, p-type oxide semiconductors are far behind mainly because of low on/off ratio, low hole mobility, and high subgap trap density[3]. However, p-type TFTs are essential in order to fabricate complementary integrated circuits with low static power consumption, high noise margin, high yield, and high reliability for actual applications. Realizing sophisticated all-oxide circuits operating in complementary mode has been challenging due to the difficulty in making high-performance p-type oxide TFTs matched with their n-type counterparts. Up to date, SnO is considered as the most promising p-type oxide due to its high field-effect hole mobility, good uniformity for large-scale fabrication, and high stability in ambient air [3,7]. To realize complementary inverters, one can either combine an n-type TFT and a p-type TFT or use two ambipolar TFTs. A rail-to-rail output voltage behavior can be easily achieved in the former but hard to achieve in latter case because neither of the two ambipolar TFTs can be fully switched off [8, 9, 10, 11]. The static current will also result in a static power consumption, which may be an issue in the case of large scale integration. Complementary inverters using n-type oxide (such as In₂O₃, SnO₂, IGZO, and ZnO) TFTs and p-type SnO TFTs have been reported[12-19]. Five-stage ring oscillators based on n-type ZnO and p-type SnO TFTs have been fabricated on glass and polyimide foil substrates[12, 13]. Common-source amplifiers, differential amplifiers, and logic gates have also been realized on paper substrates[20]. From the point of industrial application, high gain of complementary inverter is quite desirable in order to achieve large noise margins of the integrated circuits. However, to the best of our knowledge, the gains of the reported complementary inverters based on n- and p-type oxides are not higher than 30 under a supply voltage of 10 V until now [2, 3, 12, 13, 15, 16, 18, 24]. Furthermore, to date, the dynamic responses of oxide-based complementary logic gates with rail-to-rail output voltage behavior have not been reported yet. In this work, we fabricated
high-performance n-type IGZO TFTs and p-type SnO TFTs via room-temperature sputtering method which is suitable for large-scale fabrication and commercialization for transparent/flexible electronics. Moreover, we realized the integration of SnO and IGZO TFTs to achieve complementary inverters with extremely high voltage gain up to 112. Based on these inverters, we have realized 3-stage ring oscillators, NAND, and transmission gates with rail-to-rail output voltage behavior, and the dynamic responses of these logic gates are analyzed.

II. EXPERIMENTS

The TFTs and circuits were fabricated on silicon substrate with 300-nm-thick thermally oxidized SiO$_2$. First, 50-nm-thick Al was deposited using thermal evaporation and patterned as gate electrode. Then, 30-nm-thick Al$_2$O$_3$ was deposited as dielectric by atomic-layer deposition (ALD) and patterned by wet etching. Next, 20-nm-thick SnO film was fabricated by radio-frequency magnetron sputtering and patterned by lift-off process followed by a post-annealing at 225 °C for 1 h in air. After that, 24-nm-thick IGZO layer was deposited by sputtering method and patterned by lift-off process followed by the deposition of 50-nm-thick Ti as source/drain electrodes and interconnects using electron-beam evaporation. Finally, the TFTs and circuits were annealed at 100 °C for 1 h in air. In this process, we set the geometric aspect ratio of inverters to be 5. The electrical characteristics were measured by source/measure unit (Agilent B2902A). The outputs of the logic gates and ring oscillators were measured by oscilloscope (Keysight MSOX6004A).

III. RESULTS AND DISCUSSION

Figures 1(a) and (b) show the transfer characteristics of the IGZO TFT and the SnO TFT at drain voltage of 1 and -1 V, respectively. For the IGZO TFT, the mobility is 10.05 cm$^2$/V·s, $V_{TH}$ is 5.00 V. For the SnO TFT, the mobility is 1.19 cm$^2$/V·s, $V_{TH}$ is -5.05 V, $SS$ is 1.50 V/dec, and the on/off ratio is $2.2 \times 10^4$ which is among the highest values of the reported SnO TFTs[3, 21-22]. The output curves of the IGZO TFT and the SnO TFT are shown in Figs. 1(c) and (d), respectively, indicating ideal saturation characteristics and ohmic contacts between the source/drain electrodes and the active layers. The comparable performance of SnO TFT and IGZO TFT guarantees the high-performance complementary inverter based on SnO TFT and IGZO TFT.

Figure 2(a) shows the schematic diagram of a complementary inverter based on a p-type SnO TFT and an n-type IGZO TFT. The operations of the IGZO/SnO complementary inverter at different supply voltages, $V_{DD}$, are shown in Fig. 2(b). The voltage gain at $V_{DD} = 10$ V reaches as high as 112 (Fig. 2(c)), which is the highest value among complementary inverters using n- and p-type oxide TFTs below 10 V supply voltage [2, 3, 12, 13, 15, 16, 18, 24]. The threshold voltage of the inverter, where $V_{IN} = V_{OUT}$, is found to be 1.97 V and 4.25 V at $V_{DD} = 5$ V and 10 V, respectively. They are close to the ideal value, $V_{DD}$/2. The threshold voltage of the inverter can be further optimized by increasing the geometric aspect ratio, which is defined as the ratio of (W/L)$_h$ to (W/L)$_n$, where (W/L)$_h$ and (W/L)$_n$ are the width-to-length ratio of SnO channel and IGZO channel, separately. The input-low voltage ($V_{IL}$) and the input-high voltage ($V_{IH}$) are defined as the point where $d(V_{OUT})/d(V_{IN}) = -1$. When $V_{DD} = 5$ V, $V_{IL} = 1.52$ V and $V_{IH} = 2.26$ V. When $V_{DD} = 10$ V, $V_{IL} = 3.54$ V and $V_{IH} = 4.78$ V. The transition region can be determined by ($V_{IH} - V_{IL}$) which equals 0.74 V and 1.24 V at $V_{DD} = 5$ V and 10 V, respectively. When $V_{DD} = 5$ V, the noise margin high is 2.74 V by using ($V_{DD} - V_{IH}$), and the noise margin low is 1.52 V which equals $V_{IL}$. When $V_{DD} = 10$ V, the noise margin high is 5.22 V and the noise margin low is 3.54 V. The large values indicate that the inverter could withstand a high noise level. The high gain and large noise
margin of inverters ensure that the logic gates and complex circuits for actual applications based on these inverters can be realized and work reliably.

Figure 3(a) shows the schematic diagram of complementary inverter based on a p-type SnO TFT and an n-type IGZO TFT. In the Fig. 3(b), we can see, input pulse, $V_{in}$, and the corresponding output, $V_{out}$, at 4-kHz operating frequency. The delay time of the inverter is found to be 27.75 $\mu$s. Figures 3(c) and (d) illustrate the schematic diagram and performance of a two-input NAND gate based on two complementary inverters, respectively. The output of the NAND is ‘0’ only when both of the inputs are set to ‘1’. Figures 3(e) and (f) show the schematic diagram and performance of a transmission gate, respectively. The output signal, $B$, equals to input signal, $A$, only when the control signal, $C$, is ‘1’. When $C$ is set to ‘0’, $B$ is always ‘0’.

All of the logic gates demonstrate rail-to-rail voltage swing from 0 to 10 V at $V_{DD} = 10$ V. This can be attributed to the robust complementary mode of operation of the IGZO/SnO inverter.

![Schematic diagram and output characteristics of the complementary inverter based on a p-type SnO TFT and an n-type IGZO TFT.]

FIG. 3. (a) Schematic diagram and (b) output characteristics of the complementary inverter based on a p-type SnO TFT and an n-type IGZO TFT. (c) Schematic diagram and (d) output characteristics of the SnO/IGZO NAND gate. (e) Schematic diagram and (f) output characteristics of the SnO/IGZO transmission gate.

Figures 4(a) and (b) show the layout and the schematic diagram of the 3-stage ring oscillator with an output buffer, respectively. Figure 4(c) describes the operation of the ring oscillator at different $V_{DD}$. The oscillation frequency of the ring oscillator increases with increasing of $V_{DD}$. When $V_{DD} = 20$ V, the oscillator frequency reaches 32.87 kHz. The stage delay of the 3-stage ring oscillator can be calculated with $(1/6f)$, where $f$ is the oscillation frequency. The stage delay is found to be 5.07 $\mu$s when $V_{DD} = 20$ V. Such stage delay is in the same order of magnitude compared to the 5-stage ring oscillator based on ZnO and SnO TFTs [12, 13].

![Layout of the 3-stage ring oscillator with an output buffer. Schematic diagram of a 3-stage ring oscillator with an output buffer. Output voltages of the complementary ring oscillator as a function of time at different $V_{DD}$.

FIG. 4. (a) Layout of the 3-stage ring oscillator with an output buffer. (b) Schematic diagram of a 3-stage ring oscillator with an output buffer. (c) Output voltages of the complementary ring oscillator as a function of time at different $V_{DD}$.

IV. CONCLUSIONS

In this letter, complementary inverters with extremely high voltage gain up to 112 at $V_{DD} = 10$ V are fabricated based on the n-type IGZO and the p-type SnO TFTs. The dynamic responses of the inverter, NAND and transmission gates are analyzed. The delay time of the inverter is 27.75 $\mu$s at $V_{DD} = 10$ V. All of the fabricated logic gates show ideal rail-to-rail output voltage behavior. The output frequency of 3-stage ring oscillator reaches 32.87 kHz when $V_{DD} = 20$ V. Our study indicates that other complementary logic gates and sophisticated circuits for potential larger-area transparent/flexible electronics with large noise margin and low static power consumption can be realized based on n-type IGZO and p-type SnO TFTs.

REFERENCES


