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Capacitor Balancing Controller Voltage Sorting Statistics in Modular Multilevel Converters

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Abstract—Modular multilevel converters (MMCs) are made up of many submodules (SMs) connected in series. In order to avoid semiconductor over-voltages, SM capacitors should be kept within strict voltage limits. The capacitor balancing controller (CBC) is used to sort SM capacitor voltages prior to modulation. This paper investigates the variation in sorting complexity at steady state and transient conditions for a brute-force and past-position methodology based on the bubble sort algorithm. A focus is placed on the potential for ‘worst-case’ sorting, requiring increased computational effort. This paper forms part of ongoing research to analyze the hardware constraints on MMCs with very large numbers of SMs. Simulation results based on a PSCAD/EMTDC detailed equivalent model are used for analysis and conclusions.

Keywords—Modular Multilevel Converter, Nearest Level Control, Capacitor Balancing Control, Sorting Algorithm

I. INTRODUCTION

Multilevel converters are an increasingly attractive technology for high voltage applications, especially in facilitating the transmission of power from offshore wind to mainland grids [1-4]. A multilevel converter is often defined as a converter which can output three or more levels at the ac phase terminals [5]. Many variations of multilevel converter exist. However, they are primarily based on the three main topologies: Cascaded Two-Level Converters (C2LCs), Alternate-Arm Converters (AACs) and Modular Multilevel Converters (MMCs), commercialized by ABB, GE Grid Solutions and Siemens respectively [5-8]. MMCs are ideal for high-voltage direct-current (HVDC) applications, replacing traditional Line-Commutated Converters (LCCs) and two/three-level Voltage Source Converters (VSCs) [5]. The number of VSC-HVDC projects using multilevel converters has increased from two in 2012 to eighteen in 2017 (October), with growth expected to continue increasing over the coming years [9]. The growth of VSC-HVDC in Europe is driven by increased investment in renewable generation, particularly offshore wind energy, as governments adhere to the 2020 green energy target deadlines [10-13]. The global HVDC (and FACTS) market size is expected to increase by nearly 50%, from \$6 bn in 2014 to \$9 bn by 2020. The rate of increase during this time is also expected to rise, predicting continued adoption of HVDC technologies over the coming decade [14]. Despite increases in the number of publications regarding

VSC-HVDC, public domain knowledge of multilevel converters is still limited [15]. The need for a more detailed understanding of the operation of multilevel converters continues to rise as they become a more popular solution for HVDC connections. The principal benefits of multilevel over two/three-level topologies are as follows [16-18]:

- Reduced switching frequency (increased efficiency)
- Modular construction (for ease of repair)
- Reduced harmonics (minimizes filter requirements)

The level count chosen for a multilevel converter is influenced by a number of factors. One constraint is the harmonic performance of the converter. Reference [19] concluded that an MMC requires only 15 levels to meet harmonic regulations if connected to an 11 kV network due to inherent damping in distribution systems [19]. However, basic analysis of a 31-level staircase waveform from a signal generator, similar to that of a MMC without filtering, reveals that a 31-level MMC would meet IEEE 519 harmonic limits but fail to meet the IEC standards for individual harmonic distortion [20] and ENA G5/4-1 recommendations [21]. Given the simplicity of the analysis by [20] and considering a connection to a transmission network, 31 levels is taken as sufficient for the minimum number of levels required by an MMC to meet harmonic requirements [20]. Another constraint is set by semiconductor-switch technology. In the case of multilevel converters, and other high voltage applications, the Insulated Gate Bipolar Transistor (IGBT) is typically favored. Recent improvements in Silicon Carbide (SiC) switches have pushed collector-emitter voltage ratings above 10 kV per device. However, in HVDC transmission, reliability is crucial. Until the questions surrounding SiC are answered [5], Silicon (Si) remains the dominant choice for IGBTs. For MMCs, IGBT voltage ratings of 3.3 kV and 4.5 kV are most common, suitable for operational voltage ratings up to 2 kV and 3 kV respectively (FIT of 100) [5, 22]. A DC link-voltage of ± 200 kV is typical in HVDC networks, requiring hundreds of IGBTs to spread the voltage stress to suitable levels. Therefore at higher voltages, switch ratings dominate converter design.

In converters with many levels, such as the 201-level Trans Bay Cable, [23] or the 401-level INELFE link [24], nearest level control (NLC) is used. Other modulation schemes

involving vector control or harmonic elimination can be complicated to implement and often lead to high switching frequencies which reduce converter efficiency [16, 25].

NLC constructs a staircase waveform at the converter output which improves with the number of levels. However, the ideal staircase waveform assumes all submodule (SM) capacitors are the same capacity and store an equal amount of energy, allowing for equal voltage steps throughout the waveform. Alternating current in the converter arm charges and discharges the SM capacitors at different rates and if left to run in open loop, voltages can reach unsafe levels, potentially damaging IGBTs. Capacitor balancing control (CBC) is used to maintain the SM voltages to within $\pm 5\%$ of the nominal. The CBC receives and sorts all SM capacitor voltages for the NLC. Reference [26] reviewed alternative balancing algorithms, some without the need for SM voltage measurement [27]. However, these methods may lead to difficulties in transient state operation, especially regarding stored energy estimation. In [28] the ‘‘Tortoise and Hare’’ method was discussed and validated in MMC hardware. Initial studies are promising, but the method requires voltage controlled oscillators for capacitor voltage measurement and limits the number of SM state changes to two per level change, which may not be suitable in all operational scenarios.

The sorting algorithms used by the CBC are often overlooked or omitted in academic research papers e.g. [29]. Typically under the misconception that improvements in computational resource has rendered sorting fast and simple to implement and therefore negligible in calculation time. This may be true for the typical reduced scale prototype MMC; however, [30] highlighted that the chosen sorting algorithm may lead to a bottleneck in computation when sorting large data sets, especially when the time available for calculation is limited, such as in the case of modulating MMCs with hundreds of SMs. Sorting algorithms have been well researched by computer scientists over the years, with the most common defined in terms of worst, average and best-case performance. Hardware considerations during MMC design partly rely on this information but very little knowledge exists in the public domain on how the algorithms perform in the context of MMCs. This paper seeks to provide a more in-depth understanding of how sorting varies during system operation.

Bubble sort, a simple algorithm to understand and implement, has been cited in a few publications for use with MMCs [20, 31-33]. Following this, two common sorting methods based on bubble sort, ‘brute-force’ and ‘past-position’, are investigated and compared for steady-state and transient conditions. A focus is placed on the potential for worst-case sorting, as this would allow designers to better size control hardware for peak sorting intensity. Histograms and point-on-wave (POW) graphs are used to highlight the sorting statistics. Data for these studies are collected using a 31-level PSCAD/EMTDC detailed equivalent model (DEM) constructed by [34] following the research of [35]. The computational performance of each sorting algorithm is assessed using fundamental operations which can be applied to any hardware. The conclusions are made with the view that sorting statistics can be scaled to considerably larger data sets.

II. MMC TOPOLOGY

A. MMC Structure

The basic structure for a single-phase MMC is shown in Fig. 1a. A converter phase, or leg, is split into two arms, consisting of a number of submodules and a reactor connected in series. At the simplest level each SM contains a half-bridge converter utilizing IGBTs (S1, S2), anti-parallel diodes (D1, D2) and an SM capacitance (Csm), as depicted in Fig. 1b. Typically, the SMs will also have integrated circuit protection and bypass switches for fault control [1, 20]. By duplicating the single-phase design across the DC link a three-phase MMC can be created. Only two switch states are used during normal operation: closing S1 to connect the capacitor or closing S2 to bypass the capacitor. Fig. 1c describes the switching pattern for the SM. In Fig. 1c, ‘1’ represents a closed switch and ‘0’ represents an open switch.

It can be seen from Fig. 1b that the SM terminal voltage (V_{sm}) is equal to the capacitor voltage (V_{cap}) when S1 is closed (neglecting diode and IGBT voltage drops). Csm will charge or discharge depending on the arm current direction while connected. By opening S1 and closing S2, the capacitor is bypassed, effectively shorting V_{sm} . At no point should S1 and S2 both be closed as this creates a short circuit across the capacitor, leading to dangerous over-currents. The arms of the converter are made up of series connected SMs therefore, through appropriate switching control, each arm can be considered as a variable voltage source.

B. MMC Operation

The equivalent circuit for a single-phase MMC, seen in Fig. 2, can be used to further describe system operation. Two controllable voltage sources, V_{ua} and V_{la} , are used to represent the upper and lower converter arms respectively. The ac phase voltage is taken over Z_l , the mixed impedance ac load, with respect to the mid-point of the dc link, assumed to be at earth potential [20]. R_{arm} and L_{arm} are the arm resistance and inductance respectfully.

Fig. 1. Single-phase MMC (a) with basic SM design (b) and nominal operation mode switching patterns (c)

Fig. 2. Equivalent circuit for single phase MMC

Kirchoff's Voltage Law can be applied to the circuit in Fig. 2 to derive (1) and (2) describing the phase voltage, V_a :

$$V_a = \frac{V_{dc}}{2} - V_{ua} - L_{arm} \frac{dI_{ua}}{dt} - I_{ua} R_{arm} \quad (1)$$

$$V_a = V_{la} - \frac{V_{dc}}{2} + L_{arm} \frac{dI_{la}}{dt} + I_{la} R_{arm} \quad (2)$$

Equations (3) and (4) represent the upper and lower arm currents, I_{ua} and I_{la} , respectively; each comprises:

- I_{dc} , a dc component from the dc link voltage shared across the three phases equally
- I_a , an ac phase current generated by the phase voltage shared across the arms equally
- I_{circ} , a dc component created by unequal voltages between converter phases

$$I_{ua} = \frac{I_{dc}}{3} + \frac{I_a}{2} + I_{circ} \quad (3)$$

$$I_{la} = \frac{I_{dc}}{3} - \frac{I_a}{2} + I_{circ} \quad (4)$$

By combining (1) – (4), (5) can be derived which describes the relationship between the phase voltage and arm voltages.

$$V_a = \frac{V_{la} - V_{ua}}{2} - \frac{L_{arm}}{2} \frac{dI_a}{dt} - \frac{R_{arm}}{2} I_a \quad (5)$$

During normal operation half of the SMs in a phase will be connected across the dc link. The nominal voltage on each SM capacitor can be described by (6) where n represents the number of SMs in an arm. The number of SMs connected in each arm then determines the output voltage for the upper and lower arms as seen in (7) and (8).

$$V_{cap} = \frac{V_{dc}}{n} \quad (6)$$

$$V_{ua} = n_{oua} V_{cap} \quad (7)$$

$$V_{la} = n_{ola} V_{cap} \quad (8)$$

It can be seen from (5) – (8) that the phase voltage can be determined through appropriate control of the SMs. This control will be further described in III.

Only half of the SMs in a converter leg are connected at any one time, therefore the number of levels in the system must be chosen accordingly. In a ± 200 kV system, a minimum of 200 SMs per arm are required to keep the nominal voltage stress across IGBTs at 2 kV, creating a 201-level converter.

III. MMC CONTROL

A. Inner Voltage Control

The MMC has multiple levels of cascaded control from multi-terminal system behavior down to semiconductor switching. The control loop of interest in this paper is the inner voltage loop, consisting of the capacitor balancing controller, nearest level controller and a circulating current suppression controller. Fig. 3 represents the schematic for this control loop.

B. Circulating Current Suppression Control

Circulating current suppression control (CCSC) balances the energy stored in each leg of the converter in order to minimize the I_{circ} component of the arm current in (3) and (4) [16]. When uncontrolled, circulating currents flow between the phases leading to increased losses and greater SM capacitor voltage variation. In this paper, CCSC is assumed to be working ideally, eliminating the I_{circ} term.

C. Nearest Level Control

In two-level converters, pulse width modulation (PWM) or optimal pulse width modulation (OPWM) is used to modulate the output voltage and synthesize a sinusoid at the ac terminals. The frequency of switching in two-level systems is a trade-off between efficiency and harmonics. As discussed by [16], NLC is the simpler low frequency modulation scheme to understand and implement for modular multilevel converters with a high number of SMs.

NLC creates a staircase waveform by outputting the nearest voltage level to the reference voltage, V_{ref} using the round

Fig. 3. Basic control schematic for inner MMC control loop

Fig. 4. 21-level NLC waveform with sinusoidal reference signal

function in (9). Each phase is controlled independently through individual reference comparisons. Fig. 4 represents a 21-level waveform for an NLC with a corresponding reference signal.

The continuous reference sinusoid is sampled and converted. Following (6) and (9), n_{nlc} , the number of SMs required to be turned on, or off, in each arm to meet the reference voltage is calculated. SMs are then selected, and firing signals generated.

$$n_{nlc} = \frac{1}{V_{cap}} \text{round}(V_{ref}) \quad (9)$$

The modulation index, k , for the MMC can be defined by (10) comparing the peak internal ac voltage, V_{pk} to half the dc link voltage, V_{dc} .

$$k = \frac{2V_{pk}}{V_{dc}} \quad (10)$$

D. Capacitor Balancing Control

The choice of which SMs to connect, or disconnect, from the arm is supported by the capacitor balancing controller (CBC). Equations (3) and (4) describe the arm currents in the converter. The alternating nature of these currents leads to an imbalance in capacitor voltages which must be controlled to maintain system stability.

Capacitor voltages from all SMs in the converter are captured and stored in an array. Typically, these voltages are sorted in order of magnitude prior to each level change using a specific sorting algorithm. The arm currents in the converter are measured to determine in which order the voltages should be sorted, highest to lowest or vice versa. A corresponding array of submodule identifiers (SM IDs) is communicated to the NLC which fires the appropriate number of SMs, in the order determined by the SM ID array. By inserting SMs at the lowest voltage when the current is positive and SMs at the highest voltage when the current is negative the capacitors are charged and discharged accordingly.

Following this method all capacitors will be balanced against one another around the capacitor voltage set point, distributing the stored charge equally across the arm.

IV. CAPACITOR VOLTAGE SORTING

A. Common Sorting Algorithms

A number of common sorting algorithms exist, which handle data sets in different ways. Very few papers identify the sorting algorithm used within the simulation or physical prototype MMC. These models and prototypes tend to be simplified or designed with fewer SMs per arm and so the computational constraints are rarely considered. For this reason, papers that mention the chosen sorting algorithm tend to use bubble sort for the simplicity of implementation [20].

The bubble sort algorithm works through a data array (A) comparing and swapping (when required) adjacent values. If sorting into ascending order, a swap is made when the value in position $A[i-1]$ is greater than the value in position $A[i]$, ‘bubbling’ the largest value to the end of the array. A comparison may not always lead to a swap, but a swap always requires a comparison. Subsequent passes through the data are made until the array is fully sorted [36].

The implementation of these methods is open to the programmer. Brute-force methodologies require no historic positioning of data whereas past-position methodologies require details from the previous sort to be stored. For the brute-force method the SM capacitor voltages are captured and placed into an array by physical position in the converter e.g. SM1, SM2, SM3... SMn. The chosen algorithm, bubble sort in this case, will order the array while maintaining the order of the SM ID array. For the past-position method the SM capacitor voltages will be initially placed into their past sorted positions following the historic SM ID array. The chosen algorithm will then order the capacitor voltage array while maintaining the correct positions of SM IDs for the NLC. The SM ID array will be stored for use at the next calculation.

Capacitor voltage data was gathered using the 31-level DEM. A sorting frequency of 1.5 kHz was used in the model; representing a full sort prior to switching at every other level change, i.e. 30 sorts per cycle. The capacitor voltage values from each SM were stored over the duration of the each run (prior to each internal sort).

The brute-force and past-position algorithms were implemented in MATLAB using a custom bubble sort. These functions were applied to each group of capacitor voltages in order to count the number of ‘comparisons’ and ‘swaps’ required to sort the data into ascending order.

B. Steady State Performance

For steady state analysis the DEM was set to import and export real and reactive power at fixed set-points close to the converter limits. Each simulation led to 15,000 unique data points. Only data collected after initial transients had settled were used for the analysis.

Fig. 5 and Fig. 6 represent histograms for the number of comparisons and swaps required to sort the upper arm

Fig. 5. Histogram of comparisons and swaps using the brute-force bubble sort method (import)

Fig. 6. Histogram of comparisons and swaps using the past-position bubble sort method (import)

capacitor voltages of 30 SMs when the MMC is importing 800 MW and 600 MVar of power. Fig. 5 is for the brute-force method and Fig. 6 is for the past-position method. 435 comparisons and swaps are required to bubble sort 30 values in a worst-case scenario. For the brute-force method a worst-case comparison situation occurs when the lowest value is at the large end of the array. In the context of MMCs, SM 30 is always initially placed at the large end of the array. When sorting in ascending order, the maximum number of swaps occurs when the capacitor in SM 30 has one of the lowest 4 potentials in the arm, leading to an increased number of comparisons to complete the sort.

Assuming it is equally likely for each SM to fall into any position in the sort then there is a 13.33% chance SM 30 will have one of the lowest 4 potentials. The data in Fig. 5 and Fig. 6 are made up of 15000 unique measurements; therefore 2000 of these are likely to result in a worst-case comparison situation, matching the large spike at 430 – 435 comparisons on Fig. 5. The number of swaps required to complete the sort using the brute-force method has been shown to closely approximate a Gaussian distribution, centered at the midpoint of 210 – 220 swaps. The mean is 216 swaps and 398 comparisons for the data in Fig. 5.

In order to keep losses to a minimum, SMs are usually only switched on or off a maximum of three times during each fundamental (50 Hz) cycle. In this case, the CBC re-selects at every level change, leading to increased switching losses but improved capacitor balancing. At each converter output level change a minimum of two SMs are switched. As all the SMs in each arm are connected in series the current through each connected SM is the same, therefore the energy transfer to the SM capacitor voltages between sorts remain largely unchanged. By using the past-position method the number of comparisons and swaps decreases significantly in comparison to the brute-force method, at 223 and 90 respectively.

The NLC determines which SMs to connect using the sorted list from the CBC. When the current is negative, the highest voltage SM will be connected to maintain voltage balance. At the following time-step the disconnected SM will be placed into its previous position in the sort, which can lead to increased sorting difficulty. This is seen in Fig. 6 at the 430 – 435 comparison mark. There is an overhead associated with the past-position algorithm as historic position data needs to be retrieved from memory; this is negligible for higher numbers of levels due to the quadratic nature of bubble sort.

Fig. 7 presents the histogram for the number of comparisons and swaps required to sort the upper arm capacitor voltages of 30 SMs using the past-position method. In this case the MMC is exporting 800 MW and 600 MVar of power. The mean number of comparisons and swaps required during power export is 185 and 98 respectively. While the average number of swaps for import and export are similar, the export case has a larger number of high swap count sorts. The average number of comparisons for the export case is lower than that for import, but the spread in comparisons during export is more consistent over the range of different sort complexities. The noticeable differences between Fig. 6 and Fig. 7, especially regarding the required number of swaps, show that sorting scenarios change with power flow.

In summary the past-position method increases the likelihood of a fast sort in comparison to the brute-force algorithm, but both still exhibit poor comparison behaviour.

Fig. 7. Histogram of comparisons and swaps using the past-position bubble sort method (export)

C. Cyclic Worst-Case

Worst-case comparison situations in sorting for MMCs using the brute-force method are mostly random, occurring at any point during the 50Hz cycle as seen in Fig. 8. A worst-case swap situation did not occur during steady state simulations for the brute-force or past-position algorithms.

The past-position algorithm is impacted by the arm voltage and current. Fig. 9 and Fig. 10 are graphs of average comparisons and swaps against arm current and the absolute gradient of the arm voltage. It can clearly be seen that peaks in the number of required operations occur following peaks in dV/dt . Dips in the number of operations during the dV/dt peaks are due to near-zero arm current. As seen in Fig. 8 the brute-force method leads to random peaks in computational intensity, unrelated to the arm current and voltage. From Fig. 9 and Fig. 10 we can see that the most computationally intensive sorting during steady-state operation for the past-position method be likely to occur when the gradient of the arm voltage and the peak arm current are in phase.

Key (Fig. 8, 9 and 10): Gradient of Voltage, black, dashed; Average Number of Operations, red, dash-dot; Current, blue, solid

Fig. 8. Point-on-wave plot of average number of comparisons against arm current and voltage gradient for the brute-force bubble sort method

Fig. 9. Point-on-wave plot of average number of comparisons against arm current and voltage gradient for the past-position bubble sort method

Fig. 10. Point-on-wave plot of average number of swaps against arm current and voltage gradient for the past-position bubble sort method

D. Transient Performance

A complete power reversal was considered for the transient condition to simulate a worst-case scenario for submodule control. Two step changes were considered to analyze algorithm performance, the first from -800 MW, -600 MVar to 800 MW, 600 MVar, represented in Fig. 11 and the second from 600 MW, 800 MVar to -600 MW, -800 MVar, represented in Fig. 12.

Line diagrams of histogram data are presented for each power reversal at 5 equal steps in Fig. 13 and Fig. 14. In both figures the line level corresponds to the histogram bin count for frequency of comparisons required across all 3 phases for 40 ms before the given time. This range is moved in 40 ms steps across 200 ms of transient behaviour. It can be seen that sorting

Fig. 11. Power step -800 MW, -600 MVar to 800 MW, 600 MVar

Fig. 12. Power step 600 MW, 800 MVar to -600 MW, -800 MVar

Fig. 13. Line chart of histogram data for comparisons made during a power step change from -800 MW, -600 MVar to 800 MW, 600 MVar

Fig. 14. Line chart of histogram data for comparisons made during a power step change from 600 MW, 800 MVar to -600 MW, -800 MVar

complexity, in terms of comparisons, tends to follow the change in power, matching the previous findings seen in Fig. 6 and Fig. 7. There is very little ‘transient’ variation during the step-change i.e. no temporary peaks due to the rate of change of power. Therefore the converter sorting algorithm is not noticeably strained during set-point changes. Sorting complexity is instead determined by the power output, arm voltage gradient and arm current.

E. Further Discussion

Sorting algorithms have defined best, average and worst-case performances. The worst-case for bubble sort has a time complexity of $O(n^2)$ which means the time required to complete a sort is increased quadratically with input array size. Other sorting algorithms, such as merge sort, are logarithmic, rather than quadratic. Merge sort has a worst-case $O(n \log_2(n))$ time complexity performance criteria for best, average and worst-case performance i.e. the sort will always require the same number of operations for the same input size regardless of how unsorted the array is.

The merge sort works through a data array A by initially splitting it into two arrays of equal size (± 1 cell). Both of these arrays are split again, into two arrays of equal size (± 1 cell) and so on, until each array is of size 1, and cannot be split. The data is then merged back together, recreating each array by comparing and moving the data to the correct position in arrays of increasing size, this is the ‘merge’ process.

Bubble sort requires memory space for the input array (A) and only one additional variable whereas merge sort requires the memory space for the input array and an array of equal length. One ‘swap’ operation in a bubble sort can require up to 3 ‘move’ operations: if $A[i]$ is less than $A[i-1]$ then *move* value in $A[i-1]$ to temporary variable B , *move* value in $A[i]$ to $A[i-1]$, *move* value in B to $A[i]$. As merge sort utilizes an additional array of equal size, the variables do not need to be swapped, instead they are moved into the appropriate position in a new array: if value in $A[i]$ is less than $A[i-1]$ then *move* value in $A[i-1]$ to new array position $B[i]$ and *move* value in $A[i]$ to new array position $B[i-1]$ [36].

Merge sort was applied to the same submodule voltage data used to generate Fig. 6. Fig. 15 shows a histogram of comparisons and moves for this algorithm. Comparisons vary slightly between sorts due to the method of array merging however it is clear that the number of moves stays the same for every sort. The use of a logarithmic sorting algorithm would be a preferred strategy, as the computational requirements are equal for all possible situations. On-going research investigates the constraints placed on logarithmic sorting algorithms, especially the impact of incorrectly sized hardware on system performance and converter scaling complications.

V. CONCLUSION

The effects of steady state and transient operation on bubble sort, a common $O(n^2)$ algorithm, have been explored and compared against merge sort, a common $O(n \log_2(n))$ algorithm. With a more detailed investigation into how bubble sort performance varies with arm voltage and current. Clearly the use of merge sort, with fixed performance in all scenarios, is a better choice over the variable performance n^2 algorithms, for hardware sizing and average performance. For researchers

Fig. 15. Histogram of comparisons and moves using the merge-sort

or manufacturers implementing the bubble sort algorithm the past-position method consistently outperforms the brute-force method. However, further research is required to identify the correct hardware sizing for either case. On-going research seeks to investigate the impact of incomplete sorting or delayed firing, following incorrectly sized hardware or communication delays, on ac total harmonic distortion. Alternative, partial sorting strategies are also being explored.

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