Thermal and Small-Signal Characterisation of GaAs and GaN Pseudomorphic High Electron Mobility Transistors (pHEMTs)

A thesis submitted to The University of Manchester for the degree of MPhil

In the Faculty of Engineering and Physical Sciences

YEAR OF SUBMISSION: SEPTEMBER 2012

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ABSTRACT

Development of linear temperature dependent small signal models for active devices is useful for circuit designers to predict the circuit performance incorporating the devices. It is especially the case for high power devices where tremendous heat is expected to be generated and the underlying physics of the device could be affected. In this thesis, a comparison of thermal and small-signal characteristics of AlGaAs/InGaAs pseudomorphic high electron mobility transistors (pHEMTs) and AlGaN/InGaN pHEMTs have been analysed and modelled for the first time. A comprehensively developed small-signal parameter extraction procedure has been used which automatically determines the device small-signal parameters directly from the measured S-parameters. An automated direct equivalent circuit parameters (ECPs) extraction, covering temperature range from -40 to 150°C, was carried out on the two types of transistors. Analyses of both sets of the extracted ECPs provide some valuable insights to the governing physics of the transistors which can be helpful for future designs and optimizations for advanced monolithic microwave integrated circuits (MMICs) such as multilayer 3D MMICs.
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DECLARATION

I declare that no portion of the work referred to in the thesis has been submitted in support of an application for another degree or qualification of this or any other university or other institute of learning.
I would like to express my greatest appreciation to my supervisor, Professor Ali A. Rezazadeh. He has given me tremendous help and guidance in the course of this work. He is very supportive and has been a great mentor to me. I also deeply appreciate the help and companionship provided by my senior colleague Mayahsa Mohammed Ali. I am grateful for the help and guidance provided by my sponsor the Bangabandhu Fellowship on Science and ICT Project, Ministry of Science and Technology, Government of the People's Republic of Bangladesh.
CHAPTER ONE: INTRODUCTION

1.1 Introduction

High electron mobility transistor (HEMT) is a field effect transistor incorporating a junction between two materials with different band gaps (i.e., a heterojunction) as the channel instead of a doped region. A commonly used material combination is GaAs with AlGaAs, though there is wide variation, dependent on the application of the device. Devices incorporating more indium generally show better high-frequency performance, while in recent years, gallium nitride HEMTs have attracted attention due to their high-power [20]. To allow conduction, semiconductors are doped with impurities which donate mobile electrons (or holes) and these electrons are slowed down through collisions with the impurities (dopants). HEMTs avoid this through the use of high mobility electrons generated using the heterojunction of a highly-doped wide-bandgap n-type donor-supply layer (AlGaAs or AlGaN) and a non-doped narrow-bandgap channel layer with no dopant impurities (GaAs or GaN).

Ideally, the two different materials used for a heterojunction would have the same lattice constant (spacing between the atoms). In practice, e.g. AlGaAs on GaAs, the lattice constants are typically slightly different, resulting in crystal defects. A HEMT where this rule is violated is called a pHEMT or pseudomorphic HEMT. This is achieved by using an extremely thin layer of one of the materials – so thin that the crystal lattice simply stretches to fit the other material. This technique allows the construction of transistors with larger bandgap differences than otherwise possible, giving better performance. Because there are no dopants atoms in the InGaAs channel to ionically scatter the conduction electrons; the channel
electrons have a high mobility and the pHEMT has higher transconductance or gain. AlGaN/InGaN pHEMTs are similar to the AlGaAs/InGaAs pHEMTs but the semi-insulating material is replaced by either a Silicon substrate or a SiC substrate [37].

The HEMT was originally developed for high speed applications. It was only when the first devices were fabricated that it was discovered they exhibited a very low noise figure. This is related to the nature of the two dimensional electron gas (2DEG) and the fact that there are less electron collisions. On the other hand, pHEMT transistors find wide market acceptance because of their high power added efficiencies and excellent low noise figures and performance [20]. So, an accurate characterisation of pHEMTs is crucial for the design of modern microwave devices. In this work, the comparison of DC, RF and temperature dependent small-signal characterisation and modelling of two type of devices AlGaAs/InGaAs (with 2x100x0.5µm²) and AlGaN/InGaN (with 4x50x0.15 µm²) pHEMTs have been investigated in order to study their electrical characterisations. The procedure used to carry out this task is shown in figure 1.1.

Figure 1.1: Flow diagram of AlGaAs/InGaAs and AlGaN/InGaN pHEMTs performance analysis
The extracted small-signal models of both pHEMTs has been compared and validated to the RF S-parameters measurements. Direct parameter extraction procedure is used which is fast and accurate. The equivalent circuit parameters (ECPs) are accounted insights of the underlying physics of the device, could be achieved by careful analyses. In order to investigate these effects the two pHEMTs are compared with their corresponding ECPs. Thermal effects, being one of the major issues for power-related applications, are one of the key research areas in this work.

The main focus was drawn upon the temperature dependent model parameters and how the underlying physics of the transistors behave in response to the change of temperature. These novel insights are especially valuable for devices designed specifically for high power applications where tremendous heat could be generated. Hence to know how the change of temperature would affect the characteristics and performance of the AlGaAs/InGaAs and AlGaN/InGaN pHEMTs is one of the major concerns. These investigations would assist in the development of reliable, efficient and low cost production of future compact 3D multilayer MMICs.

1.2 Key Objectives

The main aims of this research work are:

- To carry out a review of published theoretical and experimental reports to investigate and to improve electrical characterization of microwave devices such as AlGaAs/InGaAs and AlGaN/InGaN pHEMTs.

- To study the small signal parameter extraction of the AlGaAs/InGaAs and AlGaN/InGaN pHEMTs to fully characterise the microwave device for circuit application. Direct parameter extraction is to be used, where the extraction is made directly from the measured DC and RF data without requirement of iterations or optimisations.
To extend the small-signal model development of the AlGaAs/InGaAs and AlGaN/InGaN pHEMTs and validate the models to the on wafer S-parameters measurements.

To develop temperature dependent small-signal models for the AlGaAs/InGaAs and AlGaN/InGaN pHEMTs and compare the both.

To establish linear temperature dependent expressions for each of the equivalent circuit model parameters and observe the temperature coefficients between AlGaAs/InGaAs and AlGaN/InGaN pHEMTs.

To analyse and attain knowledge of the AlGaAs/InGaAs and AlGaN/InGaN pHEMTs in various temperature and explore ways of optimising the performance.

1.3 Thesis Organisation

Chapter 1: Introduction

This chapter represents a general overview of the research work in concern with High Electron Mobility Transistor (HEMTs). Motivation and key objectives are highlighted. An outline of the thesis is also given.

Chapter 2: Literature Review

For any research work before being undertaken requires a strong foundation or background in-depth study. This chapter provides background reviews on the High Electron Mobility Transistors along with their DC and RF theory in details. Following, pHEMTS are reviewed placing emphasis on the development of small-signal model. Lastly, thermal effects are discussed with its implications on the performance explained.

Chapter 3: Experimental Techniques
The experimental set-up is presented in Chapter 3. Software tools that are used during the course of this work are introduced. Procedures and how to apply them in order to achieve good results are discussed and explained. On-wafer DC and RF measurements are shown and temperature control set-up is given.

- Chapter 4: Results and Discussions

This is the main results chapter providing analysis and discussions of the obtained data. The first sub-chapter discusses device physical structure, the second sub-chapter discusses DC characterisation and results to explore the DC temperature dependent modelling of the pHEMTs, the change of DC characteristics of the both pHEMTs to the change of temperature is observed and explained with the thermal effect. The third sub-chapter represents the RF characterisation where the concept of the development of small-signal model is extended to temperature dependent small-signal model for both pHEMTs. The fourth sub-chapter discusses the noise figures analysis and results. The fifth sub-chapter represents the temperature dependent pHEMTs modelling in concern with temperature dependent equivalent circuit parameters (ECPs) and thermal effects. Circuit parameters are divided into two categories, extrinsic and intrinsic, and analysed. Each of the circuit parameters is expressed in a linear temperature-dependent equation giving a temperature coefficient. The implications of the temperature coefficients are discussed and both AlGaAs/InGaAs and AlGaN/InGaN pHEMTs are compared.

- Chapter 5: Conclusions and Future work

This chapter details the key objectives achieved in this work and identifies and discusses some aspects of the future work.
CHAPTER TWO: LITERATURE REVIEW

2.1 Structure of High Electron Mobility Transistors (HEMTs)

High Electron Mobility Transistors (HEMTs) come from FETs family (Field Effect Transistors). HEMT’s mainly use III-V compound semiconductors as channel material. The main intention behind HEMT is to make use of the high mobility in logical applications instead of silicon. But later it was found that HEMT has very low noise figures which attracted communication sector and since it’s been used widely in the high frequency applications. The main difference in a HEMT device is in the layer layout structure where it experiences the two dimensional electron gas (2DEG) phenomena. The 2DEG accounts for the term of high electron mobility due to the high electron sheet density for the confined electrons in the quantum well where the 2DEG sheet is formed.

Similar to FET devices, the gate dimensions of HEMT devices (gate length L_g x gate width W_g) are very important. As the gate length L_g plays an essential role in determining the maximum frequency of the device whereas the gate width (W_g) affects the device current [2]. In microwave applications, the typical gate length L_g is between (0.1 μm – 1 μm) [5]. The gate width can be 100 to 2000 [5] times bigger than the gate length L_g. Small gate width W_g dimension is preferred to reduce the noise. On the other hand, large gate width is required for power application. As a result, a compromise needs to be made depending on the application in which the device would be used.

Lastly the bulk and the contact material of the semiconductor device affect the physical and electrical characteristic of these devices. The above advantages make HEMTs strong candidates for low noise microwave and millimeter-wave applications as they yield higher gain value than noise figure [3].
2.1.1 Two-Dimensional Electron Gas (2DEG)

As the HEMT is closely related to the JFET and the MESFET, these devices use the electric field to control the flow of current through the device. The HEMTs characterized by its creation of a two dimensional electron gas (2DEG). A 2DEG is an effect dictated by the principles of quantum mechanics and a uniquely shaped potential well. A triangular potential well is created. Electrons tunnel into it, but cannot get out. In the well, the electrons obey their wave properties (recalling that everything is both a particle and a wave at the same time), and end up in the part of the well corresponding to the first half-wavelength of the electron, called the first energy sub-band. They cannot go any deeper into the potential well because quantum mechanics states that they have a zero probability of taking up a space smaller than their half-wavelength \([10]\). Of course, this channel only covers one of the dimensions, in this case the thickness of the device. The electrons are free to form a sheet in the other two dimensions (length and width of the device), and since the motion of the charges in the sheet is random like a gas, for this, the term two-dimensional electron gas.

2.1.2 Epitaxial Layer Structure of HEMTs

Conventional HEMTs are heterostructure field effect transistors with high electron mobility. The 2DEG phenomena emerges when a wide band gap (n-type layer) of undoped AlGaAs usually with a thickness of (50 Å) \([5]\) is sandwiched between two layers; one is of narrow band gap energy material and the other is a doped semiconductor material. These two layer are: A bottom layer (called the buffer layer) of p-type GaAs (narrow band gap semiconductor) very slightly doped and a top layer of n-type doped AlGaAs layer (called the supply layer). The electrons from the supply layer are free to move in the entire crystal and they are controlled by their thermal energy, until they are trapped in the quantum well.

The above undoped AlGaAs is grown on top of the buffer layer and is called the spacer layer. It is lattice matched with the GaAs buffer layer which in turn is
grown on top of the bottom semi-insulating layer. The thickness of the buffer layer can be up to 5000 Å [5] and the thickness of the supply layer is typically (300 – 2000 Å) [5]. The thickness and doping profile of the undoped AlGaAs spacer layer is carefully designed so that it is fully depleted when the device is under normal biasing conditions. On top of the n-doped (10^{17} – 10^{18} cm^{-3}) [3] supply layer, a highly doped (up to 7 × 10^{18} cm^{-3}) GaAs layer is grown. This layer is called the ohmic (contact) layer to facilitate the source and drain contacts. Then this layer is recessed so that the schottky gate contact is deposited on top of the doped AlGaAs supply layer. A cross-sectional view of HEMT layer structure is depicted in figure 2.1.

An active layer is formed in the quantum well (the GaAs buffer layer) because two layers of different band gap energy and doping profile are grown on top of each other as mentioned before. One of high band gap usually n-type doped AlGaAs and a narrow band gap layer of undoped GaAs. The electrons transfer from the higher conduction band to the lower conduction band where a dip occurs at the boundary between these two layers as a result of the difference in their conduction band energy levels [5]. The active thin layer is formed at the interface between the
undoped AlGaAs spacer layer and the GaAs buffer layer. The electrons in the quantum well create a very thin sheet with carrier density of about \((5 \times 10^{11} \text{ cm}^{-2} \text{ to } 10^{12} \text{ cm}^{-2})\) for AlGaAs based HEMTs [3].

The electrons in the quantum well experience a phenomenon called the two dimensional electron gas (2DEG). The electrons in this sheet can be separated from the donor atoms which results in reduced coulomb scattering. Regarding this reason, the electrons are high in concentration and mobility and free to move in the direction parallel to the interface. If the thickness of the doped AlGaAs supply layer is not thick enough to be depleted under normal operation, the contact parasitics will contribute as a reducing factor to the 2DEG concentration and their speed in the quantum well. The thickness of the quantum well is typically about 100 Å. This 2DEG layer is very thin most likely less than 30 Å [3].

The electron concentration in the depletion region is inversely proportional with the gate bias \(V_g\). The role of the high resistivity GaAs ohmic layer is to passivate the doped n-AlGaAs spacer layer which reduces unwanted contact resistance for ohmic metallization. The n-AlGaAs supply layer supplies electrons to the active channel where the 2DEG occurs. The buffer layer role is to prevent any coupling between the substrate layer and the undoped AlGaAs spacer layer.

2.1.3 Depletion and Enhanced Mode HEMTs

The depletion-mode HEMT device is the most common mode used in microwave applications. In this device, there is a current flow through the 2DEG region before the application of a reverse-bias gate voltage \(V_g\). When small amount of drain – source voltage \((V_{ds})\), a current starts to flow and it is directly proportional to \(V_{ds}\). As the voltage increases the electrons starts to gain high carrier velocity for a while until they reach the saturation state, in which the current stays constant. Whereas, increasing \(V_g\) reduces the current conduction. On the other hand, for enhanced mode HEMT device the current doesn’t flow until forward gate bias is applied [5].
2.1.4 Pseudomorphic High Electron Mobility Transistors (pHEMTs)

In Pseudomorphic HEMTs an additional layer of usually undoped InGaAs placed between the GaAs buffer layer and undoped AlGaAs layer. The AlGaAs/InGaAs device is usually called a pseudomorphic HEMT, because of the lattice mismatch between the AlGaAs (narrow band gap) and InGaAs (wide band gap) layers. The two-dimensional electron gas channel improves transport properties due to the higher mobility of InGaAs. The Schottky contact to the semiconductor is made through standard Pt/Ti/Au layered structure. Drain and source contacts are alloyed AuGe/ NiAu and this type of structure has been established as a very stable and robust contact structure. All the discrete pHEMTs are passivated with silicon nitride ($\text{Si}_3\text{N}_4$) which doubles as scratch protection [16]. A cross-sectional view of AlGaAs/InGaAs pHEMTs layer structure is depicted in figure 2.2.

![AlGaAs/InGaAs pHEMT epitaxial layer structure](image.png)

Figure 2.2: AlGaAs/InGaAs pHEMT epitaxial layer structure [37]

AlGaN/InGaN pHEMT composition and structure similar to the AlGaAs/InGaAs pHEMT in figure 2.3 but the semi-insulating material is replaced by a SiC substrate. The Silicon Carbide has much better thermal conductivity than Silicon but is difficult to fabricate and expensive compared with Silicon [37]. The gate is
made of Ni/Au and can be either rectangular or mushroom shaped to decrease its resistance and hence improve the noise figure of the device [20-21].

![Diagram of AlGaN/InGaN pHEMT epitaxial layer structure](image)

Figure 2.3: AlGaN/InGaN pHEMT epitaxial layer structure [37]

The epitaxial layer compositions for basic GaAs based and GaN based pHEMTs devices compared with those of HEMTs is shown in table 2.1.

<table>
<thead>
<tr>
<th>Device Layer</th>
<th>HEMT</th>
<th>pHEMT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ohmic contact</td>
<td>n⁺ GaAs</td>
<td>n⁺ GaAs</td>
</tr>
<tr>
<td>Schottky contact</td>
<td>n AlGaAs</td>
<td>n AlGaAs</td>
</tr>
<tr>
<td>Supply layer</td>
<td>n⁺ AlGaAs</td>
<td>n⁺ AlGaAs</td>
</tr>
<tr>
<td>Spacer layer</td>
<td>Undoped AlGaAs</td>
<td>Undoped AlGaAs</td>
</tr>
<tr>
<td>Channel layer</td>
<td>Undoped GaAs</td>
<td>Undoped InGaAs</td>
</tr>
<tr>
<td>Buffer</td>
<td>p⁺ GaAs</td>
<td>p⁺ GaAs</td>
</tr>
<tr>
<td>Substrate</td>
<td>S.I GaAs</td>
<td>S.I GaAs</td>
</tr>
</tbody>
</table>

Table 2.1: Epitaxial layer compositions for basic HEMT and pHEMT
2.1.4 Single and Multiple Channel HEMTs

The single channel has only one channel in which the 2DEG occurs. Multiple-channel HEMT has different epitaxial layer structures than those of single channel. Two types of multiple-channel HEMT are discussed in this section. When multiple 2DEG sheets conduct in the same layer thus in one quantum well and when multiple 2DEG sheets are formed in different layers (multiple quantum wells) are depicted in figures 2.4 and 2.5 respectively [12, 14]. Multiple-channel-HEMT device delivers much higher drain current than the single channel type, because of the higher charge density due to the 2DEG in multiple quantum wells.

In terms of transconductance $g_{m}$ properties, the second structure gives much linear transconductance because of the behaviour of the 2DEG and their contribution to the current flow. On the other hand, the linearity of multiple-channel HEMT is very good because of the transconductance flat properties over certain band of the applied gate voltage. Therefore, these types are desirable in high power applications.

![Diagram of Double channel pHEMT with one quantum well](image)

Figure 2.4: Double channel pHEMT with one quantum well [12]
2.1.6 Single and Multiple Delta Doping HEMTs

Delta doping is a technique used in pHEMT devices which is not to dope the entire AlGaAs, but instead to put the dopants in a single layer. The delta doping would be formed at the interface between the supply layer n-AlGaAs and the spacer layer AlGaAs. This will prevent the electrons from escaping to the surface and reduce the parasitic resistances $R_{pgs}$ and $R_{pds}$. The former structure as shown in figure 2.6 has one of the delta doping underneath the channel and the other one above the channel while the latter structure as shown in figure 2.7 has both delta doping above the channel. The doping concentration and the place of the second delta doping are chosen to avoid parasitics.

The advantage of the former structure (figure 2.6) is that, the second delta doping (semiconductor material with higher conduction band energy) works as a barrier that keeps the electrons from escaping to the buffer layer. In this case, the transconductance profile of the device is wider over broader range of $V_{gs}$ which in turn improves the linearity of the device. Whereas, for the latter structure (figure 2.7), both delta doping layers are placed above the channel. The second delta doping is grown near the surface which in turn facilitates better gate voltage...
control and reduces the effective channel length [15] which is an added advantage for the output current and transconductance of the device. Both of the structure has advantages and disadvantages from different aspects of their application in RF and microwave field.

Figure 2.6: Multiple delta doping layers of pHEMT device one above the (InGaAs) channel and one behind the channel [15]

Figure 2.7: Multiple delta doping layers of pHEMTs device, both above the (InGaAs) channel [15]
In multiple delta doping and one channel the gate to channel thickness is a vital factor which affects the linearity of the device [17]. The carrier density is directly proportional to the number of delta doping layers. When the second delta doping is placed beneath the channel, the separation is expanded which leads to a wider transconductance \( g_m \) range but the maximum \( g_m \) value is not greatly affected because the gate no longer controls the second delta doping. However, placing the second delta doping above the channel does not improve the device linearity but improves the current and the peak value of the transconductance of the device. The conduction of the multiple delta-doping structures is much faster and consequently it gives higher output current and transconductance than the former structure.

2.1.7 Energy Band Diagram of HEMT Devices

The FET based transistors are usually negatively biased. When a positive voltage is applied between the source and drain terminals, it will create an electric field which will direct the electrons to the active channel. This electric field should give the electrons the necessary energy to transfer from the lower conduction-band to the next higher valley. As known HEMT devices have additional thin layer (quantum well) in which the electrons are directed to and trapped in. Once the electrons are confined in the 2DEG sheet they cannot escape back to supply layer. The electrons in this region are free to move and they are attracted to the interface between heterojunctions, correspondingly the electrons scattering caused by the ionized impurities is much reduced.

In this section, a summary and comparison of the electrons and energy band diagram behaviour in the previously mentioned types of HEMT devices are discussed. Figure 2.8 and 2.9 demonstrate the energy band diagram of a single-channel HEMT and pHEMTs device. Figure 2.10 demonstrates the energy band diagram of a single-channel delta doped pHEMT device. The electrons in the 2-DEG channel experience the inverted mode conduction operation for one quantum well.
Figure 2.8: Energy band diagram of single channel HEMT device [1]

Figure 2.9: Energy band diagram of single-channel pHEMT device [13]

Figure 2.10: Energy band diagram of single-channel delta-doped pHEMT device [14]
Figure 2.11 illustrates the band diagram of a double-channel pHEMT device. The electrons are better confined and the electrons concentration is greatly improved in the multiple 2DEG layers. The electrons in the 2-DEG channel experiences the normal mode conduction operation for multiple quantum wells. The delta-doping technique enhances the electrons concentration in the 2DEG layer and their mobility is higher than if the same spacer layer thickness is used without the delta doping. High carrier mobility reduces the parasitics, therefore improves the transconductance and the break down voltage with better control of the threshold voltage. Accordingly, it will amplify the linearity and minimize the noise of the device. HEMTs with gate length of 0.5 μm are expected to produce a gain of 10 dB and noise figure of (0.7 – 1 dB) [3].

Figure 2.11: Energy band diagram of double-channel HEMT (normal – mode) [14]

Figure 2.12 represents the energy band diagram of AlGaN/InGaN pHEMTs. The GaN-based HEMT device is capable of maximizing electron mobility by forming a quantum well at the heterojunction interface between the AlGaN layer and the InGaN layer. As a result, electrons are trapped in the quantum well. The trapped electrons are represented by a two-dimensional electron gas in the undoped InGaN layer. The amount of current is controlled by applying voltage to the gate electrode, which is in Schottky contact with the semiconductors so that electrons flow along the channel between the source electrode and the drain electrode.
2.2 Advantages and Disadvantages of GaN Technology

This project is based on DC, RF and temperature dependent small signal characterisation of AlGaAs/InGaAs and AlGaN/InGaN pHEMTs. So, it is necessary to study the material properties as well as the advantages and disadvantages of technology that is used in the field of RF and microwave communication devices. A variety of technologies are competing each other, such as Si lateral-diffused metal-oxide-semiconductors and bipolar junction transistors, GaAs metal-semiconductor field-effect transistors (MESFETs), GaAs heterojunction bipolar transistors, SiC MESFETs and GaN HEMTs. Compared to other competing materials, the material properties of GaN are presented in table 2.2. Wide bandgap, large breakdown electric field and high electron saturated velocity make it as an excellent candidate for RF and microwave power amplifiers. Besides RF and microwave power amplifiers, AlGaN/GaN HEMTs also exhibit the promising potential to construct digital integrated circuits (ICs), especially for the operations at high temperature that is impossible for silicon or GaAs-based technologies. The competitive advantages of GaN-based devices compared to other candidate material for a commercial product are described in table 2.3.
Table 2.2: Properties of some semiconductor materials for high power, high temperature and high frequency electronic devices [66]

<table>
<thead>
<tr>
<th>Properties</th>
<th>Si</th>
<th>GaAs</th>
<th>4H-SiC</th>
<th>GaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bandgap (eV)</td>
<td>1.11</td>
<td>1.43</td>
<td>3.26</td>
<td>3.42</td>
</tr>
<tr>
<td>Relative Dielectric Constant</td>
<td>11.8</td>
<td>12.8</td>
<td>9.7</td>
<td>9.0</td>
</tr>
<tr>
<td>Breakdown Field (V/cm)</td>
<td>2.5x10^5</td>
<td>3.5x10^5</td>
<td>35x10^5</td>
<td>35x10^5</td>
</tr>
<tr>
<td>Saturated Velocity (cm/sec)</td>
<td>1.0x10^7</td>
<td>1.0x10^7</td>
<td>2.0x10^7</td>
<td>1.5x10^7</td>
</tr>
<tr>
<td>Electron Mobility (cm^2/V-sec)</td>
<td>1350</td>
<td>6000</td>
<td>800</td>
<td>1000</td>
</tr>
<tr>
<td>Hole Mobility (cm^2/V-sec)</td>
<td>450</td>
<td>330</td>
<td>120</td>
<td>300</td>
</tr>
<tr>
<td>Thermal Conductivity (W/cm-K)</td>
<td>1.5</td>
<td>0.46</td>
<td>4.9</td>
<td>1.7</td>
</tr>
</tbody>
</table>

In table 2.3, the first column states the required performance benchmarks for any power device technology and the second column lists the enabling features of GaN-based devices that fulfil this need. The last column summarizes the resulting performance advantages at the system level and to the customer.

Table 2.3: Competitive advantages of GaN devices [20]

<table>
<thead>
<tr>
<th>Need (operation)</th>
<th>Enabling Feature</th>
<th>Performance Advantage</th>
</tr>
</thead>
<tbody>
<tr>
<td>High power density</td>
<td>Wide bandgap; High field</td>
<td>Compact ease of matching</td>
</tr>
<tr>
<td>High voltage</td>
<td>High breakdown field</td>
<td>Eliminate/Reduce step down</td>
</tr>
<tr>
<td>High linearity</td>
<td>HEMT Topology</td>
<td>Optimum band allocation</td>
</tr>
<tr>
<td>High frequency</td>
<td>High electron velocity</td>
<td>Bandwidth, m/mm-wave</td>
</tr>
<tr>
<td>High efficiency</td>
<td>High operating voltage</td>
<td>Power saving</td>
</tr>
<tr>
<td>Low noise</td>
<td>High Gain &amp; velocity</td>
<td>High dynamic range receivers</td>
</tr>
<tr>
<td>High temperature</td>
<td>Wide bandgap</td>
<td>Rugged, reduced cooling</td>
</tr>
<tr>
<td>Thermal management</td>
<td>SiC substrate</td>
<td>High power devices with reduced cooling needs</td>
</tr>
<tr>
<td>Technology leverage</td>
<td>Direct bandgap: Enable for lighting</td>
<td>Driving force for technology: Low cost</td>
</tr>
</tbody>
</table>
Among all the advantages, one of major disadvantages is of trap states in AlGaN/GaN Heterostructures [38]. These traps may appear on the AlGaN surface, in the AlGaN barrier layer at the AlGaN/GaN heterointerface, or in the GaN buffer layer, as the schematic shown in figure 2.13. Presence of trap states in AlGaN/GaN HEMTs can cause a voltage delay in device operation through trapping and de-trapping process, thereby degrading the power handling capability at high frequency.

There are two kinds of surface trap states: intrinsic surface states and defect related extrinsic surface states. The term “intrinsic” refers to the fact these states would exist in an ideally perfect surface. They correspond to solution of Schrodinger equation with energy levels within the forbidden gap. The extrinsic surface states are caused by defects or impurities at the surface, forming during crystal growth or in subsequent device fabrication processes. Similar to the case of interface states, interruption of the periodicity of the crystal lattice at the heterointerface forms interface states. Interface states can also be induced by interface roughness and compositional non-uniformities [38].

Figure 2.13: Cross-sectional view of AlGaN/InGaN pHEMT showing possible locations of traps [38]
In lack of a suitable substrate, GaN and GaN-based alloys are usually grown on sapphire or SiC with large lattice mismatch. Consequently, AlGaN/GaN epilayers grown with presently available technology are imperfect crystals with dislocations, impurities, and defects in the material. These defects may cause the formation of deep level trap states within the GaN and AlGaN layer.

2.3 Semiconductor Principle

Electronically, three types of solid materials exist: insulators, metals, semiconductors which can be differentiated from the other by its band-gap value and the atomic number associated with the specific material. The band-gap is the energy difference between the valence band edge and the conduction band edge. Electrons in the valence band participate in bonding; electrons in the conduction band participate in conduction. No electrons or holes are allowed to exist in the forbidden band-gap unless an energy level is created through the doping process of the material. The band-gap is a function of temperature [4]:

$$E_g(T) = E_0 - \frac{\alpha T^2}{(T+\beta)}$$

(2.1)

where, $E_0$ is the absolute value of the energy band-gap (= 1.519 eV for GaAs), $\beta$ is a curve fitting factor (= 204K for GaAs), and $\alpha$ is also a curve fitting factor (= 5.405x10^{-4} eV / K). It is the ability to change the doping in semiconductors which radically alters the electronic properties of semiconductors.

2.3.1 Doping Semiconductor Materials

The doping process, the addition of impurities, alters the electronic characteristics of a semiconductor. Two types of doping may be achieved: negative or n-type and positive or p-type. Silicon has a valence of four, boron is a p-type donor because it has three valence electrons; arsenic is an n-type donor because it has five valence electrons. Gallium Arsenide is slightly different; the Gallium ions will be negative and surrounded by positive arsenic or vice versa. An isotope of Silicon, Si^{29}, is an
n-type donor for GaAs. When donor atoms are added to the semiconductor, they create new energy levels near the conduction band. When the donor atom is ionized, it is positively charged. Acceptor atoms grab electrons from the valence band, creating holes. The ionized acceptor is negatively charged [6].

2.3.2 Mobility

Mobility describes how fast an electron moves under an applied electric field:

\[ v = \mu E \]  \hspace{1cm} (2.2)

Here, \( v \) indicates the drift velocity, \( \mu \) is the carrier mobility, and \( E \) is the applied electric field. The semiconductor drift-velocity is linear with the electric-field if the drift-velocity is small compared to the thermal velocity. As the electric-field is increased, the drift-velocity departs from this linear relationship. The drift-velocity starts to decrease and eventually saturates [1, 2]. It can be approximated by

\[ v(E) = \frac{\mu E}{1 + \frac{\mu E}{v_{\text{sat}}}} \]  \hspace{1cm} (2.3)

Where \( v_{\text{sat}} \) the saturation velocity.

2.3.3 Fermi Level

The Fermi level represents the energy at which the probability of finding an electron is 0.5. The probability of an electron occupying an allowed energy level is provided by the Fermi Dirac distribution function, \( F(E) \) is given by,

\[ F(E) = \frac{1}{1 + \exp \left( \frac{E - E_F}{kT} \right)} \]  \hspace{1cm} (2.4)

Where, \( E_F \) is the Fermi level, \( E \) is the energy in question, \( k \) is Boltzmann’s constant, and \( T \) is the absolute temperature. If donor atoms are introduced, the Fermi level rises above the middle of the band-gap because there are more
electrons present in the conduction band. If acceptor atoms are introduced, the Fermi level decreases because there are more holes in the valence band which decreases the energy level [2].

### 2.3.4 Schottky Diode Concept

A metal in contact with a semiconductor forms a rectifying contact called a Schottky Diode. The difference between the vacuum level and the Fermi energy is the work function. The vacuum level is the energy at which the electrons are no longer bound to the atom. The electron affinity is the difference between the conduction band edge of the semiconductor and the vacuum level. The barrier height is the difference between the metal work function and the electron affinity of the semiconductor. The formula for the barrier height, expressed as $\Phi_b$, is given by the equation below:

$$q\Phi_b = q(\Phi_m - \chi)$$  \hspace{1cm} (2.5)

Where $q$ is the electron charge, $\Phi_b$ is the barrier height, $\Phi_m$ is the metal work function, and $\chi$ is the electron affinity of the semiconductor. When a reverse bias is applied the barrier height increases until no electrons can escape to the opposite direction of the heterojunction. The diode current experience an exponential behaviour as follows [1].

$$I = I_0 e^{\frac{qV}{nKT}}$$

$$I_0 = S \pi^{**2} T^2 \exp \left( -\frac{q\Phi_b}{KT} \right)$$  \hspace{1cm} (2.7)

Where $I_0$ is the reverse saturation current in the dark, $q$ is the electron charge of $1.6\times10^{-19}$C, V is the applied bias, n is the ideality factor, K is Boltzman constant equal to $1.23 \times 10^{-23}$ m².kg.s⁻².K⁻¹, T is the room temperature of $300K$, $A^{**}$ is the effective Richardson Constant = 8.64 A/ cm²/ K² for Au/Pt/Ti Schottky contacts with GaAs [18-19] and 26 A/ cm²/ K² for Au, Ni, Pt Schottky contacts with GaN devices [10], S is the Schottky diode area = $L_y \times W_y$ [2]. The barrier height is an
important factor which affects the electrical and transfer properties of the schottky diodes. After taking the natural logarithm (ln) of both sides of equation (2.7) and rearranging the parameters, the barrier height $\phi_b$ is

$$\phi_b = \frac{KT}{q} \ln \left( \frac{SA"T}{I_0} \right) \quad (2.8)$$

The ideality factor $n$ is a comparative element to the operation of an ideal diode [1]. Therefore, the ideally the ideality factor should be 1. When $V$ is greater than $3kT/q$, the current in equation (2.6) becomes

$$I = I_0 e^{qV/kT} \quad (2.9)$$

After taking the natural logarithm of both sides of equation (2.9) and rearranging the parameters, the ideality factor expression becomes,

$$n = \frac{q \Delta V}{kT \Delta (\ln I)} \quad (2.10)$$

### 2.4 DC Characteristics of pHEMTs

The operation of a pHEMT in this manner is very similar to the operation of a MESFET. Figure 2.14 shows the operation of an n-type depletion-mode MESFET under common source configuration.

![Figure 2.14 Cross-sectional view of a GaAs MESFET under common source configuration][3]
The gate is used as the input and is reverse bias and the drain is used as the output and forward bias. A depletion region under the gate semiconductor Schottky barrier is formed, due to reverse bias. This depletion region will have a rectifying effect on the electron transport along the channel which flows from the source to the drain end. It is clear that, if the gate voltage is fixed, as the drain voltage increases, more current will flow through. That is why, initially, for small drain voltage, the MESFET behaves like a resistor. However, as the potential at the drain end is increased, the depletion width closer to the drain end will become larger; a point will be reached when the channel could accommodate the maximum velocity of the electrons. As this happens, the current starts to saturate.

For long channel (gate length \( L_g \gg y \)), based on constant low field mobility and gradual channel approximation, the current \( I_{ds} \) is given as [3]:

\[
I_{ds} = (\text{Channel area}) \times (\text{charge density}) \times (\text{mobility}) \times (\text{field})
\]

\[
I_{ds} = Z[Y-d(x)]qN_d\mu dV dX
\]

(2.11)

where, \( Z \) is the gate width, \( Y \) is the channel depth, \( d(x) \) is the depletion width and \( N_d \) is the doping concentration, \( d(x) \) is the depletion width, is given by [3]:

\[
d(x) = \left\{\frac{2\varepsilon_s[V(x)+V_{bi}-V_{gs}]}{qN_d}\right\}^{1/2}
\]

(2.12)

where \( \varepsilon_s = \varepsilon_o\varepsilon_r \) is the semiconductor dielectric constant, \( V_{bi} \) the built-in potential. Substituting equation (2.12) into equation (2.11) yields

\[
I_{ds} = G_0 \left\{V_{ds} - \frac{2[(V_{ds}+V_{bi}-V_{gs})]^3 - (V_{bi}-V_{gs})^3]}{3V_p^2}\right\}
\]

(2.13)

where \( G_0 \), the channel conductance and is given by [3]:

\[
G_0 = \frac{q\mu N_d ZY}{L}
\]

(2.14)
and $V_p$, the pinch-off voltage when the depletion width $d(x)$ equals the channel depth $Y$, is [3]:

$$V_p = \frac{qN_d Y^2}{2\varepsilon_s}$$  \hspace{1cm} (2.15)

On the other hand, for short channel MESFET (small $L_g/Y$ ratio); the $I_{ds\ (sat)}$ can be approximated as [3]:

$$I_{ds\ (sat)} \approx Z[Y-d]qN_d V_{sat}$$  \hspace{1cm} (2.16)

where $V_{sat}$ is the saturation velocity and the intrinsic transconductance $g_m$ is [1],

$$g_m = \left. \frac{\partial I_{ds}}{\partial V_{gs}} \right|_{V_{ds}=\text{const.}}$$  \hspace{1cm} (2.17)

$$g_m = \frac{\varepsilon Z V_{sat}}{d}$$  \hspace{1cm} (2.18)

A typical DC characteristic of a pHEMT can be seen in figure 2.15 and 2.16.

![Graph](image-url)

**Figure 2.15**: The output characteristics of 0.5x120\mu m^2 AlGaAs/InGaAs pHEMT
The transconductance $g_m$ properties are very important for pHEMTs functions as they give an indication of how good or bad the linearity and the speed of the device [3]. The transconductance $g_m$ is the change of the output current $I_{ds}$ in response to the change of input voltage $V_{gs}$ at a constant output voltage $V_{ds}$. The intrinsic transconductance $g_m$ is directly proportional to the gate width and inversely proportional to the gate length.

The output conductance $g_{ds}$ is the change in the output current $I_{ds}$ with a change in the output voltage $V_{ds}$ at a constant input voltage $V_{gs}$. It is inversely proportional to the gate length. The output conductance expression is,

$$g_{ds} = \frac{\partial I_{ds}}{\partial V_{gs}} \bigg|_{V_{gs} = \text{const.}}$$  \hspace{1cm} (2.19)

$$g_{ds} = -\frac{\varepsilon g Z V_{sat}}{d}$$  \hspace{1cm} (2.20)

In the saturation region the transconductance is affected by one factor which is $R_s$ shown in figure 2.17, which yields the relation between the extrinsic transconductance $g'_m$ and the intrinsic transconductance $g_m$.
The ideal small-signal equivalent circuit is shown in figure 2.17 (a). The small-signal drain current is then:

\[ I_{ds} = g_m V_{gs} \]  

(2.21)

This is a function only of the transconductance and the input-signal voltage. The effect of the source series resistance can be determined using figure 2.17 (b).

\[ I_{ds} = g_m V'_{gs} \]  

(2.22)

The relation between \( V_{gs} \) and \( V'_{gs} \) can be found from

\[ V_{gs} = V'_{gs} + g_m V_{gs} R_s = (1 + g_m R_s) V'_{gs} \]

\[ V_{gs}' = V_{gs} \frac{1}{1 + g_m R_s} \]  

(2.23)

From this relation we get

\[ I_{ds} = g_m V'_{gs} = \left( \frac{g_m}{1 + g_m R_s} \right) V_{gs} \]  

(2.24)

By applying the definition \( (dI_{ds}/dV_{gs}) \) extrinsic transconductance becomes [4],

\[ g'_m = \frac{g_m}{1 + g_m R_s} \]  

(2.25)

If \( R_s \) is zero, the extrinsic and intrinsic transconductance will be the same value.
2.5 RF Characteristics of pHEMTs

The RF characteristics include measuring the scattering parameters (S – parameters) of the device under test in order to extract small signal circuit parameters. Then, they are used to calculate the cut-off frequency \( f_t \) and the maximum frequency of oscillation \( f_{\text{max}} \).

2.5.1 Small Signal Circuit Parameters Approach

**The Current Gain:**

The current gain frequency (Cut-off frequency) is greatly affected by the doping concentration and carries velocity in the 2DEG sheet. The point where the input current \( i_{\text{in}} = 2 \pi f_t (C_{gs} + C_{gd}) v_s \) passes through \( (C_{gs} + C_{gd}) \) is equal to output current \( i_{\text{out}} \) of \( [g_m V_g] \), happens at a certain frequency which is known as the current gain frequency \( f_t \). It can be calculated as follows [2],

\[
 f_t = \frac{1}{2 \pi \tau} = \frac{g_m}{2 \pi (C_{gs} + C_{gd})}
\]

Where \( \tau = \frac{L}{v_s} \) and L is the depletion region width, \( v_s \) the electrons saturation velocity.

**Unity Power Gain:**

Maximum frequency of oscillation or unity power gain frequency can be maximised by the same factors as in the cut-off frequency and additional other factors like obtaining maximum \( R_i/R_{ds} \) but minimal gate resistance \( R_g \), minimal source resistance \( R_d \), and small feedback capacitance \( C_{gs} \). When the unilateral gain is approximated by \( U = \left( \frac{f_{\text{max}}}{f_t} \right)^2 \), then the maximum frequency of oscillation can be calculated from the following [1, 2],

\[
 f_{\text{max}} = \frac{f_t}{2 \sqrt{(f_t + f_t \tau)}}
\]
Where $r_1$ is the input to output resistance ratio time constant $= (R_g + R_i + R_s)/R_{ds}$, $\tau$ is the time constant $= 2\pi R_g C_{gd}$ and $R_i$ is the internal resistance. The gate resistance can be minimized with two-fingered gate approach as this will reduce the gate length $l_g$ and consequently reduce the internal capacitance of the device and improve $g_m$.

- **RF Transconductance:**

Another approach can be used to calculate the transconductance $g_m$ at radio frequencies (RF). The transconductance at RF is a little different (higher in pHEMTs) from the DC transconductance. If the device is a low noise device and $\text{Re } (Y_{21}) >> \text{Im } (Y_{21})$ along with $\omega R_i C_{gs} \approx 0.01$ and $\omega C_{gd} \approx 0.001$ [5]. Then the RF transconductance can be calculated as follows:

$$g_m = \text{Re}[Y_{21}]$$ (2.28)

The RF $g_m$ maximum value is different form DC $g_m$ according to the following reasons of self heating and trapping effects. The former reduces the DC $g_m$ and the latter reduces the RF $g_m$. The RF $g_m$ is higher than the DC $g_m$ with HEMT devices. According to RF conditions the device is under fast sweep and the traps are at their highest electron velocity because of the 2DEG phenomena. So the electrons would take usually longer time to start to decline their saturation velocity as long as the output current is modulated by the gate voltage [16].

**2.5.2 Scattering Parameters Approach**

- **The Current Gain:**

In Microwave frequency mode, the S-parameters need to be characterized at these high frequencies. The current gain (cut-off) frequency derivation starts from converting the ABCD parameters to h-parameters, then converting h-parameters to S-parameters as follows [8]: The ABCD parameters for two port networks are,
When \( I_2 = 0 \), then the parameters from expression (2.29) become,

\[
A = \frac{V_1}{V_2} \bigg|_{V_2 = 0} \quad \text{and} \quad C = \frac{I_1}{I_2} \bigg|_{I_2 = 0}
\]

When \( V_2 = 0 \), then the parameters from expression (2.29) become,

\[
B = \frac{V_1}{I_2} \bigg|_{V_2 = 0} \quad \text{and} \quad D = \frac{I_1}{I_2} \bigg|_{V_2 = 0}
\]

The equivalent \( h \)-parameters are,

\[
\begin{bmatrix} V_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ V_2 \end{bmatrix}
\]

When \( I_1 = 0 \), then the parameters from expression (2.32) are,

\[
h_{12} = \frac{V_1}{V_2} \bigg|_{I_1 = 0} \quad \text{and} \quad h_{22} = \frac{I_2}{V_2} \bigg|_{I_1 = 0}
\]

When \( V_2 = 0 \),

\[
h_{11} = \frac{V_1}{I_1} \bigg|_{V_2 = 0} \quad \text{and} \quad h_{21} = \frac{I_2}{I_1} \bigg|_{V_2 = 0}
\]

As it can be seen from (2.31) and (2.34), the current gain is,

\[
h_{21} = \frac{1}{D}
\]

The D parameter from ABCD parameters conversion to S-parameters is,

\[
D = \frac{(1-S_{11})(1+S_{22}) + S_{12}S_{21}}{-2S_{21}}
\]

The current gain \( h_{21} \) is

\[
|h_{21}| = \left| \frac{I_0}{I_{in}} \right| = \left| \frac{-2S_{21}}{(1-S_{11})(1+S_{22}) + S_{12}S_{21}} \right|
\]

The cut-off frequency can be extracted from the current gain slope extrapolation as the current gain will reduce by -20dB/ decade when the frequency increases.
Unity Power Gain:

The maximum frequency of oscillation $f_{\text{max}}$ can be extracted by two possible terms. The maximum frequency of oscillation $f_{\text{max}}$ can be extracted either from the unilateral gain (U) or from the maximum available gain (MAG). It was seen that, from the project’s experiments, both terms gave very close values of $f_{\text{max}}$. That’s why both U and MAG can be used to extract $f_{\text{max}}$. Originally, the transducer gain ($G_T$) which is the ratio between the maximum power delivered to the output load and the maximum power delivered to the input source load. $G_T$ is defined by the following expression [33],

$$G_T = \frac{|S_{21}|^2 (1 - |\Gamma_S|^2)(1 - |\Gamma_L|^2)}{|(1 - S_{11} |\Gamma_S|^2)(1 - S_{11} |\Gamma_L|^2) - \Gamma_L \Gamma_S S_{12} S_{21}|^2}$$  \hspace{1cm} (2.38)

Where $\Gamma_s$ and $\Gamma_L$ are the source and load reflection coefficients. The maximum unilateral transducer gain ($G_{\text{TUmax}}$) is achieved when the conjugate source reflection coefficient ($\Gamma^*$) is equal to reflection at the input ($S'_{11}$) and similarly when $\Gamma^*_L$ is equal to ($S'_{22}$) [32]. When $S_{21}$ is assumed to equal 0 (no reflection from the output to the input) along with $\Gamma^*_S = S'_{11}$ and $\Gamma^*_L = S'_{22}$, the maximum unilateral transducer gain becomes [32],

$$U = \frac{|S_{21}|^2}{(1 - |S_{11}|^2)(1 - |S_{22}|^2)}$$  \hspace{1cm} (2.39)

The stability factor $K$ is used to see if the device is going to oscillate when the load and source impedances are connected to the device with no feedback [2]. When $K$ is greater than 1 the device (transistor), is said to be unconditionally stable and vice versa. The stability factor $K$ is:

$$K = \frac{1 + |S_{11} S_{22} - S_{12} S_{21}|^2 - |S_{11}|^2 - |S_{22}|^2}{2 |S_{21}| |S_{12}|}$$  \hspace{1cm} (2.40)

Maximum Stable Gain MSG is used when the device is conditionally stable (when $K < 1$). Maximum Stable Gain (MSG) is [32],
Maximum available gain (MAG) is used when the device is unconditionally stable and $K > 1$. MAG is the maximum gain of the transistor with no external feedback. It can be used to extract $f_{\text{max}}$ from the maximum available gain slope of -20 dB/decade and its intersection with the frequency axis. The Maximum Available Gain (MAG) is as follows [33],

$$\text{MAG} = 10 \times \log \left( \frac{|S_{21}|}{|S_{12}|} \right) + 10 \times \log \left| K \pm \sqrt{K^2 - 1} \right|$$  \hspace{1cm} (2.42)

### 2.6 Small Signal Analysis

The small signal circuit parameters of pHEMTs are the same as in a FET device. The small signal circuit of typical FET devices (including MESFETs and HEMTs) is shown in figure 2.18. The physical meaning of each parameter will be explained in this section as per reference [23-29].

**Figure 2.18: Small signal circuit parameters of FET devices [3]**

- Here $C_{pg}$, $C_{pd}$, $L_g$, $L_d$, $L_s$, $R_g$, $R_d$ and $R_s$ are extrinsic parameters and sometimes called parasitics. They are bias-independent and should remain constant for different biasing.
C_{pg} and C_{pd} are the parasitic capacitances that are mainly made up of the sum of capacitances formed between the gate and drain contact pads to the ground.

L_g, L_d and L_s are inductances of the three contacts. Dimensions and geometries of the source/drain pads and gate fingers are the most contributing factors to C_{pg}, C_{pd} and L_g, L_d, L_s, R_g, R_d and R_s are the resistances associated to the three terminals. Not only the metallisation contacts but also the semiconductor contact resistances and bulk resistances will contribute the overall R_s and R_d.

The intrinsic parameters are C_{gs}, C_{gd}, C_{ds}, R_i, g_{ds}, g_m and τ.

C_{gs} and C_{gd} are capacitances associated with the depletion region underneath the gate, as the bias changes the width of the depletion region, C_{gs} and C_{gd} will increase or decrease accordingly. C_{ds} is attributed to the substrate current; the substrate current can be seen as a leakage current from the main channel current and will contribute as a loss. The material used for the substrate will affect the value of the C_{ds}.

R_i is the channel resistance, measuring how difficult the electrons flow in the channel and is apparently to do with the bias. It is included primarily to improve the match to S_{11}. The output conductance of the device is g_{ds} which is the inverse value of R_{ds}, is the drain to source conductance/resistance, it is again a parameter related to the substrate current and the material used for the substrate.

g_m is the transconductance, indicating how much change in output current from a change of a given input voltage, can represent the gain of the device.

Lastly, τ represents the time delay for the output current to be generated with the given input voltage. The transconductance takes some time to charge after applying the gate voltage which defines term time delay (τ).
Equations that can be used to calculate or evaluate these parameters values of the equivalent circuit following the technology are tabulated in table 2.4 [3].

Table 2.4 Relationships of small-signal parameters to the physical properties of FET [3]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Comment</th>
<th>Equation</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{\text{contact}}$</td>
<td>Contact resistance</td>
<td>$\frac{1}{Z} \sqrt{\frac{\rho_c}{q\mu N_d Y}}$</td>
</tr>
<tr>
<td>$R_{SG}$</td>
<td>Bulk resistance $R_{SG} = R_{\text{contact}} + R_{SG}$</td>
<td>$\frac{L_{SG}}{q\mu N_d YZ}$</td>
</tr>
<tr>
<td>$L_{SG}$ is the distance between drain and gate contact.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_{GD}$</td>
<td>Bulk resistance $R_{GD} = R_{\text{contact}} + R_{GD}$</td>
<td>$\frac{L_{GD}}{q\mu N_d YZ}$</td>
</tr>
<tr>
<td>$L_{GD}$ is the distance between drain and gate contact.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_g$</td>
<td>Gate series resistance; $m =$ number of gate strips</td>
<td>$\frac{\rho Z}{3m^2 h \lambda}$</td>
</tr>
<tr>
<td>$C_{gs}$</td>
<td>Gate-Source capacitance</td>
<td>$\frac{\varepsilon Z L}{d} \left( 1 + \frac{X}{2L} \frac{2d}{L+2X} \right)$</td>
</tr>
<tr>
<td>$C_{gd}$</td>
<td>Gate-Drain capacitance</td>
<td>$\frac{2\varepsilon Z}{1+\frac{2X}{L}}$</td>
</tr>
<tr>
<td>$R_i$</td>
<td>Input resistance; $\mu$ is the low field mobility</td>
<td>$\frac{V_{\text{sat}} L}{\mu I_{ds}}$</td>
</tr>
<tr>
<td>$g_{gm}$</td>
<td>Intrinsic transconductance</td>
<td>$\frac{\varepsilon Z V_{\text{sat}}}{d}$</td>
</tr>
<tr>
<td>$\tau$</td>
<td>Signal delay</td>
<td>$\frac{1}{V_{\text{sat}}} \left( \frac{X}{2} - \frac{2d}{1+\frac{2X}{L}} \right)$</td>
</tr>
<tr>
<td>$d$</td>
<td>Depletion width</td>
<td>$\sqrt[\frac{1}{7}]{\frac{2\varepsilon_s (V_{bi} + V_{SG})}{qN_d}}$</td>
</tr>
<tr>
<td>$X$</td>
<td>Depletion extension toward the drain End</td>
<td>$\sqrt[\frac{1}{7}]{\frac{2\varepsilon_s}{qN_d (V_{bi} + V_{SG})}} (V_{bi} + V_{DG})$</td>
</tr>
<tr>
<td>$I_{ds}$</td>
<td>Saturated drain-Source current</td>
<td>$I_{ds} = Z[Y-d]qN_d V_{\text{sat}}$</td>
</tr>
</tbody>
</table>
2.7 Temperature Characterisation

There are mainly two important reasons to have a good knowledge of the thermal characteristics of GaAs or GaN devices. First is that electrical performance of a GaAs or GaN device is a function of temperature. The temperature dependent parameters include gain, efficiency, output power, phase shift and many more. The second reason is to have an accurate prediction of the device reliability. [30-31]. The most significant temperature dependent properties are band-gap of the material, electron saturation velocity, electron mobility, built-in potential and barrier height of the material, dielectric constants and specific contact resistance.

The band-gap energy can be expressed as from equation (1.2) [7, 11]

\[ E_g(T) = E_{gap}(T_0) - \frac{\alpha T^2}{(T+\beta)} \] (2.43)

The electron saturation velocity can be expressed as [7, 10]

\[ V_{sat}(T) = V_{sat}(T_0) [1 + B_{vsat}(T-T_0)] \] (2.44)

where \( B_{vsat} \) is between -1 and -2.5 x 10\(^{-3}\)/\(^\circ\)C. The change in the Schottky barrier height and surface potential with temperature can be expressed as:

\[ V_{bi}(T) = V_{bi}(T_0) + m[E_{gap}(T) - E_{gap}(T_0)] \] (2.45)

where \( m \) is between 0 and 1. Both dielectric constants \( (X = \varepsilon) \) and specific contact resistance \( (X = \rho_c) \) can be expressed as:

\[ X(T) = X(T_0) + [1 + B_X(T-T_0)] \] (2.46)

where \( B_{\varepsilon} = 10^{-4}/\circ\)C and \( B_{\rho_c} \) will be determined by measurements. Temperature will have different influence on the physical parameters. In this work, one of the objectives is to develop a temperature dependent small-signal model. It is observed that, apart from some extreme heat or cold, for a certain temperature range, all
the equivalent circuit parameters (ECPs), like those fundamental physical parameters mentioned above, will exhibit a linear temperature dependent relationship [7, 11]. They can be expressed as:

$$P(T) = P(T_0)[1 + B(T - T_0)]$$  \hspace{1cm} (2.47)

Where

- $B$ is the temperature coefficient (TC) in units per degree;
- $T_0$ is the reference temperature in $0^\circ C$, and
- $P(T_0)$ is the value of the parameter at the reference temperature.
CHAPTER THREE: EXPERIMENTAL TECHNIQUES

3.1 S-Parameter Measurement

The S-parameters for a two-port network are defined using the reflected or emanating waves, $b_1$ and $b_2$, as the dependent variables; and the incident waves, $a_1$ and $a_2$, as the independent variables. The general equations for these waves as a function of the S-parameters are also shown in figure 3.1.

\[
\begin{bmatrix}
  b_1 \\
  b_2
\end{bmatrix} =
\begin{bmatrix}
  S_{11} & S_{12} \\
  S_{21} & S_{22}
\end{bmatrix}
\begin{bmatrix}
  a_1 \\
  a_2
\end{bmatrix}
\]

Figure 3.1: Definition of a two-port S-parameter network

Using these equations, the individual S-parameters can be determined by taking the ratio of the reflected or transmitted wave to the incident wave with a perfect termination placed at the output ($S_{11}$, $S_{12}$, $S_{21}$ and $S_{22}$). These four S-parameters completely define the two-port network characteristics. One of the main advantages of describing electrical functions in S-parameters is because of the fact that voltages and currents at high frequency are very hard to be quantified and described correctly. RF and microwave networks are often characterized using S-parameters. The S-parameters of a network provide a clear physical interpretation of the transmission and reflection performance of the device. On-wafer measurement provides the designers a useful platform to perform fast, repeatable and accurate frequency domain measurements without packaging the devices.
3.2 On-Wafer RF and DC Measurements Setup

Basically, the small-signal RF characterization is performed on devices by measuring the scattering parameters (S-parameters) at high frequencies. The configuration of the S-parameters measurements is shown in figure 3.2, which consists of a two-port vector network analyzer (VNA) and a DC bias source. The measuring system is controlled by a PC running Agilent® IC-CAP software. The bias point and measuring frequencies can all be set via the software.

On-wafer DC and RF measurements are carried out providing a fast, accurate and repeatable way of characterising the devices. Agilent’s Vector Network Analyser (VNA) HP85107A, DC source HP4142B, Cascade Microtech probe stations and Ground-Signal-Ground (GSG) probes are all hooked up together to perform the measurement tasks. A VNA measures vector ratios of reflected or transmitted energy to energy incident upon the device-under-test (DUT). The VNA is capable of RF S-parameter measurements up to 110 GHz in frequency domain. DC control and biasing are provided by the HP4142B DC source. The On-wafer measurement setup showing the HP 85107A VNA, H 4142B DC source, probe station and wafer chuck is depicted in figure 3.3.
Figure 3.3: On-wafer measurement setup showing the HP 85107A VNA, H 4142B DC source, probe station and wafer chuck

Investigated On-wafer measurement of pHEMTs device in this work is represented for the 2x100x0.5 μm² AlGaAs/InGaAs and 4x50x0.15 μm² AlGaN/InGaN pHEMTs under test using Vector Network Analyzer (VNA) with probes of 150μm pitch size are depicted in figure 3.4. The measurements start by putting the sample-on-wafer on the probe station after calibrating the probes.

Figure 3.4: Micrographs of the 2x100x0.5 μm² AlGaAs/InGaAs and 4x50x0.15 μm² AlGaN/InGaN pHEMTs under test with probes of 150μm pitch size
3.2.1 Calibration Techniques

Parasitics are well known errors associated with RF measurements. It exists in interconnects like cables, wires, probing tips and etc. The parasitic inductances, resistances and capacitances have to be removed in order to have accurate reading of measurement. Moreover, so often, phase reference planes have to be realigned to the edge of the device under test (DUT) instead of the contact points of VNA. It is therefore, a careful calibration has to be carried out to eliminate the unwanted parasitic effects [11, 71]. A Line-Reflect-Reflect-Match (LRRM) advanced calibration method is used in this work and the calibration standard is provided by the probes manufacturer, Cascade Microtech. The associated calibration software, WinCal, is installed in a PC and can be hence controlled by the user [34]. An illustration of the calibration standard used in the LRRM calibration method is presented in figure 3.5. As required, open, short, load and thru standards are needed to have proper calibration. The through-line delay and DC resistance of matched load needs to be specified during the calibration process. Temperature study and measurements, for each measured temperature; calibration is carried out every time after the temperature stabilising period of half an hour.

![Figure 3.5: Layout of the GSG probes and calibration standards for LRRM method: GSG probes open standard, through standard, short standard and load standard [34]](image-url)
The LRRM technique is an integral feature of Cascade Microtech’s WinCal VNA calibration software (figure 3.6). The VNA measures the characteristics of the device connected to the measurement reference plane. The calibration is said to be good only when the plot of $S_{11}$ is well within ±0.10 dB as shown in figure 3.7. After the calibration, measurements may be taken from WinCal, or directly from the VNA.

Figure 3.6: Snapshot of the user’s surface of Microtech’s WinCal

Figure 3.7: Magnitude of $S_{11}$ versus frequency showing a good calibration of $S$-parameter measurements (±0.05 dB of error)
3.2.2 Temperature Dependant Measurement

Temperature control equipment is needed to perform measurements covering several temperatures over a broad range. The specific temperature of the device is introduced by means of creating an ambient temperature through the wafer chuck. A temperature stabilising period is required to have accurate measurement. This is normally done by leaving the wafer in the temperature control chamber for more than 30 minutes. A Temtronic TP03200A temperature control unit together with the temperature control wafer chuck are integrated with the VNA in this work. The equipment provides an accuracy of ±2°C.

Stage I: Air flow device

- Put your sample and then switch on the air flow box (on the wall). Check the air flow gauge (put it: Usually between 3 & 4). The air flow is needed when cold temperature is used. Leave it for 30 min.

![Air Flow Device](image)

Figure 3.8: Air flow device to control air flow and gauge (Between 3 & 4)

- Ice is formed when reducing the temperature increase the air flow gauge and wait for 30 min. every time it is needed to change the air flow gauge leave the machine for 30 min (when ice is formed it shown cloudy milky layer).
Stage II: Thermal device

- Figure 3.9 represents the temperature controlled wafer chuck and the temperature control unit. Switch on the thermal box (Temptronic TP03200A). It takes about 6 min to start up. It will be set on 40°C. This is the temperature that doesn’t need the fridge.

- Set the temperature you need. It is easier to choose from the already set temperatures. For calibration purposes. Position the probes close to your sample but not too close.

- Leave for 30 min. in order for the sample and the probes to be at the required temperature.

- Make sure to lift the probes when moving to the calibration substrate. As the substrate might be in a different level and when moving the probes it will damage the probes if they were to hit the surfaces.

- After positioning the probe on the calibration substrate, do the calibration very quickly, (max: 5-10 min), if longer the temperature of probes will change.

- Note: every time to change the temperature repeat stage 3 to 5.

![Figure 3.9: The temperature control equipment: Temptronic TP03200A temperature controller and temperature controlled wafer chuck](image-url)
Figure 3.10: GSSG probe of 150μm pitch size, probes on wafer and vertical probe view

The figure above (3.10) represents GSSG 150μm pitch size infinity probe placed on wafer with thermocouple. The GSSG 150 is an ideal match for device characterization and modelling and differential applications, with industry-leading performance providing extremely low contact resistance on pads with unsurpassed RF measurement accuracy for highly reliable, repeatable measurements which is designed for on-wafer/planar surface work only.

Stage III: Switching off

- Before switching off change the temperature to 40°C, then leave for 15 min, don’t open the chuck straight away. If do so, water will be formed as the sample and the atmosphere is cold. Make sure to wait for 15min. Switch off the thermal box then move to the air flow box. Reduce the air flow gauge to 0. Then switch off.
3.3 CAD Software

Agilent’s Integrated Circuit Characterization and Analysis Program (IC-CAP) and Advanced Design System (ADS) is used to fully characterise the devices.

3.3.1 Integrated Circuit Characterization and Analysis Program

Agilent’s Integrated Circuit Characterization and Analysis Program (IC-CAP) is powerful commercial software specialising in DC and RF semiconductor device modelling. It extracts accurate compact models for various applications, such as high speed/digital, analogue and power RF applications. Device technologies like silicon CMOS, Bipolar, III-V compound gallium arsenide (GaAs), gallium nitride (GaN) and many more in the industry are using IC-CAP to perform the tasks of measurement, simulation, optimisation and statistical analysis. IC-CAP not only provides a very reliable toolkit for the required tasks, it also manages to perform all these on a single platform [35].

There are several industry standard CMOS and FET models built-in available in IC-CAP. The excellent data acquisition and handling capabilities of IC-CAP allows user to perform some huge amount of measurements, extractions and optimisations with ease. The GUI is user-friendly, with flexibility of customising own specific routines. The interactions with other instrumentations, such as DC source, Vector Network Analyser (VNA) and other Time/Frequency domain instruments are done by the GPIB interface. Results obtained from the IC-CAP have also the flexibility of several popular formats that could be easily incorporated in some of the most popular CAD software in the market. One of the key features of IC-CAP is that there is an inherently built in scripting language, Parameter Extraction Language (PEL). With this programmable language, macros which automate huge amount of tasks could be established, minimising the human interference. Fast and accurate results could thus be achieved. In this work, IC-CAP is used to perform DC, RF measurements and model parameter extractions. The procedures or routines of these measurements and extractions are later written
in macros and become automated. A typical view of the IC-CAP working environment can be seen in figure 3.11.

Figure 3.11: A schematic view of IC-CAP environment [35]

3.3.2 Parameter Extraction in IC-CAP

An appropriate model chosen for the device under investigation, in order to perform parameter extraction in IC-CAP has to be setup and configured. The required bias condition, measurement input parameters are to be configured in such a way that IC-CAP would understand and no errors to be found. Figure 3.12 shows a typical IC-CAP measurement setup. Extraction of parameter can then be achieved by manipulating the data. Usually, a set of expressions for the parameter are derived first from the theorised equivalent model, and judging from the expressions, a certain aspect of the measurement results would need to be taken and rearranged to extract the parameter. A typical procedure implemented in IC-CAP for parameter extraction is shown in figure 3.13.
After the on-wafer DC and RF S-parameter measurements are taken, the extracted parameters are then stored in IC-CAP (figure 3.14) and these data are transferred to Agilent’s Advance Design System (ADS). Advance Design System (ADS) is a circuit simulator which is totally compatible to the data formats of IC-CAP. In this work, simulation work is carried out in ADS. This is because an equivalent
circuit model is adopted for the GaAs and GaN pHEMTs. ADS is an excellent circuit schematic simulator. It provides the flexibility and ease of reference to test-bench definitions. Comparisons between developed model and raw measurement are done in ADS as well, gaining the advantage of validation on a single platform.

Figure 3.14: Parameter extraction using PEL in IC-CAP

3.3.3: Advanced Design System (ADS)

Agilent’s Advanced Design System (ADS) is useful CAD software, particularly suitable for electronic circuit simulation that allows circuit design engineers to run circuit simulations in many settings, like time or frequency domain. Its comprehensive library of electronic components and the user-friendly environment make it a vital tool for tasks such as designing, modelling, and optimization of performance for electronic device or circuit [36]. The popularity of ADS lies in the fact that it possesses a large amount of simulation models and settings for various DC, AC and RF applications and high speed digital circuits. Optimisation and tuning can also be easily achieved with its built-in functions and settings. Inherently, it provides several circuit configurations that reduce the complexity. Basic simulation procedure in ADS goes through the first step of creating the
schematic, adding stimuli such as current probes, labelling wires and pins and identifying the nodes of which to collect the data. Next, a simulation method has to be selected with required parameters specified. After that, a simulation can be carried out. Brief descriptions of the simulation types that used in this work are listed in table 3.1.

Table 3.1: Descriptions of ADS simulation types [36]

<table>
<thead>
<tr>
<th>Simulator</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC</td>
<td>Fundamental to all simulations, it performs a topology check and an analysis of the DC operating point of a circuit.</td>
</tr>
<tr>
<td>AC</td>
<td>Obtains small-signal transfer parameters, such as voltage gain, current gain, and linear noise voltage and currents. This simulator is useful in designing passive circuits and small-signal active circuits such as low-noise amplifiers (LNAs).</td>
</tr>
<tr>
<td>S-parameter</td>
<td>Provides linear S-parameters, linear noise parameters, transimpedance (Zij), and transadmittance (Yij), by linearizing the circuit about the DC operating point and performing a linear small-signal analysis that treats the circuit as a multiport. Each port is turned on sequentially. S-parameters can be converted to Y- and Z-parameters.</td>
</tr>
</tbody>
</table>

The DC simulation provides the DC operating characteristics of a circuit design. The simulator calculates the response of a circuit to a particular stimulus by solving it numerically with formulated circuit equation system. Small-signal, linear AC analysis is carried out in AC simulation in ADS and small-signal transfer parameters, such as voltage gain, current gain, transimpedance, transadmittance, and linear noise are computed. Two-port scattering parameters (S-parameters figure 3.15) simulation can also be performed in ADS, where a circuit network under investigation will be simulated and computed with the inherent formulated equations.
The result is a set of S-parameters that user can study and possibly optimise. Conversion to other 2-port parameters such as Z, Y, ABCD parameters can also be carried out in ADS. Basic simulation procedure in ADS goes through the first step of creating the schematic, adding stimulus such as current probes, labelling wires and pins and indentifying the nodes of which to collect the data. Next, a simulation method has to be selected with required parameters specified. After that, a simulation can be carried out. Most of the straight forward simulations could be done in a short time, normally in a few seconds. With the completion of the simulation, acquired results could be viewed as specified. Detailed or brief operating data could be reported as well. As plotting has been the most popular and easiest way to interpret results, a new data display window could be created with results plotted in various meaningful plots such as, logarithm S-parameters (dB/Frequency) or Smith Chart. After everything, the circuit schematic could be retuned and optimised with targets or aims specified.

Figure 3.15: ADS Schematic simulator user interface [36]
CHAPTER FOUR: RESULTS AND DISCUSSIONS

4.1 Device Physical Structure

In this project the DC and RF measurement are carried out at different temperature on GaAs pHEMT with two fingers gate of 100 μm gate widths and 0.5 μm gate lengths make it 2x100x0.50 μm² AlGaAs/InGaAs pHEMT, along with a GaN pHEMT on wafer with four fingers gate of 50 μm gate widths and 0.15 μm gate lengths making it 4x50x0.15 μm² AlGaN/InGaN pHEMT [9]. As known, GaN pHEMT composition and structure similar to the GaAs pHEMT but the semi-insulating material is replaced by a SiC substrate [37]. The cross sectional view of the 2x100x0.50 μm² AlGaAs/InGaAs and 4x50x0.15 μm² AlGaN/InGaN pHEMTs represented in figure 4.1(a) and figure 4.1(b) respectively. As the physical dimension of the device is an important factor in temperature dependent characterisation, the physical dimension of the 2x100x0.50 μm² AlGaAs/InGaAs pHEMT is 390μm x 450 μm and 4x50x0.15 μm² AlGaN/InGaN pHEMT is 395μm x 690 μm. The top view of the both pHEMTs is shown in figure 4.2.

![Cross-sectional view of the 2x100x0.50 μm² AlGaAs/InGaAs pHEMT](image-url)
4.2 Measured DC Characterisation and Results

DC characterisation of pHEMT is one of the key parameters to check device’s performance at room temperature. Three main parameters and their interdependence are usually verified with this kind of measurements. As a rule, pHEMT performance is checked for DC, a measurement that is I-V characteristics which is a regular I-V plot represents drain - source ($I_{ds}$) current as a function of applied gate - source ($V_{gs}$) with drain - source voltages ($V_{ds}$). The interesting characterisation of pHEMT in terms of DC is its transfer characteristics that is drain – source($I_{ds}$) current as a function of gate - source voltage ($V_{gs}$) and transconductance ($g_{m}$) which is defined in fact as derivative of transfer characteristics.
4.2.1 The Output Characteristics

The output characteristics of the 2x100x0.50 μm² AlGaAs/InGaAs pHEMT is depicted on figure 4.3 (a) and the drain current and gate current against drain voltage is depicted in figure 4.3 (b) respectively. All parameters have been measured in this section at room temperature and with probes of 150 μm pitch size. The output current of the 2x100x0.5 μm² GaAs pHEMT is maximum at linear region and start to decrease when it reaches saturation. As known, the drain current is inversely proportional to the channel length. When the pHEMT is biased in the saturation, the depletion region at the drain terminal extends laterally into the channel, reducing the effective channel length. Since the depletion region width is bias dependent, the effective channel length is also bias dependent and is modulated by the drain-to-source voltage. The change in the effective channel length and the corresponding change in drain current [3]. The purpose of the study of the drain current and gate current against drain voltage is to observe any artificial behaviour, kink effect and buffer leakage in the output characteristics of the device.

![Figure 4.3 (a): Measured output characteristics of the 2x100x0.5 μm² GaAs pHEMT](image-url)
In the figure 4.3 (b) gate current against drain voltage of 2x100x0.5 μm² GaAs pHEMT shows some discontinuity of the data which should be an artificial behaviour or kink effect, will be discuss later on temperature dependent DC characteristics analysis. On the other hand the 4x50x0.15 μm² GaN DC behaviour is not as similar trend of 2x100x0.5 μm² GaAs pHEMT. Three typical phenomenons can be seen in the DC characteristic of the 4x50x0.15 μm² GaN pHEMT such as artificial behaviour, kink effect and buffer leakage as depicted in figure 4.4(a) and the drain current and gate current against drain voltage is depicted in figure 4.4 (b). Artificial behaviour of the data can be seen for certain $V_{ds}$ trace of 0 V to 1.5 V, which shows some discontinuity of the data being represented more clearly in figure 4.4(c). Among this effect of artificial behaviour of the data it needs further study in future. Meanwhile kink effect and leakage is seen in the DC characteristics where it starts from 4V and diminishes at 8V of the $V_{ds}$ trace as clearly depicted in figure 4.4 (d) with $V_{ds}$ step 0.5V.
Figure 4.4(a): Measured output characteristics of the 4x50x0.15 $\mu$m$^2$ GaN pHEMT

Figure 4.4 (b): Measured drain current and gate current against drain voltage of the 4x50x0.15 $\mu$m$^2$ GaN pHEMT
The Kink effect in the DC characteristic of the 4x50x0.15 μm² GaN pHEMT is considered a typical signature of the effects of buffer traps. Such effects are caused by the injection of hot electrons into buffer traps under the influence of high drain voltage [38-39] as shown in figure 4.4(e). These trapped electrons deplete the 2DEG and result in a reduction of the drain current for subsequent V_{ds} traces, since their release time may be of the order of seconds [40-41]. Buffer traps refer to the deep levels located in the buffer layer or in the interface between the buffer layer and the substrate. Under high electric field condition, due to high drain-source voltage, electrons moving in the 2DEG channel may get injected into the buffer traps. Due to the long trapping time constant (of the order of milliseconds [42] and even seconds [38], the trapped electrons cannot follow the high frequency signal and hence, they are not available for conduction. The trapped electrons produce a negative charge, which deplete the 2DEG, and therefore reduce the channel current.
These traps are primarily related to threading dislocations in the GaN layer due to the large lattice mismatch between the GaN and the substrate. These threading dislocations manifest themselves as electrons traps. In order to reduce the incidence of this type of traps, a relaxation layer is often added between the GaN buffer and the substrate [55]. The buffer leakage shown in figure 4.4(a) known as GaN pHEMTs are made on semi-insulating GaN buffers grown on substrates like sapphire, SiC, bulk grown GaN, Si, etc. Thicker GaN buffers are grown on these substrates to reduce the threading dislocation (TD) density to yield channels with a high mobility. To achieve a high-breakdown voltage and a high-power efficiency, it is necessary to have a low leakage through the underlying GaN buffer. Residual donors, presumably oxygen, in the unintentionally doped (UID) GaN, have been identified as a source of buffer leakage [55-56]. Further study about the kink effect in DC characteristics of GaN pHEMT device will be presented in the temperature dependent characterisation.

![Graph showing kink effect and buffer leakage in DC characteristics of the 4x50x0.15 μm² GaN pHEMT](image)

Figure 4.4(d): Kink effect and buffer leakage in DC characteristics of the 4x50x0.15 μm² GaN pHEMT
4.2.2 Transfer and Transconductance Characteristics

Figure 4.5 and 4.6 illustrates the transfer and transconductance properties of 2x100x0.50 μm² AlGaAs/InGaAs and 4x50x0.15 μm² AlGaN/InGaN pHEMTs. From the measured results the transconductance properties which showed that the maximum $g_m$ is 58.5 mS at $V_{gs} = -0.2$ V and $V_{ds} = 3$ V and the pinch-off voltage is less than -0.8V for 2x100x0.50 μm² GaAs pHEMT. In order to check the maximum $g_m$ of the 4x50x0.15 μm² GaN pHEMT, three plots are taken at same $V_{gs}$ with different $V_{ds}$ values such as 4 V, 10 V, 15 V respectively as depicted in figure 4.6. It can be seen that, the value for $g_m$ is 47, 55.4 and 55.83 mS at $V_{gs} = -4.8$ V and $V_{ds} = 4, 10, 15$ V and corresponding drain source current is 29.8, 42.6, 52.8 mA respectively. For the 4x50x0.15 μm² GaN pHEMT maximum $g_m$ can be seen at $V_{gs} = -4.8$ V and $V_{ds} = 15$V and corresponding pinch-off voltage ($V_P$) is less than -6V. This is because of AlGaN/InGaN heterojunction structures with high breakdown voltage due to the increased band gap of Nitride III-V compounds. Table 4.1 shows comparison of the measured DC values with some previously published work for the both pHEMTs. This comparison based on different biasing condition of both the device investigated in this work with the references. Both of GaAs and GaN pHEMTs in this work shows better agreement with the references.
Figure 4.5: Measured transfer and transconductance characteristics of the GaAs pHEMT

![Graph showing GaAs pHEMT characteristics](image)

Figure 4.6: Measured transfer and transconductance characteristics of the GaN pHEMT

![Graph showing GaN pHEMT characteristics](image)
Table 4.1: Comparison of the measured DC-Parameters of the 2x100x0.50 μm² GaAs pHEMT with reference [61] and 4x50x0.15 μm² GaN pHEMT with reference [63]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>This work</th>
<th>Ref [61]</th>
<th>Ref [63]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device</td>
<td>pHEMTs</td>
<td>GaAs</td>
<td>GaN</td>
<td>GaAs</td>
</tr>
<tr>
<td>L₉( μm)</td>
<td>Gate Length</td>
<td>0.5</td>
<td>0.15</td>
<td>1</td>
</tr>
<tr>
<td>Wₛ( μm)</td>
<td>Gate width</td>
<td>200</td>
<td>200</td>
<td>100</td>
</tr>
<tr>
<td>A ( μm²)</td>
<td>Area</td>
<td>100</td>
<td>30</td>
<td>100</td>
</tr>
<tr>
<td>Vₛₛ(V)</td>
<td>Gate – source voltage</td>
<td>-0.2</td>
<td>-4.8</td>
<td>-0.3</td>
</tr>
<tr>
<td>Vₛₛ(V)</td>
<td>Drain – source voltage</td>
<td>3</td>
<td>15</td>
<td>3</td>
</tr>
<tr>
<td>Iₛₛo</td>
<td>Drain saturation current</td>
<td>0.2 pA</td>
<td>0.2 μA</td>
<td>3.9 μA</td>
</tr>
<tr>
<td>Ψₒ(V)</td>
<td>Barrier height</td>
<td>0.69</td>
<td>0.72</td>
<td>0.76</td>
</tr>
<tr>
<td>n</td>
<td>Ideality factor</td>
<td>1.23</td>
<td>1.49</td>
<td>1.32</td>
</tr>
<tr>
<td>Vₛₚ(V)</td>
<td>Pinch off voltage</td>
<td>&lt; -0.8</td>
<td>&lt; -6.0</td>
<td>&lt; -0.6</td>
</tr>
<tr>
<td>gₛₘ(mS)</td>
<td>Transconductance</td>
<td>58.5</td>
<td>55.8</td>
<td>22.6</td>
</tr>
<tr>
<td>Iₛₐ(mA)</td>
<td>Drain currents</td>
<td>32.5</td>
<td>52.8</td>
<td>22.5</td>
</tr>
<tr>
<td>gₛₙ(mS/mm)</td>
<td>Transconductance width</td>
<td>292.5</td>
<td>279</td>
<td>226.2</td>
</tr>
<tr>
<td>Iₛₙ(mA/mm)</td>
<td>Drain current density</td>
<td>162.5</td>
<td>264</td>
<td>225.8</td>
</tr>
</tbody>
</table>

4.3 RF Parameter Extractions Procedure

On-wafer S-parameter measurements were carried out on 2x100x0.50 μm² GaAs pHEMT and 4x50x0.15μm² GaN pHEMT for small-signal characterising and analyzing of device performance. The measurements data will then be used in a procedure called parameter extraction. In this project, direct parameter extraction has been used [22]. Agilent’s Integrated Circuit Characterization and Analysis Program (IC-CAP) is used to perform the extraction in which enable the analysis to be done on a single platform. An equivalent circuit pi-model presented in figure 4.7, where it can be seen in two different parts, one is the intrinsic and the other is the extrinsic parts.
The **intrinsic** elements $g_m$, $g_d (R_{ds})$, $C_{gs}$, $C_{gd}$, $C_{ds}$, $R_i$ and $\tau$ are bias dependent elements and hence are required to be extracted at **hot** bias condition.

The **extrinsic** elements $L_g$, $R_g$, $C_{pg}$, $L_s$, $R_s$, $R_d$, $C_{pd}$ and $L_d$ are independent of the biasing condition. These are extracted using **off** and **cold** bias conditions.

![Equivalent Circuit Model](image)

**Figure 4.7: π small-signal equivalent circuit model for pHEMT in common source configuration [22]**

### 4.3.1 Cold Bias Extraction

The extraction process can thus be divided into two parts. Extrinsic parameters are determined first. Later, these extrinsic parameters will then be subtracted from the whole device model and, as a result, intrinsic parameters can be determined.

Two different operating conditions are needed to extract the extrinsic parameters:

- OFF (where, $V_{DS} = 0$ and $V_{GS} = 0$)
- STRONG PINCH-OFF (where, $V_{DS} = 0$ and $V_{GS}$ much lower than pinch off voltage $V_{PO}$).

At both bias points $V_{DS}$ is zero in order to achieve a symmetric and a simplified equivalent circuit model. The following flow chart in figure 4.8 shows the steps to be followed to extract the corresponding extrinsic values.
Figure 4.8: Flow chart for determining the extrinsic parameters of FETs [22]

All the steps illustrated in the flowchart are performed and the corresponding results obtained are detailed below:
Step1: Extracting the Parasitic Inductances and Resistances

The OFF state $S$ parameters ($V_{DS} = 0$ and $V_{GS} = 0$) of the device are measured via IC-CAP. These $S$-parameters are then converted to $Z$ parameters for the computation of inductances and resistances. The $Z$ parameters at OFF state hence derived are given by the following equations [22]:

\begin{align}
Z_{11} &= R_S + R_g + 0.5R_{ch} + \left[ \omega \left( L_s + L_g \right) - \frac{1}{\omega C_g} \right] \\
Z_{12} &= Z_{21} = R_S + 0.5R_{ch} + j\omega L_s \\
Z_{22} &= R_d + R_S + R_{ch} + j\omega (L_s + L_d)
\end{align}

The parasitic inductances $L_s$, $L_d$ and $L_g$ can be computed by using the imaginary parts of the above equations, it has been illustrated with the extracted values from the equations, (4.1)-(4.3),

- To extract $L_s$ \[ \text{Im} \left( Z_{12} \right) = j\omega L_s \] \hspace{1cm} (4.4)
  \[ L_s = \frac{\text{Im}(Z_{12})}{\omega} \] \hspace{1cm} (4.5)

- To extract $L_d$ \[ \text{Im}(Z_{22}) = j\omega(L_s + L_d) \] \hspace{1cm} (4.6)
  \[ L_d = \frac{\text{Im}(Z_{22})}{\omega} \] \hspace{1cm} (4.7)

- To extract $L_g$ \[ \text{Im} \left( Z_{11} \right) = j\omega(L_s + L_g) \] \hspace{1cm} (4.8)
  \[ L_g = \frac{\text{Im}(Z_{11})}{\omega} - L_s \] \hspace{1cm} (4.9)

Similarly, the resistances can be extracted from the real parts of equations (4.1)-(4.3). However, an additional expression is needed as there are four unknowns needing four equations. As a solution, under the heavy pinch-off condition where ($V_{DS} = 0$ and $V_{GS}$ much lower than pinch off voltage $V_{PO}$), the channel is completely off and the real part of $Z_{11}$ is given as [22]:

\[ Z_{11} = R_S + R_g + 0.5R_{ch} - \frac{1}{\omega C_g} \]
As a result, by looking at equations (4.1)-(4.3) and (4.10), the resistances can be extracted as follows:

- To extract $R_{ch}$ (only $R_{ch}$ is extracted using both Pinch off and OFF state)
  - Pinch off state: $\text{Re} \left[ Z_{11} (\nu_{po}) \right] = R_s + R_g$ (4.11)
  - OFF state: $\text{Re} \left[ Z_{11} \right] = R_s + R_g + 0.5R_{ch}$ (4.12)
  - $R_{ch} = 3xR_e Z_{11} - R_e [Z_{11\text{PO}}]$ (4.13)

- To extract $R_s$
  - $\text{Re} \left[ Z_{12} \right] = 0.5 \, R_{ch} + R_s$ (4.14)
  - $R_s = \text{Re} \left[ Z_{12} \right] - 0.5R_{ch}$ (4.15)

- To extract $R_g$
  - $R_g = \text{Re} \left[ Z_{11} \right] - R_s - 0.5R_{ch}$ (4.16)

- To extract $R_d$
  - $R_d = \text{Re} \left[ Z_{22} \right] - R_s - R_{ch}$ (4.17)

**Step 2: Extracting the Parasitic Capacitances**

From the equivalent circuit model in figure 4.7, there are two parasitic capacitances that are required to be extracted, $C_{pg}$ and $C_{pd}$, which are the pad capacitances formed on the gate and drain side respectively. For this extraction again the cold or pinch-off bias condition (should be disimilar for GaAs and GaN pHEMTs) is used. The $S$-parameters measured at this condition are converted to the respective $Z$-parameters and then, according to the topology of the equivalent circuit model, the inductances and the resistances computed in the previous section are subtracted to eliminate their effect.

\[
Z_{11} - R_s - R_g - j\omega (L_s + L_g) \quad (4.18)
\]
\[
Z_{12} - R_g - j\omega L_s = Z_{21} - R_s - j\omega L_s \quad (4.19)
\]
\[
Z_{22} - R_d - R_s - j\omega (L_s + L_d) \quad (4.20)
\]
After that, the resultant $Z$ parameters are transformed to the respective $Y$-parameters. The capacitances can then be extracted and are given as:

$$Y_{11} = j\omega(2C_b + C_{pg})$$  \hspace{1cm} (4.21)

$$Y_{12} = Y_{21} = j\omega C_b$$  \hspace{1cm} (4.22)

$$Y_{22} = j\omega(C_b + C_{pd} + C_{ds})$$  \hspace{1cm} (4.23)

Where, $C_b$ is the fringing capacitance due to depleted layer extension at each side of the gate/residual capacitance [22]. Using equations (4.21)-(4.23) the pad parasitic capacitances can be extracted as follows:

- To extract $C_b$: $C_b = \text{Im}(Y_{12})$  \hspace{1cm} (4.24)
- To extract $C_{pg}$: $\text{Im}(Y_{11}) = j\omega(2C_b + C_{pg})$  \hspace{1cm} (4.25)
  $$C_{pg} = \frac{\text{Im}(Y_{11})}{\omega} - 2C_b$$  \hspace{1cm} (4.26)
- To extract $C_{pg}$: $\text{Im}(Y_{22}) = j\omega(C_b + C_{pd} + C_{ds})$  \hspace{1cm} (4.27)
  $$C_{pd} = \frac{\text{Im}(Y_{22})}{5\omega} - C_b$$  \hspace{1cm} (4.28)

With all the extrinsic parameters extracted, the intrinsic bias dependent parameters can now be extracted and determined.

### 4.3.2 Hot Bias Extraction

**Step3: (Extracting Intrinsic Parameters)**

The intrinsic elements $g_m$, $g_d$, $C_{gs}$, $C_{gd}$, $C_{ds}$, $R_i$ and $\tau$ are bias dependent elements and hence are required to be extracted at hot biasing conditions. The flowchart of the extraction of the intrinsic parameters is presented in figure 4.9. In this experiment the biasing condition was chosen so that the maximum transconductance value could be determined.
Consider the hot bias condition, $V_{gs} = -0.05V$, $V_{ds} = 3V$ @ max $g_m = 37.6ms$.

Subtract series inductances computed:
- $Z_{11} = j\omega L_{s1}$
- $Z_{22} = j\omega L_{d1}$

Subtract parallel capacitances computed:
- $Y_{11} = j\omega C_{ps}$
- $Y_{22} = j\omega C_{pd}$

Subtract resistances and source inductances computed:
- $Z_{11} = R_s - j\omega L_s$
- $Z_{12} = R_s - j\omega L_s = Z_{21} - R_s - j\omega L_s$
- $Z_{22} = R_s - j\omega L_s$

Use these $Y$-parameters to compute the 7 intrinsic parameters:
- $Y_{11} = \frac{R_{c2} \omega^2}{D} + j\omega \left( \frac{C_{ei}}{D} + C_{pd} \right)$
- $Y_{12} = -j\omega C_{ps}$
- $Y_{21} = g_{ds} \exp(-j\omega \tau) - j\omega C_{ps}$
- $Y_{22} = g_{ds} + j\omega (C_{ds} + C_{pd})$

Figure 4.9: Flow chart for determining the intrinsic parameters of FETs [22]

As shown in figure 4.9, to determine the intrinsic parameters, firstly the computed extrinsic parameters are to be deembedded. The procedure is as follows:
Transform the S-parameters of the chosen bias point into Z-parameters. From the obtained Z-parameters subtract the gate and the drain parasitic series inductances computed from extrinsic extractions.

\[
Z_{11} - j\omega L_g \quad (4.29)
\]

\[
Z_{22} - j\omega L_d \quad (4.30)
\]

The resulting Z-parameters are then converted to Y parameters and then the effects of the two parasitic capacitances are eliminated:

\[
Y_{11} - j\omega C_{pg} \quad (4.31)
\]

\[
Y_{22} - j\omega C_{pd} \quad (4.32)
\]

Finally the Y-parameters are converted back to Z-parameters and the series resistances and source inductances are subtracted, completing the process of deembedding.

\[
Z_{11} - R_s - j\omega L_s \quad (4.33)
\]

\[
Z_{12} - j\omega L_s = Z_{21} - R_s - j\omega L_s \quad (4.34)
\]

\[
Z_{22} - R_d - j\omega L_s \quad (4.35)
\]

The Z-parameters obtained are then converted back into Y-parameters which are now ideal for the intrinsic parameter extraction. The following equations are then used to determine the intrinsic parameters:

\[
C_{gd} = \frac{\text{Im}(Y_{22})}{\omega} \quad (4.36)
\]

\[
C_{gs} = \frac{\left[\text{Im}(Y_{11}) - \omega C_{gd} \right]}{\omega} \left[1 + \frac{\text{Re}^2(Y_{11})}{\left[\text{Im}(Y_{11}) - \omega C_{gd} \right]^2}\right] \quad (4.37)
\]

\[
g_{ds} = \text{Re}(Y_{22}) \quad (4.38)
\]

\[
C_{ds} = \frac{\text{Im}(Y_{22}) - \omega C_{gd}}{\omega} \quad (4.39)
\]

\[
R_i = \frac{\text{Re}(Y_{11})}{\text{Re}^2(Y_{11}) + \left[\text{Im}(Y_{11}) - \omega C_{gd}\right]^2} \quad (4.40)
\]
\( \tau = \frac{1}{\omega} \arcsin \left[ \frac{-\text{Im}(Y_{21}) - \omega C_{gs} R_1 \text{Re}(Y_{21})}{g_m} \right] \) (4.41)

\( g_m = \left[ \left( \text{Im}(Y_{21}) + \omega C_{gs} \right)^2 + \text{Re}^2(Y_{21}) \right]^{\frac{1}{2}} \left( 1 + \omega^2 R_1^2 C_{gs}^2 \right)^{\frac{1}{2}} \) (4.42)

### 4.3.3 Small Signal Parameter Extraction Results

Small signal parameter extraction is carried out under the biasing values of \( V_{gs} = -0.2 \) V and \( V_{ds} = 3 \) V for 2x100x0.50 μm^2 AlGaAs/InGaAs pHEMT and \( V_{gs} = -4.8 \) V and \( V_{ds} = 15 \) V for 4x50x0.15 μm^2 AlGaN/InGaN pHEMT to achieve the maximum transconductance, \( g_m \). Figure 4.10 and 4.11 represents the small signal equivalent circuit developed by Agilent ADS from the extracted small signal data of GaAs and GaN pHEMTs respectively. The figures are grounded to source to avoid the oscillation when signal travel from output port to the input port. Table 4.2 shows the comparison of the extracted small signal parameter from the measured S-parameter of 2x100x0.5 μm^2 GaAs and 4x50x0.15 μm^2 GaN pHEMTs with probe of 150 μm pitch size.

![Small Signal Parameter Extraction Diagram](image1)

**Figure 4.10**: Extracted small signal circuit parameters of the 2x100x0.5 μm^2 GaAs pHEMT at \( V_{gs} = -0.2 \) V and \( V_{ds} = 3 \) V
Figure 4.11: Extracted small signal circuit parameters of the 4x50x0.15 μm² GaN pHEMT at $V_{gs} = -4.8$ V and $V_{ds} = 15$ V

Table 4.2: The extracted small signal parameter from the measured S-parameter

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>GaAs pHEMT</th>
<th>GaN pHEMT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{pg}$ (fF)</td>
<td>Parasitic gate capacitance</td>
<td>36.48</td>
<td>50.2</td>
</tr>
<tr>
<td>$C_{pd}$ (fF)</td>
<td>Parasitic drain capacitance</td>
<td>61.30</td>
<td>85.78</td>
</tr>
<tr>
<td>$L_s$ (pH)</td>
<td>Source inductance</td>
<td>2.91</td>
<td>0.75</td>
</tr>
<tr>
<td>$L_d$ (pH)</td>
<td>Drain inductance</td>
<td>65.25</td>
<td>69</td>
</tr>
<tr>
<td>$L_g$ (pH)</td>
<td>Gate inductance</td>
<td>133.6</td>
<td>150</td>
</tr>
<tr>
<td>$R_s$ (Ω)</td>
<td>Source resistance</td>
<td>2.50</td>
<td>2.97</td>
</tr>
<tr>
<td>$R_d$ (Ω)</td>
<td>Drain resistance</td>
<td>4.96</td>
<td>5.71</td>
</tr>
<tr>
<td>$R_g$ (Ω)</td>
<td>Gate resistance</td>
<td>1.92</td>
<td>2.71</td>
</tr>
<tr>
<td>$C_{gd}$ (fF)</td>
<td>Gate-drain capacitance</td>
<td>17.08</td>
<td>34.2</td>
</tr>
<tr>
<td>$C_{ds}$ (fF)</td>
<td>Drain-source capacitance</td>
<td>81.88</td>
<td>126.3</td>
</tr>
<tr>
<td>$C_{gs}$ (fF)</td>
<td>Gate-source capacitance</td>
<td>428.5</td>
<td>152</td>
</tr>
<tr>
<td>$R_{ds}$ (Ω)</td>
<td>Output resistance</td>
<td>540</td>
<td>187</td>
</tr>
<tr>
<td>$R_i$ (Ω)</td>
<td>Input resistance</td>
<td>1.47</td>
<td>1.6</td>
</tr>
<tr>
<td>$g_{m}$ (mS)</td>
<td>Intrinsic transconductance</td>
<td>69</td>
<td>66.3</td>
</tr>
</tbody>
</table>
### 4.3.4 Measured and Modelled S-parameters Comparison

In order to investigate the validity of the developed small-signal model for the both 2x100x0.50 μm² AlGaAs/InGaAs and 4x50x0.15 μm² AlGaN/InGaN pHEMTs, comparisons between the simulated and measured S-parameters is necessary. With these parameters extracted in table 4.2, by putting them in the small-signal circuit model as shown in figures 4.10 and 4.11 in Agilent’s Advanced Design System (ADS), simulation is made and then compared to the measured ones. A comparison of the simulated and measured S-parameters are made for the 2x100x0.50 μm² AlGaAs/InGaAs pHEMT and 4x50x0.15 μm² AlGaN/InGaN pHEMT as shown in figures 4.12 and 4.13 to validate the small signal model.

<table>
<thead>
<tr>
<th>g&lt;sub&gt;ms&lt;/sub&gt; (mS/mm)</th>
<th>Transconductance width</th>
<th>345</th>
<th>331.5</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \tau ) (pS)</td>
<td>Signal delay</td>
<td>0.21</td>
<td>0.58</td>
</tr>
</tbody>
</table>

![Graph](image-url)  

**Figure 4.12(a):** Comparison of measured and modelled S<sub>11</sub> of the GaAs pHEMT
Figure 4.12(b): Comparison of measured and modelled $S_{12}$ of the GaAs pHEMT

Figure 4.12(c): Comparison of measured and modelled $S_{21}$ of the GaAs pHEMT
Figure 4.12(d): Comparison of measured and modelled $S_{22}$ of the GaAs pHEMT

Figure 4.13(a): Comparison of measured and modelled $S_{11}$ of the GaN pHEMT
Figure 4.13(b): Comparison of measured and modelled $S_{12}$ of the GaN pHEMT

Figure 4.13(c): Comparison of measured and modelled $S_{21}$ of the GaN pHEMT
The results (figure 4.12 and 4.13) show good agreement between the measured and simulated parameters up to 20 GHz. The hot and cold biasing method has limitation above 20-30 GHz. Therefore, the used methodology of finding a small-signal model including the direct parameters extraction technique is well validated [22].

4.3.5 Comparison of Current Gain and Maximum Available Gain

The cut-off frequency, $f_t$, and the maximum oscillation frequency, $f_{\text{max}}$, can be found by locating the points at which the 20 dB/decade slope of lines intersects the 0 dB. The measured values for $2\times100\times0.5 \, \mu m^2$ AlGaAs/InGaAs pHEMT, $f_t$ is found to be about 27.4 GHz and $f_{\text{max}}$ is found to be 122 GHz as shown in figure 4.14 and 4.15. While for the $4\times50\times0.15 \, \mu m^2$ AlGaN/InGaN pHEMT, the cut-off frequency $f_t$ is found to be about 63 GHz and the maximum frequency of oscillation ($f_{\text{max}}$) is found to be about 127 GHz for as shown in figure 4.16 and 4.17 respectively.
Figure 4.14: Current gain $h_{21}$ as a function of frequency of the GaAs pHEMT.

Figure 4.15: Maximum Available Gain (MAG) as a function of frequency of the GaAs pHEMT.
Figure 4.16: Current gain $h_{21}$ as a function of frequency of the GaN pHEMT

Figure 4.17: Maximum Available Gain (MAG) as a function of frequency of the GaN pHEMT
In figure 4.14 and 4.16, the cut-off frequency, \( f_t \) can be found at the point when the current gain, \( h_{21} \), equals to zero. The measured \( f_t \) can be verified by using the given analytical formula in equation (2.26) given as,

\[
f_t = \frac{g_m}{2\pi(C_{gs} + C_{gd})}
\]  

(4.43)

From the extracted parameters of the table 4.2, for 2x100x0.5 \( \mu m^2 \) AlGaAs/InGaAs pHEMT, \( g_m = 69 \) mS, \( C_{gs} = 428.5 \) fF, \( C_{gd} = 17.08 \) fF. Substituting this value in equation (4.43), \( f_t = 24.6 \) GHz. For 4x50x0.15 \( \mu m^2 \) AlGaN/InGaN pHEMT \( g_m = 66.3 \) mS, \( C_{gs} = 152 \) fF, \( C_{gd} = 34.2 \) fF. Substituting this value in equation (4.43), \( f_t = 56.6 \) GHz.

Similarly, in figure 4.15 and 4.17, the maximum oscillation frequency, \( f_{max} \), can be found by plotting the maximum available gain (MAG). Again, analytical formula can also be used to determine the \( f_{max} \) using the extracted parameter values by the equations (2.27) given as,

\[
f_{max} = \frac{f_t}{2\sqrt{f_t + f_r\tau}}
\]  

where \( r_t = \frac{R_g + R_i + R_s}{R_{ds}} \) and \( \tau = 2\pi R_g C_{gd} \)  

(4.44)

(4.45)

From the extracted parameters in table 4.2, for the 2x100x0.5 \( \mu m^2 \) AlGaAs/InGaAs pHEMT, \( R_g = 1.92 \) k\( \Omega \), \( R_i = 1.47 \) k\( \Omega \), \( R_s = 2.5 \) k\( \Omega \), \( R_{ds} = 540 \) k\( \Omega \), \( C_{gd} = 17.08 \) fF, \( f_t = 24.6 \) GHz and therefore, \( f_{max} = 97 \) GHz. For the 4x50x0.15 \( \mu m^2 \) AlGaN/InGaN pHEMT, \( R_g = 2.71 \) k\( \Omega \), \( R_i = 1.6 \) k\( \Omega \), \( R_s = 2.97 \) k\( \Omega \), \( R_{ds} = 187 \) k\( \Omega \), \( C_{gd} = 34.2 \) fF, \( f_t = 56.6 \) GHz and therefore, \( f_{max} = 105.6 \) GHz.

Comparing the modelled \( f_t \) and \( f_{max} \) from extracted small signal parameters to the measured ones shown in figure 4.14-4.17 respectively for the both pHEMTs with some reference would show the accuracy of the model. Table 4.3 represents a comparison of measured and modelled values of \( f_t \) and \( f_{max} \) of 2x100x0.5 \( \mu m^2 \) GaAs pHEMT with reference [11] and 4x50x0.15 \( \mu m^2 \) GaN pHEMT with reference [63].
Table 4.3: Comparison of measured and modelled values of $f_t$ and $f_{\text{max}}$ of 2x100x0.5 μm$^2$ GaAs with reference [11] and 4x50x0.15 μm$^2$ GaN pHEMTs with reference [63]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>This work</th>
<th>Ref.[11]</th>
<th>Ref.[63]</th>
</tr>
</thead>
<tbody>
<tr>
<td>pHEMTs</td>
<td>GaAs</td>
<td>GaN</td>
<td>GaAs</td>
</tr>
<tr>
<td>Gate length (μm)</td>
<td>0.5</td>
<td>0.15</td>
<td>0.5</td>
</tr>
<tr>
<td>Gate width (μm)</td>
<td>200</td>
<td>200</td>
<td>200</td>
</tr>
<tr>
<td>Biasing point (V)</td>
<td>$V_{gs} = -0.2, V_{ds} = 3$</td>
<td>$V_{gs} = -4.8, V_{ds} = 15$</td>
<td>$V_{gs} = -0.2, V_{ds} = 3$</td>
</tr>
<tr>
<td>Measured $f_t$</td>
<td>27.4</td>
<td>63</td>
<td>26.4</td>
</tr>
<tr>
<td>Modelled $f_t$</td>
<td>24.6</td>
<td>56.6</td>
<td>23</td>
</tr>
<tr>
<td>Measured $f_{\text{max}}$</td>
<td>122</td>
<td>127</td>
<td>112</td>
</tr>
<tr>
<td>Modelled $f_{\text{max}}$</td>
<td>97</td>
<td>105.6</td>
<td>80</td>
</tr>
</tbody>
</table>

From the above table the difference in $f_t$ and $f_{\text{max}}$ is found to be about 11.2% and 25.7% for the 2x100x0.5 μm$^2$ GaAs pHEMT and while $f_t$ and $f_{\text{max}}$ is found to be about 10.7% and 20.2% for the 4x50x0.15 μm$^2$ GaN pHEMT. About 10% tolerance could be accepted for $f_t$ for most of the applications. On the other hand there is a huge difference between the calculated and modelled $f_{\text{max}}$ in figure 4.15 and 4.17. All of these discrepancies could be attributed to the fact that the adopted model is a first order crude model which is not as effective as representing high frequency beyond 20 GHz behaviour of the transistor. In addition, the measurement equipment was only calibrated and capable of accurate measurements up to 40-50 GHz, effectiveness of capturing higher frequency behaviours degrade significantly beyond the 40 GHz upper limit. However, it should be noted that, the device would only be designed below the cut-off frequency. From the above observation, the presented small-signal model is still a very good and accurate representation of the actual device. As compared to the reference [11] with 2x100x0.5 μm$^2$ AlGaAs/InGaAs pHEMT and reference [63] with 4x50x0.15 μm$^2$ AlGaN/InGaN pHEMTs in this work presented in table 4.3 showing good agreements in all aspects which prove the accuracy of the model to represent the actual device.
4.3 The Noise Figure Analysis and Results

Noise in microwave FETs is produced by both ‘intrinsic sources’ to the device and by ‘thermal sources’ associated with the parasitic resistances. The intrinsic noise source arises from two mechanisms:

- One is thermal (Johnson) noise, which is produced in the ohmic section of the device channel and

- Another is diffusion noise, which is produced in the velocity-saturated section of the channel and can be the dominant one for short-gate devices.

The minimum noise figure, $NF_{\text{min}}$ in FETs is related to the transistor small signal equivalent circuit parameters and this can be approximated by the equation given below [43].

$$NF_{\text{min}} = 1 + K_f \left( \frac{C_{gs}}{g_m} \right) \sqrt{\frac{g_m (R_s + R_n)}{2\pi f}}$$  \hspace{1cm} (4.46)

where $K_f$ is a fitting factor representing the quality of the channel and is called Fukui’s constant. The magnitude of $K_f$ can be evaluated approximately using a theoretical analysis of the noise theory:

$$K_f \approx 2 \frac{I_{\text{opt}}}{E_c L g m}$$ \hspace{1cm} (4.47)

Where,

- $I_{\text{opt}}$ is the optimum drain-to-source current at minimum noise figure,

- $E_c$ is the critical electric field in the channel and

- $L g$ is the gate length of the device.

A typical value for $K_f$ is 4-6 for GaAs MESFETs while this is much smaller for HEMT devices due to better quality of the electron channel. The value of $F_{\text{min}}$ is usually quoted in decibel and this is given by:
As $NF_{\text{min}}$ with good RF performance of low noise HEMTs is required, it can be expected that devices with a high maximum $f_t$ will also exhibit low $NF_{\text{min}}$. From the equation (4.48) it can be seen that minimum noise figure of pHEMTs depends strongly on the frequency and the important parasitic parameters: gate and source resistances, and gate-source capacitance.

### 4.4.1 Noise Figure Analysis of 2x100x0.5 μm² GaAs pHEMT

Figure 4.18 and 4.19 represents the modelled noise figure and $NF_{\text{min}}$ as a function of frequency of the for 2x100x0.5 μm² AlGaAs/InGaAs pHEMT. Table 4.4 demonstrates some comparison of $NF_{\text{min}}$ at different frequency and gate lengths at room temperature.

$$NF_{\text{min}} (dB) = 10 \log NF_{\text{min}}$$

$$NF_{\text{min}} (dB) = 10 \log \left[ 1 + K_f \left( \frac{C_{gs}}{g_m} 2\pi f \right) \sqrt{g_m (R_g + R_s)} \right]$$

(4.48)

$$NF_{\text{min}} (dB) = 10 \log \left[ 1 + K_f \left( \frac{C_{gs}}{g_m} 2\pi f \right) \sqrt{g_m (R_g + R_s)} \right]$$

Figure 4.18: Modelled noise figure as a function of frequency of the GaAs pHEMT
Figure 4.19: Modelled $NF_{\text{min}}$ as a function of frequency of the GaAs pHEMT

Table 4.4: Reference summary of noise figure of some GaAs pHEMTs

<table>
<thead>
<tr>
<th>Gate lengths(μm)</th>
<th>Frequency (GHz)</th>
<th>$NF_{\text{min}}$ (dB)</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.15</td>
<td>12</td>
<td>0.42</td>
<td>[44]</td>
</tr>
<tr>
<td>0.5</td>
<td>12</td>
<td>1.3</td>
<td>[45]</td>
</tr>
<tr>
<td>0.5</td>
<td>18</td>
<td>2.2</td>
<td>[45]</td>
</tr>
<tr>
<td>0.35</td>
<td>18</td>
<td>1.2</td>
<td>[46]</td>
</tr>
<tr>
<td>0.5</td>
<td>10</td>
<td>0.72</td>
<td>This work</td>
</tr>
<tr>
<td>0.5</td>
<td>12</td>
<td>0.90</td>
<td>This work</td>
</tr>
<tr>
<td>0.5</td>
<td>18</td>
<td>1.3</td>
<td>This work</td>
</tr>
</tbody>
</table>

### 4.4.2 Noise Figure Analysis of 4x50x0.15 μm² GaN pHEMT

Figure 4.20 and 4.21 represents the modelled noise figure and $NF_{\text{min}}$ as a function of frequency of the 4x50x0.15 μm² AlGaN/InGaN pHEMT. Table 4.5 demonstrates some comparison of $NF_{\text{min}}$ at different frequency and gate lengths.
Figure 4.20: Modelled noise figure as a function of frequency of the GaN pHEMT

Figure 4.21: Modelled $\text{NF}_{\min}$ as a function of frequency of the GaN pHEMT
### Table 4.5: Reference summary of noise figure of some GaN pHEMTs

<table>
<thead>
<tr>
<th>Gate lengths (µm)</th>
<th>Frequency (GHz)</th>
<th>$\text{NF}_{\text{min}}$(dB)</th>
<th>References</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.12</td>
<td>8</td>
<td>0.53</td>
<td>[47]</td>
</tr>
<tr>
<td>0.15</td>
<td>10</td>
<td>0.89</td>
<td>[48]</td>
</tr>
<tr>
<td>0.15</td>
<td>12</td>
<td>0.72</td>
<td>[49]</td>
</tr>
<tr>
<td>0.15</td>
<td>10</td>
<td>0.97</td>
<td>[50]</td>
</tr>
<tr>
<td>0.15</td>
<td>8</td>
<td>0.34</td>
<td>This work</td>
</tr>
<tr>
<td>0.15</td>
<td>10</td>
<td>0.43</td>
<td>This work</td>
</tr>
<tr>
<td>0.15</td>
<td>12</td>
<td>0.51</td>
<td>This work</td>
</tr>
</tbody>
</table>

#### 4.4.3 Noise Figure Comparison

The minimum noise figures of the 2x100x0.5 µm² AlGaAs/InGaAs and the 4x50x0.15 µm² AlGaN/InGaN pHEMTs are compared in figure 4.22. The GaN pHEMT shows much better noise figure than the GaAs ones.

![Figure 4.22: Modelled $\text{NF}_{\text{min}}$ as a function of frequency for both GaAs and GaN pHEMTs](image)
As known, $\text{NF}_{\text{min}}$ is a function of the biases (operating current) and frequency; the noise parameters modelled of this work over a frequency range of 0.45 to 50 GHz for a fixed bias point of $V_{ds} = 3\, \text{V}$, $V_{gs} = -0.2\, \text{V}$ of the $2\times100\times0.5\, \mu\text{m}^2$ AlGaAs/InGaAs and a fixed bias point of $V_{ds} = 15\, \text{V}$, $V_{gs} = -4.8\, \text{V}$ of the $4\times50\times0.15\, \mu\text{m}^2$ AlGaN/InGaN pHEMTs. Table 4.4 and 4.5 shows the comparison of modelled noise parameters of this work at different frequency of some previously published references. The comparisons represent the better noise figure of this work with respect to the references. Observation of the previous data (in table 4.4-4.5) and the comparisons (figure 4.22) suggest that the developed small-signal model of the both pHEMTs is accurate enough to represent the actual device.

4.5 Temperature Dependent pHEMTs Modelling

Temperature dependence study is a vital part of the complete characterisation on active devices. It is especially important if the active devices are to be designed for high power applications where enormous heat could be generated during the operation of the chip. The work here involves studying the temperature dependence of $2\times100\times0.5\, \mu\text{m}^2$ AlGaAs/InGaAs and $4\times50\times0.15\, \mu\text{m}^2$ AlGaN/InGaN pHEMTs. Although some previous studies on temperature dependence of GaAs pHEMTs have been reported [11], GaN pHEMT for the first time have been presented in this work.

4.5.1 Thermal Effects

It is a common practice to study thermal effects of active devices at high temperature involving complicated phenomenon in the intrinsic part of the device, especially under the gate and drain region. Hot-electrons and impact ionization are two of the most dominant effects which are reported [51-54]. Depending on the bias point and temperature, their effects can be extremely strong or moderate compared to other effects like scattering and mobility reduction. In order to achieve high-frequency applications, increasing short gate length has been designed and this results in electric field soaring to very high values for relatively low drain
bias. At the same time, in order to get high output power, the device must be biased at high field region. Therefore, it is very normal for this high field phenomenon affecting the performance of the device. On the other hand, pHEMTs which achieve better performance by having better confinement of carriers in the pseudomorphic channel favours the impact ionization due to the narrow band-gap material used for the channel [11, 71]. Figure 4.23 shows the high field phenomenon (hot electrons and impact ionisation effects) in an AlGaAs pHEMT [51].

When impact ionization happens in the channel layer, a lattice atom will give out a pair of electron and hole. The electron could achieve sufficient energy to become a carrier contributing to the overall current. Meanwhile, the hole could overcome the band discontinuity and go into the donor layer. It could be collected by the gate electrode and produce gate current or it could get trapped in one of the interface or surface states causing a degradation in transconductance ($g_m$), drain current ($I_d$), and pinch-off voltage ($V_p$) [54]. For this reason, temperature effects on the DC characteristics of pHEMTs are in need to study.
4.5.2 DC Temperature Dependent pHEMTs Modelling

In order to study the effects of temperature on the performance of the 2x100x0.5 µm² AlGaAs/InGaAs and 4x50x0.15 µm² AlGaN/InGaN pHEMTs characteristics were measured at the temperatures ranges from -40 to 150°C. The transfer characteristic of the 2x100x0.5 µm² AlGaAs/InGaAs and 4x50x0.15 µm² AlGaN/InGaN pHEMTs are presented in figure 4.24 and 4.25 at different temperature respectively. The degradation of the output current, $I_{ds}$, can be observed as the temperature increases. This is due to the fact that, at high temperature, carrier mobility is reduced due to increased scattering effect of the carriers. However, on the other hand, at lower $V_{gs}$, higher current can be seen at higher temperature, this is due to the fact that mobility reduction and scattering effect are high field phenomenon, whereas, at lower field, the pinch-off voltage shift/reduction is more prominent. The pinch-off voltage shift is due to the higher carrier concentration resulting earlier channel opening at high temperature [11].

![Figure 4.24: Measured temperature dependent of transfer characteristics of the GaAs pHEMT](image-url)
From the above figures, it is observed that the GaN pHEMT is more susceptible to the temperature effects than GaAs pHEMT devices. In order to investigate the differences in terms of degree of changes due to thermal effects, temperature dependent output characteristics of the both pHEMTs need to be studied.

From the temperature dependent output characteristics of the 2x100x0.5 µm² AlGaAs/InGaAs pHEMT depicted in figure 4.26 (a), degradation of output current can again be seen in this plot at high field, high V_{gs}, due to greater scattering and lower mobility, whereas, at low field, low V_{gs}, pinch-off voltage shift gives higher current at higher temperature. At V_{gs} = 0.2 V, a visible kink can be seen at lower temperatures, -25°C and 0°C. The DC characteristics, however, show a sudden rise in the drain current at fixed value of drain voltage, resulting in high drain conductance and reduced voltage gain. This undesirable phenomenon is called Kink Effect [37]. It is more clearly depicted in figure 4.26 (b).
Figure 4.26 (a): Temperature dependent of output characteristics of the GaAs pHEMT

Figure 4.26 (b): Output conductance against drain-source voltage of the GaAs pHEMT
The kink effect is more clearly indicated in figure 4.26 (b) by an abrupt increase in the output conductance $G_0$, where it is observed to take place at a constant gate-to-drain bias for a given temperature. This can be seen from figure 4.26 (b) where a decrease in $V_{gs}$ results in an equal decrease in $V_{ds}$, at the kink. The appearance and the mechanism of kink effect in the output I-V characteristics of pseudomorphic AlGaAs/GaInAs high-electron-mobility transistors is also reported in [67]. In this reference the kink is postulated to arise from impact ionisation in the 2-DEG. The generated electrons drift towards the drain, while generated holes are prevented from entering the AlGaAs layer by the heterojunction barrier, and are injected into the GaAs buffer layer. These holes subsequently combine with electrons on the source side of the channel and these results in additional channel width and hence the output current increases. These effects are significantly reduced with temperature getting higher introducing scattering and mobility reduction [57]. Temperature dependent output characteristic of the 4x50x0.15 μm$^2$ AlGaN/InGaN pHEMT is depicted in figure 4.27 (a).

![Figure 4.27 (a): Measured temperature dependent of output characteristics of the GaN pHEMTs](image)
**Figure 4.27 (b): Kink effect in the GaN pHEMT @ -25 and 0°C**

**Figure 4.27 (c): Output conductance against drain-source voltage of the GaN pHEMT @ -25°C**
From the figure 4.27 (a), it can be seen that, the output characteristic of the 4x50x0.15 μm² AlGaN/InGaN pHEMT suffers from kink effect at all temperature. The difference between the kink effect in 2x100x0.5 μm² AlGaAs/InGaAs and 4x50x0.15 μm² AlGaN/InGaN pHEMTs is that, the GaAs device shows kink only at -25 and 0°C while the GaN devices suffers from kink effect at all temperatures, which is considered to be a typical signature of the effects of buffer traps [38-41] as discussed before. Such effects are caused by the injection of hot electrons into buffer traps under the influence of high drain voltage. These trapped electrons deplete the 2DEG and result in a reduction of the drain current for subsequent $V_{ds}$ traces, since their release time may be of the order of seconds. It is more clearly depicted in figure 4.27 (b), 4.27 (c) and 4.27 (d). From figure 4.27 (b), the drain current shows kink in both temperature -25 and 0°C. In order to check this effect, from figure 4.27 (c) and 4.27 (d) an abrupt increase in the output conductance $G_0$, where a decrease in $V_{gs}$, results in an equal decrease in $V_{ds}$ at the kink can be seen. So, the temperature dependent kink effect modelling and analysis is an important
key for future high mobility electron transistor research. The traps effect such as kink effect and current collapse associated to epitaxial structure still need to be overcome for next-generation GaN device [70].

In order to study the effect of temperature on the pinch-off voltage shift, a comparison between the 2x100x0.5 μm² AlGaAs/InGaAs and 4x50x0.15 μm² AlGaN/InGaN pHEMTs are made in figure 4.28 and 4.29. The plots are both normalised to the data measured at 25°C to eliminate the difference seen in the output currents observed in figures 4.24-4.27. It can be seen that the change in pinch-off voltage is greater in GaN; which can indicate that the GaN pHEMTs experiences greater change in pinch-off voltage with the change of temperature compared to the GaAs ones. The effects of a lower pinch-off voltage (more negative) would mean an earlier opening of channel allowing electrons to flow through, hence, for the same applied $V_{gs}$, a lower pinch-off voltage (at high temperature) result in more output current $I_{ds}$ is observed.

![Graph showing pinch-off voltage shift with respect to temperature of the GaAs pHEMT](image)

**Figure 4.28: Pinch-off voltage shift with respect to temperature of the GaAs pHEMT**
Figure 4.29: Pinch-off voltage shift with respect to temperature of the GaN pHEMT

Figure 4.30 and 4.31 shows degradation of transconductance, $g_m$, with respect to temperature, both GaAs and GaN pHEMTs have the same trend of degradation of transconductance, this variation is greater for the GaN pHEMTs. The degradation of transconductance is due to the lower output current, $I_{ds}$, that happens at high temperature as output current decrease with increase in temperature. The degradation of $g_m$ is greater in the GaN pHEMTs because these devices are more sensitive to the change of temperature as compared with the GaAs transistors.

As the $g_m$ is directly related to output current $I_{ds}$, similar kind of comparison of the degradation of the output current $I_{ds}$ are shown in figure 4.32 and 4.33. A similar trend is seen and 4x50x0.15 $\mu$m$^2$ AlGaN/InGaN pHEMT is more susceptible to the heat effect and a bigger drop of output current is found. From the all DC temperature dependent characterisation of the both pHEMTs, the GaN device shows high temperature dependent behaviour as compared with the GaAs ones that studied in this project.
Figure 4.30: Degradation of $g_m$ with respect to the temperature of the GaAs pHEMT

Figure 4.31: Degradation of $g_m$ with respect to the temperature of the GaN pHEMT
Figure 4.32: Degradation of $I_{ds}$ with respect to the temperature of the GaAs pHEMT

Figure 4.33: Degradation of $I_{ds}$ with respect to the temperature of the GaN pHEMT
From the overall temperature dependent DC analysis of both 2x100x0.5 μm² AlGaAs/InGaAs/GaAs and 4x50x0.15 μm² AlGaN/InGaN pHEMTs from figure 4.28 to 4.33 shows two interesting phenomenon on their measured values, of those, one in lower temperature and another in higher temperature, which is due to the temperature effect and/or inherent behaviour of the devices. It is noticed that; this phenomenon arises before and after room temperature. That phenomenon is an important key for future temperature dependent high mobility electron transistor research.

This typical phenomenon represented in figure 4.34 and 4.35 for 2x100x0.5 μm² AlGaAs/InGaAs and 4x50x0.15 μm² AlGaN/InGaN pHEMTs respectively. Although the figure from 4.28-4.33 shows this phenomenon, it is shown only for tranconductance ($g_m$) here as transconductance ($g_m$) is an important parameter of pHEMTs for high frequency design.

![Temperature vs gm (mS)](chart.png)

Figure 4.34: Physical phenomenon with respect to temperature of the GaAs pHEMT
4.5.3 Small-Signal Temperature Dependent pHEMTs Modelling

An important part of the study involves developing linear temperature dependent small-signal models for the pHEMTs. For this study, Dambrine et al.'s [22] equivalent circuit model is adopted as discussed before. In this work, an automated parameter extraction procedure is used, which is developed and written in the Agilent’s IC-CAP using the parameter extraction language (PEL) [11]. Therefore, direct equivalent circuit parameters (ECPs) extractions can be achieved right after the on-wafer S-parameters measurements. In this work, comparison of both the $2\times100\times0.5$ μm$^2$ AlGaAs/InGaAs and $4\times50\times0.15$ μm$^2$ AlGaN/InGaN pHEMTs are made in order to investigate the sensitivity of both of these devices to thermal effects. Analyses of both sets of the extracted ECPs provide some valuable insights to the governing physics of the transistors which can be helpful for future designs and optimizations of multilayer 3D MMICs.
From the last section, temperature dependent DC characteristics of the 2x100x0.5 μm² AlGaAs/InGaAs and 4x50x0.15 μm² AlGaN/InGaN pHEMTs have been discussed. It is found that GaN pHEMT, compared to the GaAs pHEMT, are more sensitive to the change of temperature. For that reason, an essential study of the temperature dependent small-signal model for the both pHEMTs is required. The small-signal model is to be utilized as an accurate tool to predict the behaviour of the devices at high frequency can be obtained.

On-wafer S-parameters measurements are performed from 45MHz to 50GHz using HP8510C VNA controlled by the IC-CAP. Direct parameters extractions are then performed where it gives maximum transconductance, $g_m$. Temperature control is provided by Temptronic TP03200A varying from -40 to 150°C. Within this range of temperature and the bias point, the ECPs are expected to be linearly dependent with the temperature [7, 11, 71] and can be represented as in equation (2.47):

$$P(T) = P(T_0) [1 + B(T - T_0)]$$ (4.49)

where

- $B$ is the temperature coefficient (TC) in units per degree;
- $T_0$ is the reference temperature in 0°C, and
- $P(T_0)$ is the value of the parameter at the reference temperature.

### 4.5.3.1 Extrinsic Parameters Analysis

During the development of temperature-dependent small-signal model, extrinsic parameters, namely the device parasitics $C_{pg}$, $C_{pd}$, $L_s$, $L_g$, $L_d$, $R_s$, $R_g$, and $R_d$, are first extracted followed by the intrinsic parameters. The intrinsic parameters characterize the active region under the gate and are functions of biasing conditions, whereas the extrinsic parameters depend, at least to a first approximation, only on the technological parameters. Some of the intrinsic elements can be assumed linear for their weak dependence on the internal voltages;
those elements are $R_i$, $\tau$, and $C_{\text{dr}}$. In contrast, some of the extrinsic elements may be nonlinear if their dependence on the internal voltages is significant.

The parasitic capacitances and inductances are found to be unchanged with the temperature. As understood from the relationships between the small-signal parameters and the physical structure of the pHEMTs, $C_{\text{pg}}$ and $C_{\text{pd}}$ are the parasitic capacitances that are predominantly determined by the probing pads [3]. The pad capacitances come from the stray capacitance between the metal pads. The pad capacitance consists of crossover capacitance of the metal lines and the capacitance between the pad and the back face of the semi-insulating substrate, which is usually connected to the source terminal. However, the crossover capacitance is usually much smaller than the substrate capacitance [58]. $C_{\text{pg}}$ and $C_{\text{pd}}$ as being parasitic capacitances should not vary with temperature according to the definition of capacitance

$$C = \frac{\varepsilon_0 \varepsilon_r A}{d}$$

(4.50)

where

- $A$ is the cross sectional area of the pads
- $d$ is the distance between the pads
- $\varepsilon_r$ is the relative permeability of the material

Pads sizes, $A$, do not change with temperature as well as the distances, $d$, between them. Temperature coefficient of the dielectric constant of GaAs and GaN is about to $10^{-4}$; therefore the change should be minimal as shown figures 4.36 and 4.37. Pad capacitance values depend on the utilized layout. Pad capacitances can be estimated either from special structures without the active device or directly from S-parameter measurements using an optimization technique. Among the both pHEMTs in this study, GaN device shows higher pad capacitance value than that of GaAs ones.
Figure 4.36: Temperature dependent of $C_{pg}$ and $C_{pd}$ of the GaAs pHEMT

Figure 4.37: Temperature dependent of $C_{pg}$ and $C_{pd}$ of the GaN pHEMT
The parasitic inductances arise primarily from metal contact pads deposited on the device surface. So, the parasitic inductances, $L_s$, $L_d$ and $L_g$, relate to the physical structure of the pHEMTs. Fundamental definition of inductance suggests that the longer the trace, the greater inductance will be. The GaN pHEMT have longer interconnects, as can be observed in figure 4.2, suggesting greater inductances. However, on the other hand, the source pads of the GaN pHEMT are very much bigger than the GaAs ones. As wider conducting trace indicates lower inductance; therefore, lower $L_s$ could be expected. In addition, it also shows that $L_g$ has the highest values among the three. This can be explained by the fact that gate fingers are the narrowest and should thus possess greater inductances. Figures 4.38 and 4.39 shows the extracted values of these inductances and verifies the rationales above. Temperature wise, the parasitic inductances should not vary much with the temperature if one only considers the definition of the inductance. Available closed forms to calculate inductance normally depends on the parameters like number of turns, trace widths and lengths, spacing between traces [3]. None of the parameters defining that, the inductance is sensitive to the change of temperature.

![Figure 4.38: Temperature dependent of $L_s$, $L_d$ and $L_g$ of the GaAs pHEMT](image-url)
The terminal resistances of the devices, on the other hand, vary linearly with the temperature as shown in figure 4.40 and 4.41. It can be seen that the resistances of the 4x50x0.15 \( \mu m^2 \) AlGaN/InGaN pHEMT is greater than the 2x100x0.5 \( \mu m^2 \) AlGaAs/InGaAs pHEMT. This is because the overall physical dimensions of interconnects and probing pads of the GaN pHEMT are longer and bigger than the GaAs ones as can be seen in figure 4.2. The resistance is well understood to change with temperature. As known resistance increase as temperature increases; it is mainly due to the fact that both the conductivities of the metalization and the semiconductor are affected by the temperature. Among the three, \( R_g \) should be the lowest because it only consists of the metalization, whereas \( R_s \) and \( R_d \) are related to both the metalizations as well as the semiconductor access resistances. \( R_d \) should be the highest value as the distance from the gate to drain is 3-4 times bigger than the distance from gate to source in pHEMTs. The overall extrinsic parameter analysis the GaN pHEMT shows greater sensitivity to temperature than the GaAs ones.
Figure 4.40: Temperature dependent of R_s, R_d and R_g of the GaAs pHEMT

Figure 4.41: Temperature dependent of R_s, R_d and R_g of the GaN pHEMT
4.5.3.2 Intrinsic Parameters Analysis

In order to investigate the difference in temperature sensitivity between the 2x100x0.5 μm² AlGaAs/InGaAs and 4x50x0.15 μm² AlGaN/InGaN pHEMTs, intrinsic parameters are extracted and normalised to room temperature 25°C. Figures 4.42 to 4.47 show the temperature dependent intrinsic capacitances of the both device. The intrinsic capacitances are indicated here by C_{gs}, C_{gd}, and C_{ds}. C_{gs} and C_{gd} model the change in the depletion charge with respect to the gate-source and gate-drain voltages, respectively. The distribution of the depletion charge is symmetric with respect to the drain and source. The charge of the depletion region is shared between C_{gs} and C_{gd}. The drain-source Capacitance C_{ds} is included in the equivalent circuit on account for geometric capacitance effects between the source and drain electrodes. It is usually not considered to be bias dependent for the purposes of device modelling.

Under typical pHEMTs bias conditions C_{gs} is larger than C_{gd} because it models the change in depletion charge resulting from fluctuations in the gate-source voltage while the gate-source reverse bias voltage is less than the gate-drain reverse bias voltage. It is well known from depletion capacitance analysis that the depletion capacitance decreases as the reverse junction voltage increases. For this reason and under normal bias conditions, the gate-drain capacitance C_{gd} is considerably smaller in magnitude than C_{gs}. With the change of temperature, C_{gd} would change with respect to the change of depletion region. As discussed before, depletion region suffers from thermal effect, due to the fact C_{gd} is a small capacitance; the change in percentage is much greater.

On the other hand, the change in percentage seen in C_{ds} is smaller. C_{ds} is the only intrinsic capacitance, apart from g_m, that is having a negative temperature coefficient which means it decreases as the temperature goes higher. This suggests that a different degradation of the performance of the device as a smaller C_{ds} indicates a greater substrate current component.
Figure 4.42: Temperature dependent $C_{gs}$ of the GaAs pHEMT (normalised to 25°C)

Figure 4.43: Temperature dependent $C_{gs}$ of the GaN pHEMT (normalised to 25°C)
Figure 4.44: Temperature dependent of $C_{gd}$ of the GaAs pHEMT (normalised to 25°C)

Figure 4.45: Temperature dependent of $C_{gd}$ of the GaN pHEMT (normalised to 25°C)
Figure 4.46: Temperature dependent of $C_{ds}$ of the GaAs pHEMT (normalised to 25°C)

Figure 4.47: Temperature dependent of $C_{ds}$ of the GaN pHEMT (normalised to 25°C)
The transconductance of the device is one of the most important indicators of the device quality for microwave wave applications. Figures 4.48 and 4.49 represent the temperature dependent of $g_m$ of the 2x100x0.5 μm$^2$ AlGaAs/InGaAs and 4x50x0.15 μm$^2$ AlGaN/InGaN pHEMTs respectively. When all other characteristics are equal, a device with high transconductance will provide greater gains and superior high frequency performance.

As discussed before in chapter 2, section 2.5 that, in the saturation region the transconductance are affected by the factor $R_s$, it necessary to check this effect on the both pHEMTs. If the value of $R_s$ is zero then the extrinsic and intrinsic transconductance are equal. Figures 4.50 and 4.51 represent the change of temperature dependent intrinsic transconductance with respect to $R_s$ of the both pHEMTs.

![Figure 4.48: Temperature dependent of maximum of $g_m$ of the GaAs pHEMT (normalised to 25°C)](image-url)
Figure 4.49: Temperature dependent of maximum of $g_m$ of the GaN pHEMT (normalised to $25^\circ$C)

Figure 4.50: Temperature dependent degradation of transconductance due to source resistance of the GaAs pHEMT
The charging resistance $R_i$ represents an intrinsic resistance under the gate between the source and the channel, it is included primarily to improve the match to $S_{11}$. The output resistance $R_{ds}$ is the incremental resistance between drain and source, and it is more convenient to be explained in terms of its reciprocal, the output conductance $g_{ds}$. The output conductance is a measure of the incremental change in output current $I_{ds}$ with the output voltage $V_{ds}$. So, it can be defined as the slope of the $I_{ds}$-$V_{ds}$ characteristics with the gate-source voltage held constant. It plays a significant role in determining the maximum voltage gain attainable from a device and is extremely important for determining optimum output matching properties. As expected from the resistance response to the temperature change, both of $R_{ds}$ and $R_i$ show an increasing trend as the temperature increases is depicted in figures 4.52 to 4.55. The percentage of change in $R_i$ is greater because it is usually a very small resistance.
Figure 4.52: Temperature dependent of $R_i$ of the GaAs pHEMT (normalised to $25^\circ$C)

\[
\begin{align*}
\text{Ri}(\text{ohm}) & \quad \text{Temperature}(^\circ \text{C}) \\
\Delta \text{Ri}/\text{Ri}_{25^\circ \text{C}} (%) & \quad @ V_{gs} = -0.2 \text{ V and } V_{ds} = 3 \text{ V}
\end{align*}
\]

Figure 4.53: Temperature dependent of $R_i$ of the GaN pHEMT (normalised to $25^\circ$C)

\[
\begin{align*}
\text{Ri}(\text{ohm}) & \quad \text{Temperature}(^\circ \text{C}) \\
\Delta \text{Ri}/\text{Ri}_{25^\circ \text{C}} (%) & \quad @ V_{gs} = -4.8 \text{ V and } V_{ds} = 15 \text{ V}
\end{align*}
\]
Figure 4.54: Temperature dependent of $R_{ds}$ of the GaAs pHEMT (normalised to $25^\circ$C)

Figure 4.55: Temperature dependent of $R_{ds}$ of the $\mu m^2$ GaN pHEMT (normalised to $25^\circ$C)
The last intrinsic parameter, the time delay of the transconductance ($\tau$) of the 2x100x0.5 $\mu$m$^2$ AlGaAs/InGaAs and 4x50x0.15 $\mu$m$^2$ AlGaN/InGaN pHEMTs is shown in figure 4.56 and 4.57. The delay inherent to this process is described by the transconductance delay ($\tau$). It degrades at higher temperature suggesting a longer time delay. Figure 4.58 and 4.59 shows temperature dependent of $f_t$ and $f_{max}$ of the both pHEMTs. The degradations seen are dominantly caused by the degradation of $g_m$ seen from the figures 4.48 & 4.49. As known, the cut-off frequency is greatly affected by the transconductance $g_m$ of the device. Meanwhile the maximum frequency of oscillation can be maximised by the same factors as in the cut-off frequency and additional other factors like obtaining maximum $R_i/R_{ds}$ but minimal gate resistance $R_g$, minimal source resistance $R_s$, and small feedback capacitance $C_{gs}$. In order to validate this model, it is important to check the measured $f_t$ and $f_{max}$ from h$_{21}$ and MAG versus frequency which is shown in figure 4.60-4.63. Both of the measured and modelled data shows the similar trend of degradation as temperature increase.

\[ \tau(T) = 2\pi R_g(T)C_{gs}(T) \]

\[ \Delta \tau/\tau_{25\,\circ C} \ (\%) \]

@ V$_{gs} = -0.2$ V and V$_{ds} = 3$ V

Figure 4.56: Temperature dependent of $\tau$ of the GaAs pHEMT (normalised to 25$\circ$C)
Results and Discussions

\[
\tau(T) = 2\pi R_g(T)C_{gd}(T)
\]

@ Vgs = -4.8 V and Vds = 15 V

Figure 4.57: Temperature dependent of \(\tau\) of the GaN pHEMT (normalised to 25\(^\circ\)C)

\[
\begin{align*}
\tau &= \frac{g_m}{2\pi(C_{gs} + C_{gd})} \\
\Delta \tau/\tau_{25^\circ C} &= \left(\frac{\tau(T) - \tau_{25^\circ C}}{\tau_{25^\circ C}}\right) \\
\end{align*}
\]

\[
\begin{align*}
\tau &= \frac{R_g(T) + R(T)}{R_g(T)} \\
\tau_{\text{max}} &= 2\sqrt{\frac{\tau(T)}{f(T)}} \\
\end{align*}
\]

\(V_{gs} = -0.2\) V and \(V_{ds} = 3\) V

Figure 4.58: Modelled temperature dependent of \(f_t\) and \(f_{\text{max}}\) of the GaAs pHEMT
Figure 4.59: Modelled temperature dependent of $f_t$ and $f_{\text{max}}$ of the GaN pHEMT.

Figure 4.60: Measured temperature dependent of $f_t$ of the GaAs pHEMT.
Figure 4.61: Measured temperature dependent of $f_t$ of the GaN pHEMT

Figure 4.62: Measured temperature dependent of $f_{\max}$ of the GaAs pHEMT
Table 4.6 presents all the temperature dependent ECPs as well as the $f_t$ and $f_{\text{max}}$ with the associated temperature coefficients (TCs) with reference temperature at 0°C. It can be readily seen that all the ECPs of the GaN pHEMT are greater than the GaAs ones confirming GaN pHEMTs are more sensitive to the temperature. Applying temperature coefficients given in Table 4.6 to Equation (4.46) provides all the essential temperature dependent small-signal parameters. Temperature coefficients (TCs) for equivalent circuit parameters (ECPs) are calculated at fixed bias point; for GaAs pHEMT at $V_{gs} = -0.2$ V and $V_{ds} = 3$ V, meanwhile for GaN pHEMT at $V_{gs} = -4.8$ V and $V_{ds} = 15$ V.

Thermal effects on semiconductors can be summarised into the following important temperature dependent physical parameters: band-gap of the material, electron saturation velocity, electron mobility, built-in potential, barrier height of the material, dielectric constants and specific contact resistance [59]. The reason for the different TCs extracted for each ECPs is because all the temperature dependent physical parameters will have different degree of influence on the
respective ECPs. Comparing to published work in [11], all the extracted TCs of the both pHEMTs are found in similar fashion although different in magnitudes

### Table 4.6: Temperature coefficients (TCs) for equivalent circuit parameters (ECPs) and $f_t$ and $f_{\text{max}}$

<table>
<thead>
<tr>
<th>ECP</th>
<th>B($10^3$/°C) GaAs pHEMT</th>
<th>B($10^3$/°C) GaN pHEMT</th>
<th>B($10^3$/°C) GaAs pHEMT</th>
<th>B($10^3$/°C) GaN pHEMT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_s$ (Ω)</td>
<td>1.75</td>
<td>1.91</td>
<td>1.71</td>
<td>-</td>
</tr>
<tr>
<td>$R_d$ (Ω)</td>
<td>1.81</td>
<td>1.98</td>
<td>1.79</td>
<td>-</td>
</tr>
<tr>
<td>$R_g$ (Ω)</td>
<td>3.21</td>
<td>3.26</td>
<td>3.18</td>
<td>2.7</td>
</tr>
<tr>
<td>$C_{gd}$ (fF)</td>
<td>4.38</td>
<td>3.1</td>
<td>4.45</td>
<td>1.4</td>
</tr>
<tr>
<td>$C_{ds}$ (fF)</td>
<td>-1.94</td>
<td>-0.42</td>
<td>-1.87</td>
<td>-</td>
</tr>
<tr>
<td>$C_{gs}$ (fF)</td>
<td>0.4</td>
<td>0.39</td>
<td>0.4</td>
<td>0.34</td>
</tr>
<tr>
<td>$R_{ds}$ (Ω)</td>
<td>0.36</td>
<td>0.44</td>
<td>0.39</td>
<td>0.3</td>
</tr>
<tr>
<td>$R_i$ (Ω)</td>
<td>2.31</td>
<td>2.5</td>
<td>2.27</td>
<td>-</td>
</tr>
<tr>
<td>$g_{\text{ma}}$ (mS)</td>
<td>-1.56</td>
<td>-2.13</td>
<td>-1.44</td>
<td>-2.5</td>
</tr>
<tr>
<td>$\tau$ (pS)</td>
<td>2.85</td>
<td>3.38</td>
<td>2.3</td>
<td>-</td>
</tr>
<tr>
<td>$f_t$ (GHz)</td>
<td>-1.97</td>
<td>-2.25</td>
<td>-1.86</td>
<td>-</td>
</tr>
<tr>
<td>$f_{\text{max}}$ (GHz)</td>
<td>-2.89</td>
<td>-2.96</td>
<td>-2.66</td>
<td>-</td>
</tr>
</tbody>
</table>

For 2x100x0.5 μm² AlGaAs/InGaAs pHEMT

\[
R_s(T)=R_s(T_0)\left[1+1.75\times10^{-3}(T-T_0)\right] \tag{4.51}
\]

\[
R_d(T)=R_d(T_0)\left[1+1.81\times10^{-3}(T-T_0)\right] \tag{4.52}
\]

\[
R_g(T)=R_g(T_0)\left[1+3.21\times10^{-3}(T-T_0)\right] \tag{4.53}
\]

\[
C_{gd}(T)=C_{gd}(T_0)\left[1+4.38\times10^{-3}(T-T_0)\right] \tag{4.54}
\]

\[
C_{ds}(T)=C_{ds}(T_0)\left[1+1.94\times10^{-3}(T-T_0)\right] \tag{4.55}
\]

\[
C_{gs}(T)=C_{gs}(T_0)\left[1+0.4\times10^{-3}(T-T_0)\right] \tag{4.56}
\]
For 4x50x0.15 μm² AlGaN/InGaN pHEMT

\[ R_{ds}(T) = R_{ds}(T_0) \left[ 1 + 0.36 \times 10^{-3} (T - T_0) \right] \] (4.57)

\[ R_i(T) = R_i(T_0) \left[ 1 + 2.31 \times 10^{-3} (T - T_0) \right] \] (4.58)

\[ g_m(T) = g_m(T_0) \left[ 1 - 1.56 \times 10^{-3} (T - T_0) \right] \] (4.59)

\[ \tau(T) = \tau(T_0) \left[ 1 + 2.85 \times 10^{-3} (T - T_0) \right] \] (4.60)

\[ f_i(T) = f_i(T_0) \left[ 1 - 1.97 \times 10^{-3} (T - T_0) \right] \] (4.61)

\[ f_{\text{max}}(T) = f_{\text{max}}(T_0) \left[ 1 - 2.89 \times 10^{-3} (T - T_0) \right] \] (4.62)

The validation of the temperature dependent small-signal model is shown in figure 4.64 and 4.65 which indicates comparisons between the modelled and measured at 25°C and 125°C at the chosen bias point (\( V_{gs} = -4.8 \) V and \( V_{ds} = 15 \) V) for the 4x50x0.15 μm² AlGaN/InGaN pHEMT showing a good agreement.
Figure 4.64: Comparison between measured and simulated S-parameters of GaN pHEMT at 25°C

Figure 4.65: Comparison between measured & simulated S-parameters of GaN pHEMT at 125°C
To sum up all, DC characteristics, on-wafer RF S-parameters measurements, equivalent circuit model for the AlGaAs/InGaAs and AlGaN/InGaN pHEMTs are adopted and procedure of the extractions for each of the circuit parameters are presented and carried out. The developed small-signal models for both AlGaAs/InGaAs and AlGaN/InGaN pHEMTs are validated and compared to the measurements. The DC temperature dependent modelling of the pHEMTs, the change of DC characteristics of the pHEMTs to the change of temperature is observed and explained with the thermal effects.

The concept of the development of small-signal model is extended to temperature dependent small-signal model for both pHEMTs. Linear temperature dependent small-signal models for both AlGaAs/InGaAs and AlGaN/InGaN pHEMTs have been successfully developed using automated direct equivalent circuit parameters extractions from on-wafer S-parameters measurements. The models provide accurate predictions of the devices performance covering a temperature range from -40° to 150°C. A slight greater impact of thermal effects on AlGaN/InGaN pHEMTs is observed through the overall temperature coefficients found in these devices.
CHAPTER FIVE: CONCLUSIONS AND FUTURE WORKS

5.1 Conclusions

The characterisation and modelling of AlGaAs/InGaAs and AlGaN/InGaN pHEMTs has been successfully carried out in this work for the first time. A fast and accurate semi-automated circuit parameters extraction procedure is used. On-wafer S-parameters measurement data is directly fed into the extraction routine and a reliable and compact equivalent circuit model is thus established. This empirical process is extended to multiple bias conditions over a wide range of temperature and up to frequency of 40-50 GHz for pHEMTs. The two pHEMTs under investigation in this work have been analysed and compared by using DC and RF S-parameters measurements. It is found that different operating bias point; different output current and cut-off frequencies can be seen for those devices. The AlGaAs/InGaAs and AlGaN/InGaN pHEMTs have been carefully characterised by on-wafer measurements of DC and S-parameter measurements. In this work, an automatic data extraction tool has been used which is previously developed by using Agilent’s IC-CAP. By using the built-in Parameter Extraction Language (PEL), macro scripts are written to automate the measurements and extractions procedure in this tool. The extraction procedure used in this work does not involve optimisations and thus offer a fast and accurate way of modelling the device.

In order to extract the required equivalent circuit parameters (ECPs), three biasing conditions have been considered in the measured data. They are pinch-off, cold and hot biasing conditions. The hot biasing condition is chosen at the point where $V_{gs} = -0.2V$ and $V_{ds} = 3V$ and for AlGaAs/InGaAs pHEMT, $V_{gs} = -4.8V$. 
and $V_{ds} = 15V$ for AlGaN/InGaN pHEMT. Those points are selected to obtain the maximum transconductance, $g_{m}$, available in the pHEMTs studied. Small-signal models for each AlGaAs/InGaAs and AlGaN/InGaN pHEMTs have been developed. The validations of the models have been verified by comparing the data with the measured results. The simulation results of the generated small-signal models match very well with the measured data, especially from low frequency up to 20GHz.

Noise figure is an important parameter to characterise modern microwave devices. It is well-known that minimum noise figure of pHEMTs depends strongly on frequency and the important parasitic parameters: gate and source resistances, and gate-source capacitance. The values of these elements and the frequency can be considered as real variables so that noise figure can be expressed as a function depending on these variables. As small signal equivalent circuit including noise, temperature dependent noise figure modelling and characterisation is a key idea for future research. Among the both pHEMTs, GaN device shows better noise figure than that of GaAs ones at different frequencies.

The pHEMTs studied in this work have been designed for linear power amplifiers for future MMICs applications. Since enormous amount of heat can be generated during the operation of these circuits and the fact that the thermal conductivity of GaAs and GaN are so different, therefore the devices performances can be affected by the generated heat. Therefore an important part of this thesis was concerned with the study of the temperature characterisation of these devices. TEMTRONIC temperature control and a wafer chamber were used to measure the DC and S-parameters behaviours of these devices from -40 to 150°C. In comparison, GaN pHEMT have been observed to be more susceptible to the thermal effect than the GaAs. The difference with respect to temperature in the GaN pHEMTs is more prominent for example, a greater pinch-off voltage, $V_p$, shift is observed. These results are therefore suggesting that the GaN pHEMTs are more sensitive to the heat than those of GaAs devices.
A compact small-signal modelling technique for the pHEMTs has been established and this is extended for the temperature study with the aim of developing a novel temperature-dependent small-signal parameter model. For each device parameter a set of measurements has been taken at several temperatures covering the range from -40 to 150°C. Within this range of temperature, it was assumed that most of the equivalent circuit parameters (ECPs) can be expressed as linear equations with temperature coefficients (TCs). Extrinsic parameters, $C_{pg}$, $C_{pd}$, $R_s$, $R_d$, $R_g$, $L_s$, $L_d$ and $L_g$ are bias-independent and extracted using the given procedure. The study of these parameters indicated that the parasitic capacitances and inductances are unchanged with respect to the temperature. On the other hand, the extrinsic resistances were found to be linearly dependent with temperature.

All intrinsic parameters such as $C_{gs}$, $C_{gd}$, $R_s$ etc on the other hand, show a linear dependence with the temperature and the magnitude of most of these parameters increase with the increase of device temperature showing positive temperature coefficients. Drain-Source capacitance, $C_{ds}$, and transconductance, $g_m$, are the only two parameters which show negative temperature coefficients. It is also observed that the temperature coefficients for all the parameters are different because the thermal effects will have different degree of influence on the parameters. The degradation of $g_m$ can be explained in the same fashion as the degradation of $I_{ds}$ seen in DC. Lower output current at the same input voltage at higher temperature results in lower transconductance. As the $g_m$ is one of the most important parameters governing the performance of a device, the overall cut-off frequency, $f_c$, and maximum available gain frequency, $f_{max}$, are limited by the dominant effect of degradation of $g_m$ and this shows linear reductions with respect to temperature.

The tabulated extracted temperature coefficients for both AlGaAs/InGaAs and AlGaN/InGaN pHEMTs indicate greater temperature sensitivity for the GaN device. This is again another observation showing that GaN pHEMTs is more susceptible to the heat effects. Furthermore, the developed temperature-dependent small-signal models for both pHEMTs are validated to the measured data and showing a very good agreements. The overall effort in this work is focused on to
study the AlGaAs/InGaAs and AlGaN/InGaN pHEMTs using DC, RF, small signal parameter extraction, temperature dependent equivalent circuit parameters (ECPs) and thermal effects. By comparing the two pHEMTs, GaN device shows properties of high power, high temperature and high frequency electronic devices for future compact 3D multilayer MMICs. Table 5.1 shows some comparison of the achieved data of the two pHEMTs which carried out in this project.

Table 5.1: Comparison of the performance of the AlGaAs/InGaAs and AlGaN/InGaN pHEMTs

<table>
<thead>
<tr>
<th>Device Structure</th>
<th>Parameters</th>
<th>Description</th>
<th>GaAs</th>
<th>GaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>S (µm²)</td>
<td>Device physical dimensions</td>
<td>390x450</td>
<td>395x690</td>
<td></td>
</tr>
<tr>
<td>Lₙ (µm)</td>
<td>Gate lengths</td>
<td>0.5</td>
<td>0.15</td>
<td></td>
</tr>
<tr>
<td>Wₙ (µm)</td>
<td>Gate widths</td>
<td>2x100</td>
<td>4x50</td>
<td></td>
</tr>
<tr>
<td>A (µm²)</td>
<td>Gate Area</td>
<td>100</td>
<td>30</td>
<td></td>
</tr>
</tbody>
</table>

| DC Results       | V₉s (V)           | Gate – source voltage            | -0.2     | -4.8    |
| V₉ds (V)         | Drain – source voltage | 3      | 15      |
| gₙm (mS/mm)      | Transconductance/width | 280.7 | 372.2   |
| I₉ds (mA/mm)     | Drain current density | 155.8 | 352.1   |

<p>| RF Results       | C₉pg (fF)         | Parasitic gate capacitance       | 36.48    | 50.2    |
| C₉pd (fF)        | Parasitic drain capacitance | 61.30 | 85.78   |
| Lₙ (pH)          | Source inductance  | 2.91                             | 0.75     |
| Lₙ (pH)          | Drain inductance   | 65.25                            | 69       |
| Lₙ (pH)          | Gate inductance    | 133.6                            | 150      |
| Rₙ (Ω)           | Source resistance  | 2.5                              | 2.97     |
| Rₙ (Ω)           | Drain resistance   | 4.96                            | 5.71     |
| Rₙ (Ω)           | Gate resistance    | 1.92                            | 2.71     |
| C₉gd (fF)        | Gate-drain capacitance | 17.08   | 34.2    |
| C₉gs (fF)        | Gate-source capacitance | 428.5 | 152     |
| C₉ds (fF)        | Drain-source capacitance | 81.88 | 126.3   |
| R₉ds (Ω)         | Output resistance  | 540                             | 187      |
| R₉i (Ω)          | Input resistance   | 1.47                            | 1.6      |</p>
<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value 1</th>
<th>Value 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>$g_m$ (mS)</td>
<td>69</td>
<td>66.3</td>
</tr>
<tr>
<td>$g_m$(mS/mm)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Transconductance width</td>
<td>345</td>
<td>331.5</td>
</tr>
<tr>
<td>$\tau$ (pS)</td>
<td>0.21</td>
<td>0.58</td>
</tr>
<tr>
<td>$f_t$ (GHz)</td>
<td>24.6</td>
<td>56</td>
</tr>
<tr>
<td>$f_{\text{max}}$ (GHz)</td>
<td>97</td>
<td>105</td>
</tr>
<tr>
<td>NF $\text{min}$ (dB)</td>
<td>0.76</td>
<td>0.42</td>
</tr>
<tr>
<td>NF $\text{min}$ (dB)</td>
<td>1.49</td>
<td>0.83</td>
</tr>
<tr>
<td>NF $\text{min}$ (dB)</td>
<td>2.22</td>
<td>1.23</td>
</tr>
<tr>
<td>NF $\text{min}$ (dB)</td>
<td>2.94</td>
<td>1.61</td>
</tr>
</tbody>
</table>

Temperature coefficients (TCs) for equivalent circuit parameters (ECPs) $B$ ($x10^3/°C$)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value 1</th>
<th>Value 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_s$ ($\Omega$)</td>
<td>1.75</td>
<td>1.91</td>
</tr>
<tr>
<td>$R_d$ ($\Omega$)</td>
<td>1.81</td>
<td>1.98</td>
</tr>
<tr>
<td>$R_g$ ($\Omega$)</td>
<td>3.21</td>
<td>3.26</td>
</tr>
<tr>
<td>$C_{gd}$ (fF)</td>
<td>4.38</td>
<td>3.1</td>
</tr>
<tr>
<td>$C_{gs}$ (fF)</td>
<td>0.4</td>
<td>0.39</td>
</tr>
<tr>
<td>$C_{ds}$ (fF)</td>
<td>-1.94</td>
<td>-0.42</td>
</tr>
<tr>
<td>$R_{ds}$ ($\Omega$)</td>
<td>0.36</td>
<td>0.44</td>
</tr>
<tr>
<td>$R_i$ ($\Omega$)</td>
<td>2.31</td>
<td>2.5</td>
</tr>
<tr>
<td>$g_m$ (mS)</td>
<td>-1.56</td>
<td>-2.13</td>
</tr>
<tr>
<td>$\tau$ (pS)</td>
<td>2.85</td>
<td>3.38</td>
</tr>
<tr>
<td>$f_t$ (GHz)</td>
<td>-1.97</td>
<td>-2.25</td>
</tr>
<tr>
<td>$f_{\text{max}}$ (GHz)</td>
<td>-2.89</td>
<td>-2.96</td>
</tr>
</tbody>
</table>

As the gallium nitride (GaN) device has a wider band gap, larger breakdown voltage and higher saturation velocity than GaAs; the above comparison shows that the GaN device has the properties of candidate materials for high power, high temperature and high frequency electronic devices than the GaAs ones.
5.2 Future Works

The work in this project was to develop a linear temperature dependent small-signal models for both AlGaAs/InGaAs and AlGaN/InGaN pHEMTs. As the usefulness of a small-signal model, even a temperature dependent one, is hugely dependent on the specific applications and designs. It is imperative to extend the established techniques in this work to large-signal modelling. The future work of this project involves a more detailed look about the non-linearity of active devices:

- Study the non-linearity of the device at different input powers.
- Measuring the non-linearity of the device at different temperatures.
- Compare the non-linearity of GaAs HEMT with GaN HEMT devices.
- Develop a small theory about the non-linearity of the active devices.
- Develop a linear temperature dependent model of non-linearity of the active devices.
REFERENCES


[63] V. Kumar, W. Lu, R. Schwindt, A. Kuliev, G. Simin, J. Yang, M. Asif Khan,


[71] Tan, Jimmy Pang Hoaw, Thermal and Small-Signal Characterisation of AlGaAs/InGaAs pHEMTs in 3D Multilayer CPW MMIC, PhD thesis, Manchester, UK: The University of Manchester; 2011.
**APPENDIX 1: PROJECT PLAN**

<table>
<thead>
<tr>
<th></th>
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<tbody>
<tr>
<td>1) Study the non-linearity of the device at different input powers.</td>
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<tr>
<td>2) Measuring the non-linearity of the device at different temperatures.</td>
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<tr>
<td>3) Compare the non-linearity of GaAs HEMT with GaN HEMT devices.</td>
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<tr>
<td>4) Develop a small theory about the non-linearity of the active devices.</td>
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<tr>
<td>5) Develop a linear temperature dependent model of non-linearity of the active devices.</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>6) Writing-up</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>