MODELLING OF ADVANCED SUBMICRON GATE InGaAs/InAlAs pHEMTS AND RTD DEVICES FOR VERY HIGH FREQUENCY APPLICATIONS

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WARSUZARINA MAT JUBADI

School of Electrical and Electronic Engineering
# TABLE OF CONTENT

TABLE OF CONTENT ........................................................................................................ 2

LIST OF FIGURES AND ILLUSTRATIONS ...................................................................... 8

LIST OF TABLES .................................................................................................................. 15

LIST OF ABBREVIATIONS ................................................................................................. 17

ABSTRACT ........................................................................................................................... 19

DECLARATION ...................................................................................................................... 19

COPYRIGHT STATEMENT .................................................................................................. 21

ACKNOWLEDGEMENTS .................................................................................................... 22

DEDICATIONS ....................................................................................................................... 23

PUBLICATIONS ................................................................................................................... 24

1 CHAPTER 1 INTRODUCTION ............................................................................................ 25

1.1 Overview ....................................................................................................................... 25

1.2 Project Motivation and Objective ................................................................................ 26

1.3 Scope of thesis ............................................................................................................... 28

1.4 Thesis Outline .............................................................................................................. 28

2 CHAPTER 2 THEORY AND BACKGROUND OF PSEUDOMORPHIC
HIGH ELECTRON MOBILITY TRANSISTOR .................................................................. 31

2.1 Introduction ................................................................................................................... 31

2.2 Hetero Junction Structure ......................................................................................... 32

2.2.1 Lattice Matched and Pseudomorphic Material System ........................................ 34

2.2.2 Band Discontinuity ................................................................................................. 37

2.2.3 Quantum Well and 2-DEG ......................................................................................... 38

2.3 Metal Semiconductor Contacts ................................................................................. 39

2.3.1 Ohmic Contact ......................................................................................................... 39

2.3.2 Schottky Contact ..................................................................................................... 41

2.4 Introduction to High Electron Mobility Transistors (HEMTs) .................................... 45
3.6 Modelling the Physical Mechanisms .......................................................... 82
  3.6.1 Carrier Generation-Recombination Mechanisms ...................................... 83
  3.6.2 Traps and Defects .................................................................................. 87
3.7 Summary ..................................................................................................... 90

4 CHAPTER 4 TWO DIMENSIONAL PHYSICAL MODELLING OF ADVANCED In$_{0.7}$Ga$_{0.3}$As/In$_{0.52}$Al$_{0.48}$As pHEMTs ............................................................... 92
  4.1 Introduction .............................................................................................. 92
  4.2 Epitaxial Layer Structure ......................................................................... 93
  4.3 Mesh Definition for Device ..................................................................... 97
  4.4 Two Dimensional Device Structure .......................................................... 98
  4.5 Band Diagram and 2DEG in Physical Modelling ....................................... 100
  4.6 Modeling DC Characteristics ................................................................ 104
    4.6.1 Ideality factor and gate leakage current ......................................... 108
    4.6.2 Current-Voltage Characteristics ...................................................... 111
    4.6.3 Threshold Voltage and Transconductance ...................................... 115
    4.6.4 Modelling Impact Ionization in ATLAS ............................................ 117
    4.6.5 Kink Effect in Physical Modelling .................................................... 119
    4.7 RF Modelling for pHEMT device ......................................................... 123
    4.8 Summary .............................................................................................. 125

5 CHAPTER 5 EMPIRICAL MODELLING OF SUB-MICROMETER In$_{0.7}$Ga$_{0.3}$As/In$_{0.52}$Al$_{0.48}$As pHEMTs ................................................................. 126
  5.1 Introduction .............................................................................................. 126
  5.2 Empirical Device Modelling ................................................................... 126
  5.3 HEMT Small Signal Equivalent Circuit .................................................. 127
  5.4 Small Signal Model Parameters .............................................................. 128
    5.4.1 Extrinsic Elements Extraction ......................................................... 130
    5.4.2 Intrinsic Elements Extraction ......................................................... 131
  5.5 Large Signal Model for HEMTs .............................................................. 136
5.6 Steps in Device Modelling ................................................................. 137
5.7 pHEMT Device Structure ................................................................. 137
5.8 DC and RF Characteristics ............................................................... 140
5.9 Linear Model for device under test ................................................... 150
5.10 Nonlinear Modelling ....................................................................... 155
  5.10.1 DC Characteristics ................................................................... 155
  5.10.2 RF Performance ...................................................................... 157
5.11 Noise Model .................................................................................... 162
5.12 Summary .......................................................................................... 164

6  CHAPTER 6  DESIGN OF MONOLITHIC MICROWAVE INTEGRATED
CIRCUIT LOW NOISE AMPLIFIER USING In$_{0.7}$Ga$_{0.3}$As/In$_{0.52}$Al$_{0.48}$As
pHEMTs .................................................................................................. 165

6.1 Introduction ....................................................................................... 165
6.2 MMIC Technology ........................................................................... 166
6.3 Passive Component Design ............................................................... 167
  6.3.1 MMIC NiCr Resistor ................................................................. 168
  6.3.2 MMIC Capacitance ................................................................. 170
  6.3.3 Spiral Inductor for MMIC Inductance ..................................... 173
6.4 LNA Figure of Merits ....................................................................... 177
  6.4.1 Power Gain .............................................................................. 177
  6.4.2 Noise Figure ............................................................................ 179
3.3.1 6.2.3 Stability ........................................................................ 180
6.5 LNA Design Specifications ............................................................... 181
6.6 MMIC LNA Circuit Design ............................................................... 182
  6.6.1 Active Device .......................................................................... 183
  6.6.2 LNA Topology ......................................................................... 183
  6.6.3 Biasing Network ....................................................................... 185
  6.6.4 Matching Network .................................................................... 187
6.7 MMIC LNA Design for C-band Frequency (4-8 GHz) .......................... 188
6.8 MMIC LNA Design for 8-12 GHz (NF @ 8.4 GHz) .......................... 193
6.9 Summary .................................................................................. 197

7 CHAPTER 7 MODELLING OF ADVANCED In0.7Ga0.3As/AlAs
RESONANT TUNNELLING DIODE IN ATLAS SILVACO ................. 198

7.1 Introduction .............................................................................. 198
7.2 Principle of operations ............................................................... 199
7.3 Current-Voltage Characteristics ............................................... 201
7.4 RTD Device Structures ............................................................... 203
  7.4.1 Structure with Various AlAs barrier Thickness ......................... 204
  7.4.2 RTD Structure with Various Spacer Thicknesses ..................... 206
7.5 Analytical Modelling for RTD .................................................... 209
  7.5.1 Basic Tunnelling Current Equations ....................................... 209
  7.5.2 Physic-based Analytical Modelling ........................................ 209
7.6 Physical Modelling Approach for RTD ....................................... 212
  7.6.1 Quantum Tunnelling Process Simulation ............................... 213
  7.6.2 Non Equilibrium Green Function (NEGF) ............................ 214
  7.6.3 Mass Approximation ........................................................... 215
7.7 Results and Discussion ............................................................... 215
  7.7.1 Modelling with Spacer Thickness (tS) variations ...................... 216
  7.7.2 Doping Concentration .......................................................... 216
  7.7.3 Modelling with Barrier Thickness (tB) Variations .................... 218
  7.7.4 Quantum Well Thickness (tQW) effects in IV characteristics ...... 220
7.8 Optimisation of RTD Devices ................................................... 221
7.9 Summary .................................................................................. 223
8 CHAPTER 8  CONCLUSION AND FUTURE WORK ........................................ 224
8.1 Conclusions .......................................................................................................... 224
8.2 Future Work ........................................................................................................... 226
APPENDIX A: TWO PORT NETWORK AND S-PARAMETER....................... 228
APPENDIX B: TRANSFORMATION OF Z→Y PARAMETER ....................... 231
APPENDIX C: ............................................................................................................... 232
EE_HEMT1_Model (EEsof Scalable Nonlinear HEMT Model) ....................... 232
APPENDIX D: ............................................................................................................... 235
Material Parameters Used in XMBE131  pHEMT Device Physical Modelling..... 235
APPENDIX E: ............................................................................................................... 236
DECKBUILD File for XMBE308 RTD Device (QUANTUM MODELLING) 236
REFERENCES ............................................................................................................. 238
LIST OF FIGURES AND ILLUSTRATIONS

Figure 2.1  The energy gap of III–V compounds and ternary derivatives ..........32
Figure 2.2  Conceptual formation of (a) lattice matched, (b) lattice mismatched with defects, and pseudomorphic layers (c) Compressive and (d) Tensile strain .......36
Figure 2.3  Energy Band Diagrams for wide and narrow bandgap semiconductor ..37
Figure 2.4  An ideal undoped square shape quantum well (a) Structure, Energy band diagram, and (c) Conduction band diagram if AlGaAs is n-doped [35] .................39
Figure 2.5  Band diagram of a metal-semiconductor interface: (a) before contact and (b) after contact [33] ..........................................................................................40
Figure 2.6  Current conduction at Ohmic contact (a) via TFE in highly doped semiconductor and (b) via TE at low Schottky barrier interface [33] .................41
Figure 2.7  Energy and diagram of Schottky contact: (a) isolated and (b) on contact [33] ...........................................................................................................42
Figure 2.8  Current transport by thermionic emission in: ..................................43
Figure 2.9  Depletion type contacts to n-type substrates with increasing doping concentration \(N_D\): (a) Low \(N_D\), (b) Intermediate \(N_D\) and (c) High \(N_D\) [37] ..............44
Figure 2.10  Cross section of conventional HEMT with \(\delta\)-doped layer .........45
Figure 2.11  Conduction band of general depletion mode HEMT structure ...........47
Figure 2.12  Drain Current versus \(\delta\)-doping concentration variation [41] ..........48
Figure 2.13  Electron velocity as a function of electric field for variety of Indium (In) concentrations of InGaAs [24]. ........................................................................49
Figure 2.14  Ideal I-V characteristics of a MESFET [33] ..................................52
Figure 2.15  Transconductance extracted at different \(V_{ds}\) [44] .......................53
Figure 2.16  Frequency responses of a D-mode pHEMT under a fixed \(V_{DS}\) and \(V_{GS}\) 53
Figure 2.17  Id-Vg Characteristics as a function of Indium content in HEMT device [44] ..........................................................................................................57
Figure 2.18  \(I_D-V_{GS}\) characteristics at drain bias of 0.8V as a function of device gate length (nm). The inset presents a \(g_{m_{max}}\) at \(V_{ds}=0.8V\) [55] .........................58
Figure 2.19  Current gain \(f_T\) vs \(L_g\) for reported state-of-the-art MHEMTs, InP, HEMTs and GaAs PHEMTs [29] ..............................................................................59
Figure 2.20 Submicron Epilayer Structure and Gate Design: (a) T-Shape/Mushroom gate [18], (b) T-gate lattice-matched HEMT [14], (c) InAs channel HEMT [60], and (d) InGaN/InN/InGaN-based double channel HEMT [34] ........................................62

Figure 3.1 ATLAS Input-Output Hierarchy [80].................................................................70

Figure 3.2 ATLAS Command Groups Statement [80] ......................................................71

Figure 3.3 Epitaxial layer profile for Sample VMBE2100 used for device structure 73

Figure 3.4 Ohmic Contact and Schottky contact defined in VMBE2100 pHEMT model. The source and drain electrode are stretched until the end of the channel layer .................................................................................................................................................75

Figure 3.5 Band profile for a HEMT as a function of sheet concentration ..............77

Figure 3.6 The electron concentration in δ-doped layer and carrier concentration in Channel layer for XMBE2100 structure ......................................................................................78

Figure 3.7 Energy band diagram for the VMBE2100 pHEMT structure model in ATLAS..................................................................................................................................................79

Figure 3.8 Simulations of Electron Mobility in the Channel Layer (In$_{0.7}$Ga$_{0.3}$As material) .........................................................................................................................................................81

Figure 3.9 Definition of the trap energy level for acceptor and donor traps in reference to the conduction and valence band edges [80]..........................................................87

Figure 3.10 Carrier Capturing/Releasing Mechanism in Acceptor-Like Traps [80] 88

Figure 3.11 Modelled I-V characteristics for VMBE2100 with Trap (red line) .......88

Figure 3.12 Trap density, N$_T$ value effects on the current-voltage characteristics ... 89

Figure 3.13 The Shift in Threshold Voltage, V$_T$ due to Trap Density, N$_T$ ...........90

Figure 4.1 Epitaxial layer structures for various in-house fabricated pHEMT samples .........................................................................................................................................................94

Figure 4.2 Schematic view of 0.25μm InGaAs/InAlAs/InP pHEMT XMBE131 with Pd/Ti/Au gate scheme as compared to the Ti/Au gate metallisation (Adapted from [98]) ............................................................................................................................................95

Figure 4.3 Device Mesh Structure for pHEMT structure which defined with non-cylindrical mesh for (a) VMBE2100 and (b)XMBE131 ...................................................98

Figure 4.4 Schematic device structure for VMBE2100 showing epitaxial layers (size not to scale) .........................................................................................................................99

Figure 4.5 Schematic device structure for XMBE131 epitaxial layers (size not to scale) .........................................................................................................................99
Figure 4.6 Energy band diagram (at thermal equilibrium) for VMBE2100 epitaxial layer simulated with ATLAS Silvaco ................................................................. 100
Figure 4.7 Energy band diagram for the XMBE131 structure (at thermal equilibrium) simulated with ATLAS Silvaco ................................................................. 101
Figure 4.8 Tonyplot visualization of Electron Concentration and Sheet Carrier Density for (a) Single- and (b) Double Delta doping layer ........................................ 102
Figure 4.9 (a) Sheet concentration (2DEG) and (b) Band diagram simulated at different biasing voltage (for VMBE2100 structure) ........................................... 103
Figure 4.10 pHEMT sample VMBE2100 (1 \( \mu \)m gate length) characteristics (a) Normalized current-voltage characteristics, (b) Threshold Current, \( V_{TH} \), (c) Normalized transconductance, \( g_m \) with \( g_m=940 \text{mS/mm} \) at \( V_{DS}=2 \text{V} \) and (d) on-state leakage current where \( V_{DS}=0 \) to \( 2 \text{V} \) with 250mV steps .................................................. 105
Figure 4.11 pHEMT sample XMBE131, 0.25\( \mu \)m gate length (Pd gate metallisation) (a) Normalized current-voltage characteristics with maximum drain current, (b) Threshold Current, \( V_{TH} \), (c) Normalized transconductance, \( g_m \) with \( g_m=940 \text{mS/mm} \) at \( V_{DS}=2 \text{V} \), (d) on-state leakage current where \( V_{DS}=0 \) to \( 2 \text{V} \) with 250mV steps and (e) Off-state leakage current ......................................................................................... 107
Figure 4.12 Typical Schottky diode forward current characteristic of InP pHEMT 108
Figure 4.13 Schottky diode forward current characteristic of XMBE131 pHEMT modelled with different work function value .............................................. 110
Figure 4.14 Simulated I-V Curve (with and without) Mobility Model for VMBE2100 ............................................................................................................ 112
Figure 4.15 Current-Voltage Characteristics for normalised 4x200\( \mu \)m VMBE2100 pHEMT when only trapping mechanism activated, \( N_T=2e17 \text{cm}^3 \) (without impact ionisation) .................................................................................. 113
Figure 4.16 Modelled vs Measured I-V Characteristic for VMBE2100 ............... 113
Figure 4.17 Modelled vs. Measured \( V_T \) at \( V_{ds}=1 \text{V} \) for VMBE2100 pHEMT ......... 114
Figure 4.18 Current-Voltage Characteristics for normalised 2x50\( \mu \)m XMBE131 pHEMT (optimised with trap, impact model) ............................................ 114
Figure 4.19 \( I_{DS}-V_{GS} \) at \( V_{DS}=1 \text{V} \) for normalised 2x50\( \mu \)m XMBE131pHEMT (optimised modelled vs. measured) .................................................. 116
Figure 4.20 Transconductance (meas. Vs modelled) for normalised 2x50\( \mu \)m XMBE131pHEMT at \( V_{ds}=1 \text{V} \) ........................................................................................................ 116
Figure 4.21  2D Contour of Impact Ionisation rate in VMBE2100 Device Model:118
Figure 4.22  I-V Characteristic with Impact Ionization:119
Figure 4.23  Kink mechanism as explained by Somerville [38]  (a) Simplified device cross-section used for the model. (b) Energy bands within the extrinsic source adjacent to the gate as a function of time. (c) Drain current characteristics as a function of time.118
Figure 4.24 Kink Effect Anomalies in I-V Characteristics as a Function of Trap Density: (a) $\Delta I_{\text{kink}}$ is higher for high $N_T$ [111] for AlGaN/GaN HEMT and (b) Simulated I-V characteristics with $N_T=5\times10^{17}\text{cm}^{-3}$120
Figure 4.25 The $\Delta I_{\text{kink}}$ analysis in I-V Characteristics with different trap $N_T$ value 122
Figure 4.26 Measured vs modelled cut-off frequency, $f_T$ for XMBE131 pHEMT sample123
Figure 4.27 Measured vs modelled maximum frequency, $f_{\text{max}}$ for XMBE131 pHEMT sample123
Figure 4.28 Measured vs modelled S-parameter (a) S21, S12 and (b) S11, S22 for XMBE131 pHEMT sample124
Figure 5.1 Physical origin of the HEMT small signal equivalent circuit model [110]127
Figure 5.2 Standard form of HEMT small signal equivalent circuit [18]128
Figure 5.3 Equivalent Circuit Model for FET Cold Bias Condition [18]130
Figure 5.4 Method for extracting the device intrinsic Y matrix [105]134
Figure 5.5 An illustration of a submicron device with a T-gate structure.140
Figure 5.6 pHEMT sample XMBE131 (Ti/Au gate metallisation) (a) Normalized I-V characteristics with maximum $I_{DS}=540\text{mA/mm}$ at $V_{DS}=1\text{V}$, (b) Threshold Voltage, $V_{TH}$, (c) Normalized transconductance, $g_m$ with $g_m=940\text{mS/mm}$ at $V_{ds}=2\text{V}$ and (d) on-state leakage current where $V_{ds}=0$ to $2\text{V}$ with $250\text{mV}$ steps.142
Figure 5.7 Unity gain frequency, $f_T$ and maximum frequency, $f_{\text{max}}$ at $V_{ds}=1\text{V}$, $I_{DS}=13.19\text{mA}$ for sample XMBE131143
Figure 5.8 pHEMT sample VMBE1998 (a) Normalized I-V characteristics with maximum $I_{DS}=321\text{mA/mm}^2$ (2x50$\mu$m) and $I_{DS}=309\text{mA/mm}^2$ (2x200$\mu$m) at $V_{ds}=1\text{V}$, (b) Threshold Voltage, $V_T$ at -0.89V for both device size, (c) Normalized transconductance, $g_m$ with $g_m=529\text{mS/mm}$ (2x50$\mu$m) and $g_m=500\text{mS/mm}$
(2x200μm) at \( V_{ds} = 2V \) and (d) Off-State Gate Current Leakage: Forward and Reversed

Figure 5.9  RF characteristics for pHEMT sample VMBE1998, 2x50 μm and 2x200 μm (a) Cut-off frequency, \( f_T \) at \( V_{DS} = 1V \), 80% \( g_{m_{max}} \) and (b) Maximum frequency, \( f_{max} \) extrapolated at \( V_{DS} = 1V \), 80% \( g_{m_{max}} \)

Figure 5.10  pHEMT sample XMBE56 (a) Normalized I-V characteristics with maximum \( I_{DS} = 450 \text{ mA/mm}^2 \) (2x50μm) and \( I_{DS} = 385 \text{ mA/mm}^2 \) (2x200μm) at \( V_{ds} = 1V \), (b) Threshold Voltage, \( V_T \) at -0.98V (2x50μm) and \( V_T \) at -1.0V (2x200μm), (c) Normalized transconductance, \( g_m \) with \( g_m = 430 \text{ mS/mm} \) (2x50μm) and \( g_m = 380 \text{ mS/mm} \) (2x200μm) at \( V_{ds} = 1V \), (d) Off-State Gate Current Leakage: forward and reverse and (e) on-state leakage current for \( V_{ds} = 0 \) to 2V

Figure 5.11 (a) Schematic and (b) Equivalent transistor linear model [122]

Figure 5.12 Circuit Setup for Extrinsic element extraction (pinched) in ADS for XMBE131

Figure 5.13 Parameter extraction setup for Hot measurement

Figure 5.14 EEHEMT models for initial current-voltage parameter for DC models

Figure 5.15 Measured versus modelled XMBE131 pHEMT (a) I-V characteristics (for \( V_{GS} = 0.1 \text{ V to -0.8V, -0.1V steps} \)), (b) threshold voltage (for \( V_{DS} = 1V \) to 2V, 0.25V steps)

Figure 5.16 Curve fitting for 2x50μm XMME131 (a) Forward and Reverse Gain and (b) Input and output reflection coefficient over frequency 40 MHz to 20 GHz measured at 80% of maximum \( g_m \)

Figure 5.17 A Complete transistor model for XMBE131 2 x 50 μm pHEMT

Figure 5.18 Summary of curve fitting for 2 x 200 μm on VMBE1998 (a) I-V curve (b) Transconductance (c) Forward and reverse gain and (b) Reflection coefficient against frequency

Figure 5.19 Summary of curve fitting for 2 x 200 μm on XMBE56 (a) I-V curve (b) Transconductance (c) Forward and reverse gain and (b) Reflection coefficient against frequency

Figure 6.1 Equivalent circuit model for NiCR resistor

Figure 6.2 NiCr resistors modelled in ADS
Figure 6.3 Layout design of MMIC NiCr resistor (7.5 kΩ) with total wire length, L=3100 μm and wire width, W=20 μm.

Figure 6.4 An example for coplanar interdigital capacitor for MMICs [139].

Figure 6.5 Equivalent circuit for MMIC Capacitance.

Figure 6.6 Modelled circuit for MIM Capacitor setup in ADS.

Figure 6.7 S-parameter results for an 8pF MIM capacitor over the frequency.

Figure 6.8 Equivalent circuit for spiral inductor.

Figure 6.9 Schematic of equivalent circuit for spiral Inductor modelled in ADS.

Figure 6.10 S-parameter for 14 nH Spiral inductor over wide range frequency.

Figure 6.11 Layout design for 14 nH Spiral inductor.

Figure 6.12 Power reflection coefficients for a 2-port microwave network [110].

Figure 6.13 Reflection coefficients for a general microwave 2-port network.

Figure 6.14 Schematic diagrams of basic LNA topologies [43].

Figure 6.15 Inductive Peaking Schematic [142].

Figure 6.16 Graph of typical I-V characteristic and operating bias point for HEMT.

Figure 6.17 Circuit diagram of pHEMT with biasing circuit with inductor.

Figure 6.18 General Input and output circuit of 2-port network.

Figure 6.19 Single Stage circuit for 4-8 GHz frequency range.

Figure 6.20 Gain, Noise figure, Stability and Input and output reflection results.

Figure 6.21 Double Stage LNA circuit for 4-8 GHz frequency range.

Figure 6.22 The gain, input and output reflection results for C-band Double-stage LNA.

Figure 6.23 Single Stage circuit for 8-12 GHz frequency range.

Figure 6.24 Gain, Noise figure and Input/output reflection results for SSLNA at 8-12 GHz frequency range.

Figure 6.25 Double Double Stage LNA (DSLNA) circuit for 8-12 GHz frequency range.

Figure 6.26 Maximum Gain, Noise Figure, Stability factor, and input and output reflection results for DSLNA operating at 8-12 GHz.

Figure 7.1 Schematic of RTD Structure [153].

Figure 7.2 Energy band diagrams of an RTD and the corresponding IV curve [154].
Figure 7.3 Generic I-V characteristic of an RTD, showing peak

Figure 7.4 Generic epilayer structure of RTD using In_{0.8}Ga_{0.2}As/AlAs material system studied in this project

Figure 7.5 Band diagram and doping profile for XMBE277 RTD (size 3\(\mu\)m x 3\(\mu\)m)

Figure 7.6 IV Characteristics for various samples RTD with different barrier thicknesses

Figure 7.7 IV Characteristics for various samples RTD with different spacer thicknesses

Figure 7.8 Modelled and measured current density for sample XMBE277 (a) on large area mesa (3\(\mu\)m x 3\(\mu\)m) and (b) on sub-micrometre area mesa (2\(\mu\)m x 0.35\(\mu\)m)

Figure 7.9 Electron particle-wave duality (quantum tunnelling) [143]

Figure 7.10 A Symmetrical double barrier regions in RTD

Figure 7.11 I-V Characteristics (XMBE277 RTD) with various spacer thicknesses

Figure 7.12 Modelled and measured IV for XMBE301 RTD with doping variations

Figure 7.13 Modelled and measured IV for XMBE301 RTD with doping variations

Figure 7.14 I-V Characteristics (XMBE302 RTD) with various barrier thicknesses

Figure 7.15 I-V Characteristics (XMBE308 RTD) with various barrier thicknesses

Figure 7.16 Optimised model for XMBE308 with barrier thickness modification

Figure 7.17 Modelled IV Characteristics for XMBE301 RTD with t_{QW} variations

Figure 7.18 Optimised IV characteristics for RTD device sample:
LIST OF TABLES

Table 2.1 Lattice constant and energy band gap of common III-V binary and ternary compound semiconductors at 300 K [26, 27] .................................................. 33

Table 3.1 VMBE2100 Electrodes definition in ATLAS ........................................... 74
Table 3.2 Parameters to specify a doping profile [80] .............................................. 76
Table 3.3 Generation/Recombination Mechanism Models .................................... 83
Table 4.1 Hall measurement data at 300 K (room temperature) and 77 K for VMBE2100 and XMBE131 pHEMT device ................................................................. 96
Table 4.2 Ideality factor (n) measurement data vs modelled with various metal work function ........................................................................................................... 110
Table 4.3 Impact Ionization Parameters Applied for the Modelling [45] ............... 117
Table 5.1 Epitaxial structure for various pHEMT samples fabricated at the University of Manchester ................................................................. 138
Table 5.2 Hall measurement data at 300 K (room temperature) and 77 K for VMBE1998, XMBE56 and XMBE131 pHEMT device .................................................. 139
Table 5.3 Biasing for in-house fabricated pHEMT sample devices (a $V_{DS}=1V$) .... 141
Table 5.4 Ideality factor and Barrier height for VMBE1998 pHEMT sample ........... 145
Table 5.5 Ideality factor and Barrier height for XMBE56 pHEMT sample .......... 149
Table 5.6 Transconductance and RF characteristics XMBE56 pHEMT sample .... 149
Table 5.7 Table of Extrinsic values for various pHEMT sample devices ($V_{DS}=1V, 80\% \text{ gm}_{\text{max}}$ or $\sim 10\% \text{ Idss}$) ................................................................. 152
Table 5.8 Table of intrinsic parameters for all devices at $V_{DS}=1V, 10\% \text{ I}_{\text{DSS}}$ ....... 154
Table 5.9 Noise performance for fabricated pHEMT devices at $V_{DS}=1V, 10\% \text{ I}_{\text{DSS}}$ ................................................................................................. 163
Table 6.1 Parameter value used for in-house fabricated spiral inductor ................. 175
Table 6.2 Specification for SSLNA and DSLNA in C-band frequency ............... 188
Table 6.3 Component values used in C-band DSLNA design ......................... 191
Table 6.4 Target Specification for X-band LNA compared to related works ....... 193
Table 7.1 RTD Epitaxial Structure (XMBE277, t_b=13 Å, 1ML ~ 2.7 Å [143]) ...... 205
Table 7.2 Peak current density and PVCR for various RTD sample [142] ......... 206
Table 7.3 RTD Epitaxial Structure (XMBE308, t_s=25Å, 1 ML ~2.9 Å [143]) ...... 207
Table 7.4 Figure of merits for various RTD samples .................................... 208
Table 7.5 Fitting parameters for large area and submicron RTD on sample XMBE277 .......................................................... 212
Table 7.6 Optimised parameter value for various device structures ................. 221
<table>
<thead>
<tr>
<th><strong>Abbreviation</strong></th>
<th><strong>Definition</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>2DEG</td>
<td>Two-Dimensional Electron Gas</td>
</tr>
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<td>ADS</td>
<td>Advanced Design System</td>
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<td>ASKAP</td>
<td>Australian SKA Pathfinder</td>
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<td>Coplanar Waveguide</td>
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<td>Direct Current</td>
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<td>Heterojunction Bipolar Transistor</td>
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<tr>
<td>HEMT</td>
<td>High Electron Mobility</td>
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<td>ICCAP</td>
<td>Integrated Circuit Characterization and Analysis Program</td>
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<tr>
<td>IF</td>
<td>Intermediate Frequency</td>
</tr>
<tr>
<td>LNA</td>
<td>Low Noise Amplifier</td>
</tr>
<tr>
<td>MBE</td>
<td>Molecular Beam Epitaxy</td>
</tr>
<tr>
<td>MESFET</td>
<td>Metal Semiconductor Field Effect Transistor</td>
</tr>
<tr>
<td>MMIC</td>
<td>Monolithic Microwave Integrated Circuit</td>
</tr>
<tr>
<td>MOCVD</td>
<td>Metal-oxide Chemical Vapour Deposition</td>
</tr>
<tr>
<td>MODFET</td>
<td>Modulation Doped FET</td>
</tr>
<tr>
<td>M&amp;N</td>
<td>Microelectronic and Nanostuctures</td>
</tr>
<tr>
<td>NF</td>
<td>Noise Figure</td>
</tr>
<tr>
<td>$NF_{\text{min}}$</td>
<td>Minimum Noise Figure</td>
</tr>
<tr>
<td>pHEMT</td>
<td>Pseudomorphic High Electron Mobility Transistor</td>
</tr>
<tr>
<td>PNA</td>
<td>General-purpose Network Analyser</td>
</tr>
<tr>
<td>QW</td>
<td>Quantum Well</td>
</tr>
<tr>
<td>RF</td>
<td>Radio Frequency</td>
</tr>
<tr>
<td>RTD</td>
<td>Resonant Tunnelling Diode</td>
</tr>
</tbody>
</table>
**SDHT**  
Selectively Doped Heterostructure Transistors

**SKA**  
Square Kilometre Array

**TEGFET**  
Two Dimensional Electron Gas Field Effect Transistors

### Notations

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{ds,gs}$</td>
<td>Drain/gate to source capacitance</td>
</tr>
<tr>
<td>$C_{gd}$</td>
<td>Drain to gate capacitance</td>
</tr>
<tr>
<td>$C_{pg,pd,ps}$</td>
<td>Pad capacitances to electrodes</td>
</tr>
<tr>
<td>$\Delta E_c$</td>
<td>Conduction band discontinuity</td>
</tr>
<tr>
<td>$\Delta E_g$</td>
<td>Band gap difference of heterojunction materials</td>
</tr>
<tr>
<td>$\Delta E_v$</td>
<td>Valence band discontinuity</td>
</tr>
<tr>
<td>$E_g$</td>
<td>Band gap energy</td>
</tr>
<tr>
<td>$E_{br}$</td>
<td>Breakdown voltage</td>
</tr>
<tr>
<td>$E_{fn}$</td>
<td>Electron Quasi fermi level</td>
</tr>
<tr>
<td>$E_F$</td>
<td>Fermi Level</td>
</tr>
<tr>
<td>$L_{g,s,d}$</td>
<td>Gate/Source/Drain contact inductance</td>
</tr>
<tr>
<td>$N_C$</td>
<td>Effective density of states</td>
</tr>
<tr>
<td>$P$</td>
<td>Polarization</td>
</tr>
<tr>
<td>$P_{sp}$</td>
<td>Spontaneous polarization</td>
</tr>
<tr>
<td>$P_{pz}$</td>
<td>Piezo-electric polarization</td>
</tr>
<tr>
<td>$q$</td>
<td>Electron charge</td>
</tr>
<tr>
<td>$R_{g,s,d}$</td>
<td>Gate/Source/Drain contact resistance</td>
</tr>
<tr>
<td>$R_{ds,gs}$</td>
<td>Drain/gate to source resistance</td>
</tr>
<tr>
<td>$v_{sat}$</td>
<td>Saturation velocity</td>
</tr>
<tr>
<td>$V_T$</td>
<td>Threshold voltage of HEMT</td>
</tr>
<tr>
<td>$x_{AlGaN}$</td>
<td>Aluminium molefraction in GaN</td>
</tr>
<tr>
<td>$\mu$</td>
<td>Carrier Mobility</td>
</tr>
</tbody>
</table>
ABSTRACT

The University of Manchester
Candidate: Warsuzarina binti Mat Jubadi
Degree: Doctor of Philosophy (PhD)
Thesis Title: Modelling of Advanced Submicron Gate InGaAs/InAlAs pHEMTs and RTD Devices for Very High Frequency Circuits
Date: May 2015

InP-based InAlAs/InGaAs pseudomorphic High Electron Mobility Transistors (pHEMTs) have shown outstanding performance; this makes them prominent in high frequency mm-wave and submillimeter-wave applications. However, conventional InGaAs/InAlAs pHEMTs have major drawbacks, i.e., very low breakdown voltage and high gate leakage current. The optimisation of InAlAs/InGaAs epilayer structures through advanced bandgap engineering offers a key solution to the problem. Concurrently, device modelling plays a vital role in the design and analysis of pHEMT devices and circuit performance.

In this research, two-dimensional (2D) physical modelling of 1 μm and sub-μm gate length strained channel InAlAs/InGaAs/InP pHEMTs has been developed, in ATLAS Silvaco. All modelled devices were optimised and validated by experimental devices, which were fabricated at the University of Manchester. An underlying device physics insight is gained, i.e., the effect of changes to the device’s physical structure, theoretical concepts and its general operation, and a reliable pHEMT model is obtained. The kink anomalies in the I-V characteristics were reproduced. The 2D simulation results demonstrate an outstanding agreement with measured DC and RF characteristics.

The aim of developing linear and non-linear models for sub-μm transistors and their implementation in MMIC LNA design is achieved with the 0.25 μm In\textsubscript{0.7}Ga\textsubscript{0.3}/Al\textsubscript{0.48}As/InP pHEMT. An accurate method for the extraction of empirical models for the fabricated active devices has been developed using the Advance Design System (ADS) software. The results demonstrate excellent agreement between experimental and modelled DC and RF data. Precise models for MMIC passive devices are also obtained, and incorporated in the proposed design for a single- and double-stage Monolithic Microwave Integrated Circuit (MMIC) low noise amplifiers (LNAs) at C- and X-band frequencies. The single-stage LNA is designed to achieve a maximum gain ranging from 9 to 13 dB over the band of operation, while the gain is increased to between 20 dB and 26 dB for the double-stage LNA designs. A noise figure of less than 1.2 dB and 2 dB is expected, for the C- and X-band LNAs respectively, while retaining stability across all frequency bands.

Although the RF performance of pHEMT is being vigorously pushed towards the terahertz (THz) region, novel devices such as the Resonant Tunnelling Diode (RTD) are needed to support future ultra-high-speed, high-frequency applications. Hence, the study of physical modelling is extended to quantum modelling of an advanced In\textsubscript{0.8}Ga\textsubscript{0.2}/AlAs RTD device. The aim is to model both large-size and submicron RTDs, using Silvaco’s ATLAS software to reproduce the peak current density, peak-to-valley-current ratio (PVCR), and negative differential resistance (NDR) voltage range. The physical modelling for the RTD devices is optimised to achieve an excellent match with the fabricated RTD devices; variations in the spacer thickness, barrier thickness, quantum well thickness and doping concentration are included.
DECLARATION

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Special thanks to my beloved husband and kids, I dedicated a special and heartiest tribute to them for the understanding, help, and support throughout the years of my research. This contribution also dedicated to my beloved father, whose just passed away during the 3rd year of my PhD journey. With half of my strength almost gone, a great family support made me able to move on with the study.

Finally, I would like to acknowledge my sponsors, the Ministry of Education, Malaysia (MOE), and Universiti Tun Hussein Onn Malaysia (UTHM) for providing me an opportunity to pursue my PhD in the UK with their financial support.
DEDICATIONS

to my beloved husband Mohd Sophian

to my lovely children Adam and Aiman

to my beautiful babies

to my mother and my late father

to my family members
PUBLICATIONS

LIST OF JOURNAL PUBLICATIONS

1. F Packeer, M Mohamad Isa, W Mat Jubadi, K W Ian and M Missous, “Fabrication and characterization of tensile In$_{0.3}$Al$_{0.7}$As barrier and compressive In$_{0.7}$Ga$_{0.3}$As channel pHEMTs having extremely low gate leakage for low-noise applications”, J. Phys. D: Appl. Phys. 46 (2013) 264002 (7pp). doi:10.1088/0022-3727/46/26/264002


LIST OF CONFERENCES


2. W.M.Jubadi, M.Muhammad Isa and M. Missous, “Physical and Empirical Modelling of Highly Strained In$_{0.7}$Ga$_{0.3}$As/In$_{0.3}$Al$_{0.7}$As pHEMT Device”, School of Electrical and Electronic Engineering Postgraduate (2nd Year) Poster Conference, The University of Manchester, 22 Nov 2012.


4. W.M.Jubadi, K.W Ian, F.Packeer and M. Missous, “Optimization of Two Dimensional and Empirical Modelling of 0.25μm In$_{0.7}$Ga$_{0.3}$As/In$_{0.52}$Al$_{0.48}$As pHEMT Device for X-band MMIC Low Noise Amplifier”, UK Semiconductor 2012 Conference, Sheffield Hallam University, 9 July 2014.

5. F. Packeer, Warsuzarina Mat Jubadi and M. Missous “New Submicron Low Gate Leakage In$_{0.52}$Al$_{0.48}$As-In$_{0.7}$Ga$_{0.3}$As pHEMT for Low Noise Applications” in UK Semiconductor 2014 Conference, Sheffield Hallam University, 9 July 2014.
1 CHAPTER 1

INTRODUCTION

1.1 Overview

The High Electron Mobility Transistor (HEMT) and Pseudomorphic High Electron Mobility Transistor (pHEMT) are Field Effect Transistors (FET). HEMTs operate in a similar manner to MESFETs, but extend the performance of FET by taking advantage of the large band discontinuities in the band structures of the constituent semiconductor materials. The HEMT structure consists of compositional compound materials that are lattice-matched to the substrate. However in the pHEMT structure, the channel material is so thin that the crystal lattice stretches “pseudomorphically” to occupy the spacing of the nearby material. Consequently, it allows better performance due to the larger bandgap difference compared to the lattice-matched structure. The formation of a quantum well and the two dimensional electron Gas (2DEG) in the channel provides the HEMT with a high electron mobility and high carrier density, leading to a lower noise figure and higher cut-off frequency [1].

Amongst the material systems in the III-V compound semiconductors, InGaAs/InAlAs has the most desirable band structure and transport properties (carrier mobility, saturation velocity, etc). This material system offers pHEMT devices with high electron sheet charge density and excellent carrier confinement in the channel. This results in superior electron transport, translating into higher transconductance ($g_m$) and current gain cut-off frequency ($f_T$), and a lower noise figure (NF). Hence, the InGaAs/InAlAs system has become a popular material system for high-speed, high-frequency devices, and its use has even extended down to the 0.9 GHz and 1.9 GHz bands used for mobile communication [2]. Current development of InP-based InAlAs/nGaAs HEMTs has demonstrated excellent high-frequency and high-gain performance [3, 4]. The devices have a cut-off frequency above 625 GHz [5], and they dominate microwave and millimetre-wave applications, and low noise amplifiers (LNAs) fields [6, 7, 8].
The superior performance of InP-based InAlAs/InGaAs pHEMTs, compared to that of GaAs-based HEMTs [9] makes them the most preferred candidates for the active device selection. They also play a key role in the fabrication of Monolithic Millimetre Wave Integrated Circuit (MMIC) LNAs. The design of MMIC LNAs itself has emerged from the design of very low frequency, low noise figure, very high power devices. For over a decade, the advancement in millimetre-wave semiconductor technologies has been strongly driven by military requirements, such as for sensor and radar applications [10]. There are also an increasing number of wireless civil applications, such as telecommunications, sensors and navigation systems, which demand increasingly low-noise and low-power devices at high frequencies. Undoubtedly, these systems could be realised with the outstanding combination of high-frequency operation and low-noise performance offered by InGaAs/InAlAs/InP pHEMT devices.

1.2 Project Motivation and Objective

Recent advances in Metal Organic Chemical Vapour Deposition (MOCVD) and Molecular Beam Epitaxy (MBE) epitaxial growth techniques for III-V compound semiconductor systems have made it possible to grow extremely high-quality III-V heterojunction structures. Current development of InAlAs/InGaAs HEMTs has demonstrated high cut-off frequencies of between 625 GHz and THz, and excellent high-gain performance [3, 4]. They dominates millimetre-wave applications, such as low-cost LNAs [3] and Ka-band MMIC LNAs [6]. The previous work conducted by the Manchester group on novel pHEMT devices [11,12] - and hence the MMIC LNA development for the SKA - was initiated at the SKA-low frequency (L-band) [13, 14] using a one micron gate length device.

With the device size scaled down to the nanometre regime, and various epitaxial layer structures being designed and optimized, physical modelling becomes essential to fully characterize and identify the underlying physical behaviour of these devices. Semiconductor modelling, based on physical models [15, 16], can prove to be very helpful in the development of such transistors. The empirical modelling [17,18] is also required to accurately model and estimate the linear and non-linear behaviour of
the designed circuits - i.e. LNA over a range of frequencies; is also required to characterise the device’s technological process.

The development and verification of device simulation tools has become desirable to allow comparison between statistically-analysed and measured data. With the aid of modelling, the time and cost of device fabrication and characterization can undoubtedly be considerably reduced [19]. This research aims to employ the advances in the SILVACO simulation package and Advanced Design System (ADS) to appreciate the effect of the underlying device physics on the device output characteristics. The aim is to reproduce both the DC and RF device characteristics, and to investigate the correlation between the device physics and the output characteristics. The initial device modelling work of the 1 μm gate device is extended to the deep-submicrometer gate regime, with the aim of developing models for new transistors. The models will contribute to the design and fabrication of advanced integrated circuits using the extensive facilities available at the University of Manchester.

Despite the high cut-off frequency achievements reported for InP pHEMT in the terahertz region, i.e. [20] and [21], novel devices are needed which are able to support future ultra-high speed, high frequency applications. This is especially true for sub-THz or THz frequencies (operating at room temperature). With its ability to provide a very high fundamental frequency well into the THz region, the Resonant Tunnelling Diode (RTD) may offer a solution to this problem. Therefore, the study of physical modelling is extended to quantum modelling for an advanced InGaAs/AlAs RTD device. The purpose of this extended work is to effectively model the RTD using Silvaco’s ATLAS software, particularly with respect to the peak current density, peak-to-valley-current ratio (PVCR), and negative differential resistance (NDR) voltage range.
1.3 Scope of thesis

This thesis presents the physical and empirical modelling of advanced InGaAs/InAlAs pHEMTs for the development of low noise amplifier (LNA) designs. This is intended to fulfil the requirements of devices for the 8.0 to 12 GHz band of the Square Kilometre Array (SKA) [22]. During the preliminary work, the transistor used in this project employed a 1μm gate length, with multiple gate widths. The modelling and circuit designs are then progressed with the submicrometer gate InGaAs/InAlAs pHEMT to facilitate higher frequency applications. The transistors were fabricated at the University of Manchester, and the measurement of the transistors was carried out at room temperature. The proposed design is a Monolithic Microwave Integrated Circuit (MMIC), which combines high performance with low cost. It avoids expensive and labour-intensive external components (especially discrete inductors used for the input stage of the LNA). In this work, the advances in the InGaAs/InAlAs material system are fully utilised in the submicron gate length pHEMT. In addition, the study is extended to a simpler one-dimensional representation of a two terminal device - the InGaAs/AlAs resonant tunnelling diode (RTD).

1.4 Thesis Outline

The organization of the remainder of this thesis is as follows:

**Chapter 2** provides insights into the fundamental theory of semiconductor device physics for heterojunctions, and the background of the HEMT structure. This chapter deals with the literature review of the basic concepts of III-V compound semiconductors. The development of different III-V FET devices are presented, in relation to advancements in material engineering and their contribution to RF applications. A comparison is presented between the different FET structures (MESFET, HEMT and pHEMT), and between InGaAs-AlGaAs, InGaAs-InAlAs materials. The advantage of the InP-based pHEMT for low-noise and high-speed applications is outlined. The discussion continues with an extensive study of the physics and operation of the devices. At the end of the chapter, some important physical parameter extraction methods are highlighted, as these methods are used throughout this work.
Chapter 3 highlights the significance of device simulations, and introduces the simulation tools used in the development of the physical modelling performed in this work. Detailed procedures for the device modelling of pHEMT structures are presented, i.e. meshing, structure and parameter definitions, and physical models, and numerical methods. A detailed explanation of the concepts of device modelling, and the current-transport equations used in this project are also presented.

Chapter 4 briefly explains the fundamental models that are used in the simulation work for the small signal model. In this chapter a physically-based model for various samples of the in-house fabricated pHEMTs is developed, providing an insight to the internal device behaviour. The DC and RF characteristics of the two-dimensional physical device simulations are compared with the experimental results, which were fitted and analysed. The modelled device simulation shows excellent agreement with the experimental results.

Chapter 5 explains the empirical model parameters and device modelling steps for the pHEMT device. The empirical models for three different epitaxial layers with various device sizes and gate lengths are presented. The agreements between the modelled and measured parameters are discussed and analysed. An optimized pHEMT model which is used in the LNA design is presented at the end of the chapter, in addition to a brief study of the device’s noise characteristics. The results from device empirical modelling provide a guide for active device selection for LNA circuit designs.

Chapter 6 begins with background information on the Monolithic Microwave Integrated Circuit (MMIC) and its advantages in the integrated circuit roadmap. This is followed by an outline of the LNA theoretical concept, which is used to examine the requirements of a complete system design. The target specifications of the MMIC LNA design are then addressed; this includes discussion of the performance constraints and compromises that arise in the design of circuit topologies, biasing networks and matching configurations. The design and analysis of the single-input single-ended output, single and double-stage LNAs are presented using all of the criteria discussed in Chapters 6. The LNAs are designed to match a 50 Ω input and output impedance. At the end of this chapter, the target specifications attained from the simulation of the
single- and double-stage MMIC LNA for the C-band and X-band frequency range are presented and discussed. The layout designs of these LNA circuits are also developed and presented.

Chapter 7 demonstrates one-dimensional physical modelling for various samples of large-size and submicrometer In$_{0.8}$Ga$_{0.2}$As/GaAs RTD devices. The concept, operation principle and the applications of RTD in Terahertz (THz) region are explained at the beginning of the chapter. The modelling of the two-terminal RTD device focuses on the DC analysis; this is mainly to reproduce the I-V characteristics of experimental devices, namely the negative differential resistance (NDR), NDR peak voltage, $V_p$ (voltage at peak current) and the peak current density($I_p$). The model optimisation based of the device structure, i.e. spacer layer, barrier layer and quantum well layer thicknesses are also studied. The modelled device simulation for DC analysis shows excellent agreement with the experimental results.

Finally, Chapter 8 summarises the work that has been discussed in the earlier chapters, and suggests some potential future research to further extend the work described in this thesis.
2 CHAPTER 2

THEORY AND BACKGROUND OF PSEUDOMORPHIC HIGH ELECTRON MOBILITY TRANSISTOR

2.1 Introduction

For several decades, the electronic circuits development has been driven by an increase in the density of silicon complementary metal–oxide–semiconductor (CMOS) transistors, and the progression in their logic performance. The ICs produced are becoming more powerful, smaller, more economical and energy efficient. However, as the scaling of the silicon transistor is now reaching its limits, III-V compound semiconductors are now becoming a key choice to continue the microelectronic revolution for high-speed and high-frequency devices. The outstanding electron transport properties and frequency response of these materials might be central to the development of nanometre-scale logic transistors [23]. For example, the electron mobility in the InGaAs and InAs HEMT is more than 10 times higher than in silicon, at a comparable sheet density. In their early stages of development, the HEMT was originally intended for high speed applications, and these devices were discovered to exhibit a very low noise figure. This is related to the nature of the two-dimensional electron gas (2DEG), and the fact that there are less electron collisions in the channel [6]. These devices are also known as Modulation Doped Field Effect Transistors (MODFETs), Two-dimensional Electron Gas Field Effect Transistors (TEGFETs), Heterojunction Field Effect Transistors (HFETs) or Selectively Doped Heterostructure Transistors (SDHTs).

The basic principles which govern the development of HEMTs are explained in this chapter. An introduction to heterojunctions, their band structures, formation of quantum wells, carrier confinement, and 2DEG is discussed. The HEMT and pHEMT structures and their operational principles are summarized. Some of the applications of pHEMTs, and work concerning pHEMT design in the literature are also highlighted in later sections.
2.2 Hetero Junction Structure

Generally, HEMT structures are based on epitaxially grown layers with different compositions and energy band gaps. When these different semiconductor layers are brought together, they form heterojunctions. The principle parameters for heterostructures are the difference of energy bandgaps \( (E_g) \) and the lattice constant \( (a) \) for the two semiconductor materials. Figure 2.1 illustrates the lattice constant and energy gap parameters for various III-V material system that are of interest to the work presented here. These parameters play a very important role in the advanced bandgap engineering to optimize device characteristics.

![Figure 2.1 The energy gap of III–V compounds and ternary derivatives as a function of lattice constant [24]](image)

The ternary compound semiconductor materials that are lattice matched to GaAs and InP substrates are shown. For example, the AlAs, Al\(_x\)Ga\(_{1-x}\)As, (for all values of x) and In\(_{0.48}\)Ga\(_{0.52}\)P is lattice match with GaAs. Consequently, the In\(_x\)Ga\(_{1-x}\)As and In\(_x\)Al\(_{1-x}\)As are lattice matched to InP only at a single fixed mole fraction \( (x \sim 0.52) \).

Practically, the materials chosen must have a very close lattice constant to minimise the disturbance at the heterointerface. However, for various materials that have slightly different lattice constant, Vegard’s law is used to synthesize new
semiconductor materials to match the size of the crystal lattices. Therefore, the resulting lattice constant and the energy band gap can be approximated using Vegard’s law [21, 22] as in Equation 2.1, where \( x \) is the mole fraction and \( AZ \) and \( BZ \) are the binary compound lattice constant and band gap values,

\[ a_{\text{alloy}} = xAZ + (1-x)BZ \]  
Equation 2.1

The lattice constant and band-gap energy for various GaAs and InP-based materials are given in Table 2.1 [26,27]. Enhancements in epitaxial growth techniques have enabled the possibility of growing lattice mismatched heterostructures [27]. In this situation, the lattice atoms change abruptly between the two semiconductor materials with dissimilar energy band gaps and lattice constants [24, 25]. This growth technique is known as *pseudomorphism* and will be discussed in the next section.

Table 2.1 Lattice constant and energy band gap of common III-V binary and ternary compound semiconductors at 300 K [26, 27]

<table>
<thead>
<tr>
<th>Alloy</th>
<th>Lattice constant, ( a_0 (\text{Å}) )</th>
<th>Band gap, ( E_g ) (eV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>GaAs</td>
<td>5.653</td>
<td>1.42</td>
</tr>
<tr>
<td>AlAs</td>
<td>5.660</td>
<td>2.16</td>
</tr>
<tr>
<td>InAs</td>
<td>6.058</td>
<td>0.37</td>
</tr>
<tr>
<td>InP</td>
<td>5.869</td>
<td>1.35</td>
</tr>
<tr>
<td>( \text{In}<em>{0.53}\text{Ga}</em>{0.47}\text{As} )</td>
<td>5.869</td>
<td>0.76</td>
</tr>
<tr>
<td>( \text{In}<em>{0.52}\text{Al}</em>{0.48}\text{As} )</td>
<td>5.869</td>
<td>1.48</td>
</tr>
</tbody>
</table>

For an InP substrate, the lattice matched \( \text{In}_{0.52}\text{Al}_{0.48}\text{As} \) is usually used as a buffer as it has a large band gap, resulting in improved insulation; and \( \text{In}_{0.53}\text{Ga}_{0.47}\text{As} \) as a channel (due to its high mobility) followed by \( \text{In}_{0.52}\text{Al}_{0.48}\text{As} \) as a barrier (large \( \Delta E_c \)). Over the years, the state-of-art compound semiconductor technology has moved from GaAs channel (lattice constant =5.64Å) to \( \text{In}_x\text{Ga}_{1-x}\text{As}/\text{InP} \) channels (5.87Å) which motivated by the higher saturation velocity in these materials [20].
2.2.1 Lattice Matched and Pseudomorphic Material System

Ideally, heterostructures are formed by semiconductors with the same crystal structures and the same lattice constant. A HEMT structures grown with the same lattice constant are referred to as lattice matched HEMTs, i.e. $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ and $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ (lattice matched to InP). Structures with slightly different lattice constant are known as Pseudomorphic HEMTs (pHEMTs). In modern epitaxial growth techniques, the thickness of lattice mismatched layers is kept within a certain critical thickness limit and the deposited layer must be very thin to avoid defect or dislocation formation \[23, 29\]. This new layer is called “pseudomorphic” as it alters its original crystal structure and physical properties, i.e., $\text{InGaAs-InAlAs}$, $\text{AlGaAs-InGaAs}$. For lattice mismatched, the atoms at the hetero-interface have to slightly adjust their positions in order for them to conserve the geometry of the lattice. The adjustments of the atomic position will result in a small strain at the interface. The critical thickness of grown epilayer ($h_C$) and the strain ($\varepsilon$) is given by Equation 2.22 and Equation 2.3. Respectively, $a_S$ and $a_L$ denotes the lattice constant for substrate and grown epilayer.

\[
h_C = \frac{a_S}{2\varepsilon} \quad \text{Equation 2.2}
\]

\[
\varepsilon = \frac{a_L - a_S}{a_S} \quad \text{Equation 2.3}
\]

The Figure 2.2 illustrates the crystal formation of the binary and ternary compound semiconductor material. In Figure 2.2 (a), $a_L$ is in lattice matched with $a_S$, and hence the over-layer and base material atoms at the crystal interface are not required to adjust their positions relative to each other. However, lattice mismatched in the semiconductor may result in defects due to dislocations, as shown in Figure 2.2 (b). Above the critical thickness, the excessive strain energy is released by the formation of dislocations where some of the bonds are missing or extra bonds appear. These dislocations adversely affect the electrical characteristics of a device by creating localized states which act as traps for the charge carriers \[29\]. Materials that are not in lattice matched or have different inter-atomic lattice spacing are known as pseudomorphic i.e., $\text{AlGaAs}$ and $\text{InGaAs}$. The formation of pseudomorphic crystal
structure under compressive and tensile strains are shown in Figure 2.2 (c) and Figure 2.2 (d) respectively. When $a_L$ is larger than $a_S$, the resultant relaxed material is under compressive strain whereas the atoms are under tensile strain when $a_L$ is smaller than $a_S$. 

![Diagram showing lattice match and imperfect dislocation](image)
Figure 2.2 Conceptual formation of (a) lattice matched, (b) lattice mismatched with defects, and pseudomorphic layers (c) Compressive and (d) Tensile strain
2.2.2 Band Discontinuity

Energy band discontinuity is the most important aspect of heterojunctions. It is an interesting feature in HEMTs, which can be used to modify the transport of charge carriers. The junction of two semiconductors with a difference in energy bandgaps results in an abrupt change in the energy band diagram of the heterostructure. Figure 2.3 shows the energy band diagram of two isolated semiconductors with the notation given by: $E_C$ and $E_V$ indicating conduction and valence bands, $E_{g1}$ and $E_{g2}$ the energy band gap for material A and material B, $\chi$ is the electron affinities, $E_F$ is the Fermi level, $\Delta E_C$ the electron affinity, and $\Delta E_C$ and $\Delta E_V$ representing the conduction and valence band discontinuities between the two materials [33].

![Energy Band Diagrams](image)

Figure 2.3 Energy Band Diagrams for wide and narrow bandgap semiconductor
(a) before and (b) after contact

The energy-band model of an ideal, abrupt heterojunction, was first established by Anderson [34]. The model assumes that $\Delta E_C$ was equal to the difference in electron affinities, $\chi$ as shown in Equation 2.4 and Equation 2.5.

$$\Delta E_C = \chi_1 - \chi_2$$  \hspace{1cm} Equation 2.4

$$\Delta E_V = (E_{g2} - E_{g1}) - (\chi_1 - \chi_2)$$  \hspace{1cm} Equation 2.5

Similarly, this could be written using Equation 2.6 and Equation 2.7,
\[ \Delta E_g = E_{g1} - E_{g2} \]  

Equation 2.6

\[ \Delta E_g = \Delta E_c + \Delta E_v \]  

Equation 2.7

In most semiconductors, the band gap engineering is very effective to attain numerous amounts of junction discontinuities. A larger band discontinuity, \( \Delta E_C \) will lead to better carrier confinement and therefore a higher carrier concentration at the 2-DEG interface. The InAlAs/InGaAs/InP material system has many significant advantages over the AlGaAs/GaAs [24] or AlGaAs/InGaAs/GaAs material systems. The \( \Delta E_C \) between \( \text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As} \) layer in InAlAs/InGaAs/InP material system (> 0.5 eV) is higher than the \( \Delta E_C \) between \( \text{Al}_{0.2}\text{Ga}_{0.8}\text{As}/\text{In}_{0.15}\text{Ga}_{0.85}\text{As} \) layer (~ 0.3 eV) in the pseudomorphic AlGaAs/InGaAs/GaAs material system. The band discontinuity is even lower for \( \text{Al}_{0.30}\text{Ga}_{0.70}\text{As}/\text{GaAs} \) heterojunction where the \( \Delta E_C \) is only 0.24 eV [16]. Therefore, this property makes \( \text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InP} \) a prominent and suitable candidate for high-speed devices application with greater flexibility over carrier control at the junction.

2.2.3 Quantum Well and 2-DEG

When a thin layer of (~ 100 Å) of low band gap semiconductor material (e.g. GaAs) is sandwiched between two similar high band gap semiconductors (e.g. AlGaAs), a Quantum Well (QW) is formed in the heterostructure. Such a heterojunction boundary will experience discontinuities at the edges of the conduction band and valence band with a QW generated for the carriers (electrons and holes) as illustrated in Figure 2.4. The dopants in the high band gap layers can supply the carriers to the quantum well. When the bottom of the quantum well is below the Fermi level, the high energy donors will go down to the well, hence creating a Two Dimensional Electron Gas (2DEG). This is shown in Figure 2.4 (c). The electron is free to move parallel to the interface, and so is quasi two-dimensional. However, the electrons in the quantum well are unable to move in the direction perpendicular to the interface, i.e. the crystal growth direction [35]. Careful choice of the materials and alloy compositions allow control of the carrier densities within the 2DEG.
2.3 Metal Semiconductor Contacts

Metal-semiconductor contacts are present in every semiconductor device. There are two types of contact for a metal-semiconductor junction: Schottky contact or ohmic contact depending on the nature of the interface. The details of these contacts are discussed in section 2.3.1 and section 2.3.2.

2.3.1 Ohmic Contact

An ohmic contact is formed if no potential barrier exists between the metal and semiconductor. It is a non-rectifying contact and does not control the flow of current, thus the current flows equally in both directions (reverse and forward) with linear I-V characteristic. On top of that, an ohmic contact should have an insignificant
contact resistance, $R_C$ relative to the series resistance, $r_s$ of the semiconductor so that zero or very small current loss occurs across the device. There are 2 types of ohmic contact: (1) for n-type semiconductor; the metal workfunction, $\Phi_m$ must be closer to or smaller than the semiconductor electron affinity $\chi$. Therefore, $\Phi_m$ must be smaller than the work-function of semiconductor $\Phi_s$, i.e. $\Phi_s > \Phi_m$, as shown in Figure 2.5 (2) for a p-type semiconductor, $\Phi_m$ must be close to or larger than the sum of electron affinity and energy bandgap of the semiconductor, which is usually impractical. Hence p-type ohmic contacts are a lot more difficult to fabricate than n-type ones.

![Figure 2.5 Band diagram of a metal-semiconductor interface: (a) before contact and (b) after contact [33]](image)

Practically, there are two ways in achieving a good ohmic contact in semiconductor processing: either by high semiconductor doping layer or through a low Schottky barrier height at metal-semiconductor junction. At any metal-semiconductor contact, there always exists a Schottky barrier [33]. The carriers must overcome this barrier in order to travel between the metal and semiconductor sides. When the semiconductor is heavily doped, i.e. $N_D \geq 10^{19}$ cm$^{-3}$, the depletion width and consequently the barrier width near the metal-semiconductor contact will be reduced. Electrons now can overcome this barrier and tunnel through it as the depletion width becomes sufficiently narrow. This mechanism is known as Thermionic Field.
Emission (TFE) [36]. Alternatively, the barrier height is reduced by means of a low energy gap material at the semiconductor side. Here, the electrons have energies larger than the potential barrier and Thermionic Emission (TE) takes place by electrons moving over the barrier [33]. Figure 2.6 illustrates the TFE and TE mechanism at the Schottky barrier interface.

Figure 2.6  Current conduction at Ohmic contact (a) via TFE in highly doped semiconductor and (b) via TE at low Schottky barrier interface [33]

### 2.3.2 Schottky Contact

A Schottky contact (also known as rectifying contact), permits the flow of current in one direction and provides a barrier to the flow of current in the opposite direction. In Schottky contact, the semiconductor work-function, $\Phi_m$ is smaller than the work-function of the metal, $\Phi_m$ ($\Phi_s < \Phi_m$). Figure 2.7 (a) illustrates a metal to semiconductor interface before and after forming the Schottky contact for n-type semiconductor and metal contact. On contact, electrons from the semiconductor conduction band flow into lower energy states of metal, till a constant Fermi level is achieved at equilibrium condition. The flow of electrons will then leave a positive charge of ionised donor in the semiconductor which creates the depletion region of thickness, $X_{dep}$ as illustrated in Figure 2.7 (b). The band bending at equilibrium, results in a potential barrier, $\Phi_b$, at the interface and a built-in potential, $V_{bi}$ that restricts further diffusion of electrons from semiconductor to metal. The exact shape of the conduction and valence bands is determined by solving the Schrödinger and Poisson equations self-consistently.
The built-in potential is given by Equation 2.8:

$$V_{bi} = \Phi_b - \Phi_n$$  \hspace{1cm} Equation 2.8

where $\Phi_n$ is the potential difference between the minimum of conduction band ($E_C$) and Fermi level $E_F$, i.e.

$$\Phi_n = \frac{E_C - E_F}{q}$$  \hspace{1cm} Equation 2.9

The potential barrier, $\Phi_b$, formed at the interface is related to the metal work-function, $\Phi_m$ and semiconductor electron affinity, $\chi_s$ as in Equation 2.10 and Equation 2.11:

$$\Phi_B = \Phi_m - \chi_s$$  \hspace{1cm} Equation 2.10

$$\chi_s = \phi_S - \phi_n$$  \hspace{1cm} Equation 2.11

Under zero bias condition, the net current flow between semiconductor to metal is zero because the same amount of current flows from semiconductor to metal and vice versa. However, under forward and reverse bias conditions, the flow of current
transport changes due the changes in the $V_{bi}$. These conditions are illustrated in Figure 2.8 in which $\phi_B$ remains constant [12] in both figures.

![Figure 2.8 Current transport by thermionic emission in: (a) forward bias and (b) reverse bias [33]](image)

When a positive bias, e.g., $V_{Forward}$ is applied to a metal, it will experience forward bias condition. Under this condition, the Fermi level, $E_{Forward}$ will be shifted up and the built-in voltage, $V_{bi}$ will be reduced by a voltage $V_{Forward}$ as illustrated in Figure 2.8 (a). The Figure 2.8 (b) shows that if a negative bias, i.e., $-V_{Reverse}$ is applied to the metal, a reverse bias condition is achieved. In reversed bias condition, the Fermi level will be shifted down and the built-in-potential will increase by a voltage $V_{Reverse}$. In a pHEMT, the quantity of electrons flow from metal to semiconductor under reverse bias condition is also known as leakage current [31]. The leakage current is one of the unwanted drawback for a pHEMT device which degrades its performance, particularly at high frequency applications.
The mechanism of TE, TFE and FE at the barrier is shown in Figure 2.9. Theoretically, a metal with a higher Φ_m will yield a larger Schottky barrier on the same semiconductor. But this is not quite valid in practice. There is always an intermediate layer, contributing to the surface contamination of the metal or the surface states of the semiconductors such as native oxides or dangling bonds after etching, formed in between the metal and semiconductor. As a result, the Fermi level of a semiconductor will pin at the surface [38] of the intermediate layer before equilibrium is achieved. The resulting barrier height is not sensitive to the change of metal work function and such phenomenon is called Fermi-level pinning [33].
2.4 Introduction to High Electron Mobility Transistors (HEMTs)

HEMTs are very similar to Metal Semiconductor Field Effect Transistors (MESFET) in terms of structure and operations, but the key difference is the heterojunction structures. By bringing two dissimilar semiconductors to the junction, a potential well is formed in the channel due to the bending of energy level. This results in high density of carrier confinement in the well (channel), which only allows electron to move in a two-dimensional plane which creates the 2DEG layer. It is the high two-dimensional electron gas density with a high mobility and low scattering mechanism which contributes to naming the device the High Electron Mobility Transistor. This ultimately results in improved gain, noise and power performance of the device.

2.4.1 HEMT Epitaxial Layer

HEMT is a field effect transistor (FET) and utilises a vertical structure. A typical HEMT structure consists of epitaxial layers, namely cap layer, barrier layer, channel layer, and buffer layer which are grown on semi insulating substrates. These epilayer have different material parameters such as energy band gaps, doping concentration, layer thickness, etc. Figure 2.10 illustrates a conventional HEMT structure with a single delta doping layer.

Figure 2.10 Cross section of conventional HEMT with δ-doped layer
2.4.1.1 Cap layer

The source and drain contacts are formed through the Cap layer. The Cap layer is heavily doped (usually $>10^{18}$ cm$^{-3}$) to facilitate the formation of a low resistance for the source and drain metal contacts. The thickness of the cap layer is about 50Å to 100 Å [24]. Higher doping levels and a thicker capping layer would simultaneously reduce the device contact resistance [39] and effectively shorten the source-to-drain spacing; resulting in very high electron velocity, $g_m$, and $f_T$ in the device. However, this also significantly reduces the device breakdown voltage, $V_{BR}$, and also increases the device output conductance, $g_{ds}$, and drain-to-gate feedback capacitance, $C_{dg}$.

Another technique followed is the alloying and annealing technique in which electrons heavily diffuse down to the 2DEG thus reducing the potential barrier caused due to difference in electron concentration on both sides of the junction [35].

2.4.1.2 Supply Layer

The supply layer is formed beneath the cap Layer using a wide band gap material. Typically, the supply layer is uniformly doped with Si to supply carriers that diffuse into the channel and become available for conduction. The distance between gate and channel is very critical and is largely determined by the thickness of the supply layer [35]. A thinner supply layer allows for a small distance between the gate metal and the carrier channel that results in higher charge density in the channel, cutoff frequency, $f_T$ and transconductance, $g_m$ but reduces breakdown voltage. The thickness of supply layer and increasing doping concentration of the supply layer reduces the depletion width. If the depletion region is not fully formed, i.e. the supply layer is not fully depleted, poor field effect actions are expected to arise in this regime [40]. In order to eliminate parallel conduction in the supply layer, this layer must be completely depleted by both heterojunction and the Schottky gate.
2.4.1.3 Delta (δ) Doping Layer

A uniformly doped supply layer can be replaced by an undoped supply layer, followed by a very thin but extensively doped layer called a δ-doped layer (or pulse-doped). Hence, when the parallel conduction problem in the barrier layer is reduced, high sheet charge density and breakdown voltage can be achieved.

![Figure 2.11 Conduction band of general depletion mode HEMT structure with δ-doping and bulk-doping [33]](image)

As a result, the channel concentration increases. The difference of these doping to the structure is illustrated in Figure 2.11. The energy quantization occurs at the discontinuity formed between the high and low band gap materials. Electrons in the supply layer (bulk doping case) or δ-doping can then tunnel through the thin potential barrier and be trapped into the triangular QW. The electrons in the QW forms a high electron mobility plane called a 2DEG. The Coulomb scattering between electrons and the fixed ionized atoms separated by the spacer layer leads to high mobility. Figure 2.12 shows the relation of δ-doping concentration and the drain current as described in [41]. A degradation of the drain current is observed with reducing the δ-doping concentration.
2.4.1.4 Spacer Layer

A spacer layer of undoped materials i.e., AlGaAs or InAlAs is placed between the InAlAs donor and the InGaAs channel layer to separate the negatively charged 2DEG from the ionized dopant atoms. A thin spacer layer is preferred for low-noise and power devices due to the reduced parasitic source resistance and the increase in transconductance, $g_m$, and current density. However, a thicker spacer layer might be applied to provide higher electron mobility with a smaller charge density in the channel. At cryogenic temperatures the noise performance of a HEMT is strongly dependent on the spacer thickness due to the large increase in electron mobility and velocity [6].

2.4.1.5 Channel Layer

The channel layer is a narrow bandgap undoped material, i.e. GaAs or InGaAs. These material systems improve transport properties due to the higher mobility of InGaAs and stronger electron confinement associated with the quantum well at the heterojunction. The barrier on both sides of the channel form heterojunctions on either edge of the channel layer thus building QW which confines high carrier concentration. These electrons have superior mobility characteristic because of high mobility and undoped nature of the channel material. Increasing the Indium concentration in the carrier channel of the pHEMT will result in further improvements in electron carrier confinement and transport properties [24].
For example, the performance of InP based pHEMT is directly related to the intrinsic properties of the InGaAs/InAlAs material system. The high indium content (typically 53 – 80%) InGaAs channel contributes to the high electron mobility and velocity [42]. Moreover, the large band discontinuities at the InGaAs/InAlAs heterojunctions will permit high two-dimensional electron gas (2DEG) densities. Figure 2.13 shows the electron velocity as a function of electric field for various In concentrations of InGaAs. Unfortunately, increasing the Indium concentration in In$_x$Ga$_{1-x}$As also increases the lattice constant [24].

### 2.4.1.6 Buffer Layer

Basically, the buffer layer is developed to confine the carriers to the device channel. It is also significant to isolate any unwanted defects on the substrate surface and also to de-couple it from the 2DEG [43]. The buffer layer is grown using undoped wide bandgap material that creates an energy barrier in the conduction band, thus reducing electron injection into the buffer or substrate. The electrons being injected into the substrate layer because of the application of Drain-to-Source electric field, contribute to the drain current, thus increasing the output conductance of the device and degrading the device pinch-off characteristic. The thick buffer layer is used to reduce any growth defects, and to accumulate any impurities from the substrate interface that may degrade the performance of the 2DEG channel [35].
2.5 Principles of Operation

In a HEMT device, the channel is either built-in (depletion-mode or normally ON) or induced (enhancement-mode or normally OFF). When a bias voltage is applied to the gate metal, the depletion region will extend to the 2DEG due to the induced electric field. Hence, by adjusting the gate bias voltage, $V_{GS}$, the number of electrons in the channel can be modulated and in turn controls the conductivity of the HEMT device. The primary operating parameters dealing with high power HEMT operations are the transconductance ($g_m$), the 2DEG sheet charge concentration ($n_s$), the drain current ($I_D$), the threshold voltage ($V_{TH}$), and the contact barrier height ($\phi_B$).

The charge flowing in a HEMT device is normally confined to the 2DEG and changed by the gate voltage. When a gate voltage is applied to the device, the sheet charge concentration, $n_s$ is changed proportionally to gate voltage and is given by equation 2.12:

$$n_s(x) = \frac{C_i[V_{GS} - V_{TH} - V_{DS}(x) - q]}{q}$$  \text{Equation 2.12}

where $x$ is the direction of the drain-source electric field, $V_{ds}(x)$ is the applied drain-source electric field, $d_1$, $d_2$, and $d_3$ is the supply layer thickness, spacer thickness, and channel thickness respectively. $C_i$ is the gate channel capacitance and is given by

$$C_i = \frac{\varepsilon_0 \varepsilon_s}{d_1 + d_2 + d_3}$$  \text{Equation 2.13}

The threshold voltage is an important parameter because it is a measure of when the HEMT device will begin conducting. $V_{TH}$ can be expressed as:

$$V_{TH} = \Phi_b - \frac{\Delta E_C - E_F}{q} - V_p$$  \text{Equation 2.14}

Pinch-off voltage, $V_p$ is the condition when no current flows through the device. The 2DEG is completely depleted by the depletion region under the gate electric field. Equation 2.15 and Equation 2.16 show the values of $V_p$ for bulk doping and $\delta$-doping respectively.

50
\[ V_{p,\text{bulk doping}} = \frac{qN_p d^2}{2\varepsilon_0 \varepsilon_s} \quad \text{Equation 2.15} \]

\[ V_{p,\Delta\text{-doping}} = \frac{qn_s^2 d^*}{2\varepsilon_0 \varepsilon_s} \quad \text{Equation 2.16} \]

The most important characteristic in the HEMT operation is the channel current behaviour; linear and saturation region. The current behaviour in this channel relates to the gate length, \( L_G \), and the carrier mobility in 2DEG, \( \mu_n \), and is given by

\[ I_{DS} = \frac{W}{L_G} \mu_n C_i [(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}] \quad \text{Equation 2.17} \]

Considering the condition when \( V_{DS} \ll (V_{GS}-V_{TH}) \), the channel current will be in the linear region and Equation 2.17 can be rewritten as

\[ I_{DS} = \frac{W}{L_G} \mu_n C_i (V_{GS} - V_{TH})V_{DS} \quad \text{Equation 2.18} \]

Here, \( I_{DS} \) is shown to be linear with \( V_{DS} \) and the corresponding channel resistance is given by:

\[ R = \frac{L_G}{W \mu_n C_i} \frac{1}{V_{GS} - V_{TH}} = \frac{\Delta V_{DS}}{\Delta I_{DS}} \quad \text{Equation 2.19} \]

The relationship between \( I_{DS} \) and \( V_{DS} \) is shown in Figure 2.14. From the I-V characteristics, when \( V_{DS} \) increases, the electric field at the drain side will rise up rapidly and starts depleting when \( V_{DS} = V_{GS} - V_{TH} \) (pinch-off point). The depletion region will extend from the drain to source and any further increase in \( V_{DS} \) will only lead to a small increase in \( I_{DS} \) due to carrier velocity saturation (\( V_{\text{SAT}} \)). This is where the saturation region is located, and the corresponding equation is given by Equation 2.20,

\[ I_{DS} = \frac{W}{L_G} \mu_n C_i (V_{gs} - V_{th})^2 \quad \text{Equation 2.20} \]
Transconductance, $g_m$, is a measure of how much current gain a device can provide in response to a change in voltage input, $V_{GS}$ for a given $V_{DS}$. Based on Figure 2.14, $g_m$ can be represented by

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}}$$

Equation 2.21

$$g_{m, linear\ region} = \frac{W_G \mu_n C_{GS} V_{DS}}{L_G}$$

Equation 2.22

$$g_{m, saturation\ region} = \frac{W_G \mu_n C_{GS} (V_{GS} - V_{TH})}{L_G}$$

Equation 2.23

The transconductance for a typical pHEMT device operating in the saturation region is normally a bell shape profile. Initially, $g_m$ follows the similar trend as $I_{DS}$ with stronger $V_{GS}$ but it declines very rapidly after the peak value ($G_{m,\ max}$). However, when the Fermi level of semiconductor, $E_F$, touch the bottom of $\delta$-doping layer, this resulted in a low mobility parasitic channel. Hence, the interaction between the gate and the 2DEG causing a significant degradation in the overall mobility and the effective $g_m$ [98].
The relation of $g_m$ and drain current is shown in the Figure 2.15. The other two figures of merit of HEMT device are: (1) cut-off frequency or unity gain frequency, $f_T$, and (2) maximum frequency of oscillation, $f_{\text{max}}$, is defined using $g_m$ value and will be discussed in the following section.

The RF performance of pHEMT devices is accessed by two important figures of merit (FOM), the cut-off frequency ($f_T$) and the maximum frequency of oscillation ($f_{\text{max}}$). Their relationship is illustrated in Figure 2.16. Both short-circuit current gain ($h_{21}$) and unilateral power gain ($U$) are frequency dependent, but one rolls off at 20 dB/decade, while the other exhibits two different profiles (10 and 20 dB per decade). Figure 2.16 shows the frequency responses of a D-mode pHEMT under a fixed $V_{DS}$ and $V_{GS}$. 

---

**Figure 2.15** Transconductance extracted at different $V_{ds}$ [44]

**Figure 2.16** Frequency responses of a D-mode pHEMT under a fixed $V_{DS}$ and $V_{GS}$
The cutoff frequency, $f_T$ or also known as the unity current gain frequency, is the measure of how fast an electron can travel within a distance, $L_G$. In other words, it is the maximum frequency at which the device can operate with a current gain factor of “1”, in which case the input gate current ($I_{GS}$) is equal to the output drain current ($I_{DS}$) in the small-signal equivalent circuit. The expression of the gain current is given by Equation 2.24. The relationship between $f_T$, $g_m$ and other parasitic in HEMT device is described by Equation 2.14:

$$\left|\frac{i_{out}}{i_{in}}\right| = \left|\frac{g_m}{j\omega(C_{gd} + C_{gs})}\right| = 1 \quad \text{Equation 2.24}$$

$$\frac{g_m}{\omega(C_{gd} + C_{gs})} = 1 \quad \text{Equation 2.25}$$

where $\omega = 2\pi f_T$

$$f_T = \frac{g_m}{2\pi(C_{gd} + C_{gs})} \quad \text{Equation 2.26}$$

$C_{gd}$ and $C_{gs}$ are the gate-drain and gate-source capacitances respectively, while $v_{sat}$ is the saturation velocity and $L_G$ is the gate length. The cutoff frequency, $f_T$ can also be interpreted as the transit time ($\tau_C$) for an electron to cross the channel under the gate ($L_G$).

$$\tau_C = \frac{1}{2\pi f_T} \quad \text{Equation 2.27}$$

$$v_{sat} = \frac{L_G}{\tau_C} \quad \text{Equation 2.28}$$

$$f_T = \frac{g_m}{2\pi(C_{gd} + C_{gs})} = \frac{v_{SAT}}{2\pi L_G} \quad \text{Equation 2.29}$$

Therefore, $f_T$ could be improved by considering high $g_m$, minimize the parasitic capacitance, $C_{gd}$ and $C_{gs}$, high $v_{sat}$, and shorter $L_G$. 

54
The $f_{\text{max}}$, also known as the power gain frequency, is defined as the point in the frequency when power gain = 0 dB and given by Equation 2.30. The $f_{\text{max}}$ is dependent on the $f_T$ parameter value. $R_g$, $R_s$, and $R_{ds}$ is the gate resistance, source resistance, and drain-source resistance respectively.

\[
f_{\text{max}} = \frac{f_T}{2\sqrt{\frac{R_g + R_s}{R_{ds} + 2f_TR_gC_{gd}}}}
\]

Equation 2.30

The device maximum operating frequency ($f_{\text{op}}$) is defined by the two figure of merits of pHEMT, $f_T$ and $f_{\text{max}}$. However, these are certainly an applications dependent parameter. Generally, for higher power gain and high power applications, such as Power Amplifiers (PA) $f_{\text{max}}$ is preferred over $f_T$. While for noise sensitive applications such as LNA; a higher priority will be given to $f_T$ for better noise performance.

2.6 Optimisation of pHEMT Designs

Major interest of pHEMT design studied for the past decades varies in terms of the experimental and analysis performed of device parameters such as epitaxial structure [17-19], modelling [16, 20-22], and their applications particularly in the power performance and high speed devices arenas. The reliability of pHEMTs are mainly affected by the epitaxial structure, device fabrication, and device geometry. The important parameters affecting breakdown voltage $B_{Vds}$ and cut-off frequency, $f_T$ of the device are the length, thickness, position and shape of metal-insulator geometry. Specifically, the studies are grouped in terms of the following sections.
2.6.1 Bandgap Engineering

The demand for high speed devices and power performance leads to the advances in the design of band gap engineering and epitaxial layer optimisation. Over the years, researchers have put significant interests in various epilayer structures to satisfy the increasing demand in microwave frequency devices especially for the cutoff frequency \( f_{\text{cut}} \), maximum frequency, \( f_{\text{max}} \) [46], and low leakage current [42,45]. These advance designs include the material system for heterostructure i.e. GaN/AlGaN [49], AlGaAs/GaAs [50], and InGaAs/InAlAs [46,47] or by the number of heterojunctions i.e. DH-pHEMT and SH-pHEMT [53]. The band discontinuity, \( \Delta E_c \) in AlGaAs/InGaAs is higher than \( \Delta E_c \) in AlGaAs/GaAs material system; this is the key for pseudomorphic AlGaAs/InGaAs HEMTs (and pHEMT) on GaAs substrate demonstrating higher 2DEG sheet densities and modulation efficiencies. Consequently, that has made it possible for the HEMTs devices to achieve operating frequencies in the range of 110GHz in 1987 and further increased in the range of 200GHz in 1988 [6]. These astounding results were due to the excellent \( \Delta E_c \) in the InGaAs/InAlAs material system, which is more than twice of \( \Delta E_c \) in AlGaAs/GaAs. The high aluminum content in InAlAs barrier layers are known to improve conduction and valence band discontinuities and Schottky barrier height, whilst the presence of Indium in the channel layer leads to a higher peak electron velocity. However, by changing the barrier layer, the device processing must also be changed due to the diffusion process and re-designing of ohmic contacts.

2.6.2 Changing the Channel

Like other ordinary FET, the performance of HEMT could be improved, i.e., using graded channel or increasing the apparent band gap of the channel by reducing its thickness or changing the Indium content [54]. However, the most severe short channel effect is an increase of the output conductance \( g_0 \), i.e. the breakdown of InP based HEMTs was improved in which a composite channel HEMTs which is based on electron in the channel transfer to subchannel. The Figure 2.17 shows an analaysis of \( I_d-V_{gs} \) as a function of Indium content reported by Kalna et al. [44].
K. Kalna et al. [40, 41] have carried out Monte Carlo (MC) calibrated Drift-Diffusion (DD) simulation on short gate length HFET to improve the velocity overshoot in the channel. The carrier density in the channel drops because of reduction of the gate-to-channel distance in proportionally scaled processes. The reduction in the carrier density, which affects the power handling capability of the devices, may be compensated when an additional δ-doping layer is placed into the PHEMT structure in order to increase the drive current.

![Figure 2.17 Id-Vg Characteristics as a function of Indium content in HEMT device [44]](image)

2.6.3 Gate Geometry

Even though stages play important roles in LNA design, the gate geometry and bias condition of the two first stage are selected to minimize the noise figure. It also suggested that the gate number, \( R_n \) and \( F_{\text{min}} \) are interrelated to each other [57]. An increase of the gate number considerably decreases \( R_n \) and to a lesser \( F_{\text{min}} \) while decreasing the gate width, \( W_n \) decreases \( F_{\text{min}} \). Higher gain can be obtained by reducing the device size [16, 27]. The T-shape gate is commonly used in submicron device due to the low parasitic effects towards I-V characteristics an excessively studied using Monte Carlo simulations [16,18]. The scaling of devices with gate lengths were varied is performed in both lateral and vertical directions as shown in Figure 2.18. Significant improvement of \( g_m \) during scaling was successfully proved, even though external resistances become a limiting factor. On the other hand, the
thresholds for both impact ionization and thermionic tunnelling decrease with device scaling.

![Figure 2.18 I_D-V_GS characteristics at drain bias of 0.8V as a function of device gate length (nm). The inset presents a gm(max) at V_ds=0.8V [55]](image)

2.7 Submicrometer pHEMT Design

The demands of high speed switching device and systems, power efficiency and large bandwidths for wireless technologies are the basis of recent development of advanced HEMT design and fabrications to pick up with the challenges. One of the most effective ways is by reducing the size of the device [58]. The relation of f_T and gate length reduction in HEMT device is illustrated in Figure 2.19 [59]. Submicron InGaAs/InAlAs on InP substrates could deliver very high f_T above 625GHz [1] and f_max up to 1 THz [23]. Kalna et.al, through MC simulations, reported that such extremely high frequencies can be achieved by using InGaAs channels with Indium content of 0.7 and by scaling of the gate length to 0.25μm [18]. Furthermore, increasing (In) content in the InGaAs channel layer and reducing the gate-channel distance [30] can effectively increase mobility because the average electron velocity under the gate is enhanced. In addition, the channel aspect ratio must be increased to more than one to suppress a marked short-channel effect for sub-50nm gate HEMTs [31].

58
Figure 2.19 Current gain $f_T$ vs $L_g$ for reported state-of-the-art MHEMTs, InP, HEMTs and GaAs PHEMTs [59]

However, further reduction of the transistor size to submicron gate length deteriorates certain performance parameters such as large shift in the threshold voltage and variation of I-V curves. This is known as Short Channel Effect (SCE). It is undesirable for the fabrication of high quality integrated circuit because it affects the device switching time, $f_T$, $f_{max}$ and $V_T$ should be kept invariant with transistor dimensions and biasing conditions. Therefore, the aspect ratio has to be kept high enough to avoid short channel effects [31].
2.7.1 Short Channel Effect

Short Channel Effect (SCE) is an effect in transistor, which occurs when the channel length compared to the depth of the drain and source junctions and depletion width causes the threshold voltage and I-V curve variation. The short-channel effects are attributed to two physical phenomena; the limitation imposed on electron drift characteristics in the channel and the modification of the threshold voltage due to the shortening channel length. By reducing the channel length to increase the device speed, the short channel effects arise. In particular, improved RF performance can be obtained preserving a minimum aspect ratio of 5, limiting in such way short channel effects and reducing the electron transit time through the reduction of the effective gate length. Further improvement can be obtained reducing the source-gate access region length. Thus, the effective gate length relative increase and the parasitic intrinsic access region resistance are found to be the main factors limiting nanoscale scaling in THz InGaAs HEMTs [32].

Theoretically, the short channel effect becomes one of the problems when the gate length is scaled down to the nanometer regime. A number of problems have been identified, namely high output conductance, drain induced barrier lowering (DIBL), the gate to drain capacitance increase which in turn reduces the $f_{\text{max}}$ of the device [28] and thinning of barrier [18]. As the source & drain get closer, they become electrostatically coupled, so that the drain bias can affect the potential barrier to carrier flow at the source junction hence sub-threshold current increases. The aspect ratio, $a$ of the channel is defined as the ratio of gate length, $L_G$ to the thickness of the doped layer, $d$, given by Equation 2.31:

$$a = \frac{L_G}{d}$$  \hspace{1cm} \text{Equation 2.31}
2.7.2 Submicron pHEMT T-gate Structure

In advanced devices, the parasitic resistances play a non negligible role. A winning idea was to produce gate smaller at the bottom and bigger on the top, very similar to a mushroom. The head of the mushroom lowers the gate resistance. This novel gate was called T–gate or mushroom gate. During the years, it has been improved and used also as mask during ohmic contact deposition, leading to self–aligned T–gate process. In 1992, a 65nm self-aligned-gate In$_{0.52}$Al$_{0.48}$As/In$_{0.8}$Ga$_{0.2}$As p–HEMT reached operating frequencies higher than 300GHz [7], while the InP-based power HEMT reached frequencies in the range of 600GHz in 1995 [8].

Over the years, the submicron pHEMT regime has achieved significantly improved device performances, i.e., $g_m$, $f_T$, and $f_{max}$. Some of the epilayer design structures for submicron pHEMTs are illustrated in Figure 2.20. By reducing the gate length, $f_T$ can be increased. A T-shaped gate is required in order to minimize the gate resistance for devices with small gates and the T-shape gate contact is chosen in the devices because it reduces the series resistance of the gate stripe and hence $R_G$ [33]. However, the cross section of gate-metallization would be significantly larger for T-gate structure.

Further investigation reported by Md. Tanvir Hasan et al [34] found that the 2DEG sheet carrier concentration and mobility for DHEMT is higher than conventional SHEMTs. The high values of 2DEG sheet carrier concentration and mobility strongly suggest that the InGaN/InN/InGaN based double channel HEMT is very promising for the fabrication of high performance high speed device. Another extensive work on Double Gate HEMT (DGHEMT) and Single Gate HEMT (SGHEMT) has been done by S.Rathi et.al [26] to analyse the variation of DC and $L_G$ towards the $g_m$, $f_T$, $f_{max}$, and the ability of these structures to compensate the short channel effect (SCE).
Figure 2.20 Submicron Epilayer Structure and Gate Design: (a) T-Shape/Mushroom gate [18], (b) T-gate lattice-matched HEMT [14], (c) InAs channel HEMT [60], and (d) InGaN/InN/InGaN-based double channel HEMT [34].
2.8 The Milestone of pHEMT

The milestones in pHEMT development are summarised in Table 2.2. Back in the 1950’s, research was motivated by the first demonstration of a heterojunction device proposed by Shockley [61]. Since then, each decade has seen significant work progresses towards the development of the pHEMT. In 1969, Esaki and Tsu proposed the concept of the modulation-doped super-lattice. The knowledge of super-lattice behaviour [62] and the application of MBE growth techniques [63][64] led to the first patent by Dingle, et al. Inspired by the super-lattice structure, Mimura, et al. came up with the concept of using a field effect to modulate electrons at the interface of a heterostructure consisting of an un-doped GaAs and n-type AlGaAs pair the device principle of HEMTs was was patented in 1980 [65].

<table>
<thead>
<tr>
<th>Ref</th>
<th>Heterostructure Development</th>
<th>Year Published</th>
</tr>
</thead>
<tbody>
<tr>
<td>[61]</td>
<td>Heterostructure device proposed (patent No.2569347)</td>
<td>1951</td>
</tr>
<tr>
<td>[66]</td>
<td>Mobility Enhancement in superlattice heterojunction predicted for As/AlGaAs system</td>
<td>1969</td>
</tr>
<tr>
<td>[63][64]</td>
<td>Molecular Beam Epitaxy demonstrated</td>
<td>1969</td>
</tr>
<tr>
<td>[62]</td>
<td>Mobility Enhancement in GaAs/AlGaAs demonstrated</td>
<td>1978</td>
</tr>
<tr>
<td>[65][68]</td>
<td>First demonstration of HEMT device</td>
<td>1980</td>
</tr>
<tr>
<td>[69][70]</td>
<td>Pseudomorphic HEMT introduced</td>
<td>1985</td>
</tr>
<tr>
<td>[71]</td>
<td>Present InGaAs/AlGaAs pHEMT structure introduced</td>
<td>1986</td>
</tr>
<tr>
<td>[72]</td>
<td>Pulse-doped pHEMT demonstrated</td>
<td>1987</td>
</tr>
<tr>
<td>[73]</td>
<td>First InP pHEMT with highest f_T reported</td>
<td>1988</td>
</tr>
<tr>
<td>[74]</td>
<td>First pHEMT-based MMIC reported</td>
<td>1989</td>
</tr>
<tr>
<td>[46]</td>
<td>InP pHEMT with f_{max} greater than 1THz</td>
<td>2007</td>
</tr>
</tbody>
</table>

The remarkable Pseudomorphic HEMT (pHEMT) device was first introduced in 1985 [64,65]. After that, continuous work has been undertaken in device improvements from the conventional pHEMT, to the pulse-doped (δ-doped) pHEMT and extended to the fully functional pHEMT MMIC [66,67,69,70]. The 1990’s is the decade in which the pHEMT began to enter the marketplace. The interest on refining pHEMT performance continues until the maximum frequency in THz region was reported in 2007.
In particular, HEMT devices are ideally suited for critical front-end amplification stage of a low-noise microwave receiver system. HEMTs and pHEMTs are also widely used in MMIC design, mm-wave system, communications systems and RADAR. GaAs and InP HEMTs offers an outstanding performance of high transconductance and linearity under low dc bias operation, small size, and low noise figure capability at L-, S-, and C-band frequencies [76][77] makes them the best candidates for these applications.

2.9 Summary

The theory and fundamentals of heterojunction and pHEMT structure has been presented in this chapter. This includes explanations of the lattice matched, pseudomorphic material system and the key equations governing pHEMT operations. The factors which contribute to the superior characteristics of the device, which make it suitable for use in low noise applications were also discussed. The compressively strained In$_x$Ga$_{1-x}$As ($x > 0.7$) channel in the HEMT epitaxial is the key to the outstanding device performance. Besides, some literature works on the InAlAs/InGaAs HEMT advances were discussed. An overview of the milestone of pHEMT development, from the heterostructure concept proposed in 1951, to the first pHEMT reported in 1985 are also highlights. An understanding of the basic principle and operations of the pHEMT device will be used to realise the device modelling which will be finally implemented in LNA designs in later chapters.
3 CHAPTER 3

DEVICE MODELLING IN ATLAS SILVACO

3.1 Introduction

Physical simulation provides insights into the underlying device phenomena observed in the fabrication processes. Through the device simulation, certain internal device variables which cannot be observed directly from device terminal $I-V$ measurements such as the 2DEG density, energy band diagrams, electric field, trap density, etc., can be observed and able to reproduce the DC and RF output characteristics. Hence, it is important to employ device simulation to study the InGaAs/InAlAs pHEMT device behaviour. However, this demands precise material parameters in the model statement in order to provide accurate insight of the device behaviour.

For the past decades, the physical models for HEMTs have been developed mostly for the AlGaAs/InGaAs [78], GaAs/AlGaAs, GaN/AlGaN [79] and lattice matched InGaAs/InAlAs [45] material system. For InGaAs/InAlAs material system, modelling for the lattice matched system becomes more mature as the database for material parameters become more precise and accurate. However, for high indium (In) content, the material parameter still need to be studied for improvement in fitting the experimental data. Therefore, it is very difficult to find one specific values for the device parameter and this has led to the development of physical modelling of fitting and optimisation of the device parameters. Further details on physical device models and parameters that govern the model is presented and the models used in the physical device simulations are discussed in the following sections.
3.2 Basic Equations

The mathematical models implemented in ATLAS consist of a set of fundamental equations, which link together the electrostatic potential and the carrier densities, within some simulation domain. These are derived from Maxwell’s equations and consist of Poisson’s Equation, Carrier Continuity Equations and Transport equations. Poisson’s Equation relates variations in electrostatic potential to local charge densities [80]. The continuity and the transport equations describe the way that the electron and hole densities evolve as a result of transport processes, generation processes, and recombination processes.

3.2.1 Maxwell's Equations

The elementary semiconductor equations are derived from Maxwell's equations stated by the following equations [80],

\[ \nabla \times \vec{H} = \vec{J} + \frac{\partial \vec{D}}{\partial t} \]  \hspace{1cm} \text{Equation 3.1} \\
\[ \nabla \times \vec{E} = -\frac{\partial \vec{B}}{\partial t} \]  \hspace{1cm} \text{Equation 3.2} \\
\[ \nabla \cdot \vec{D} = \rho_c \]  \hspace{1cm} \text{Equation 3.3} \\
\[ \nabla \cdot \vec{B} = 0 \]  \hspace{1cm} \text{Equation 3.4} 

In the Equation 3.1 to Equation 3.4, \( \vec{E} \) and \( \vec{H} \) are the electric and magnetic fields, while \( \vec{D} \) and \( \vec{B} \) are the displacement and induction vectors. \( \vec{J} \) denotes the conduction current and \( \rho_c \) stands for electric charge density.
3.2.2 Poisson's Equation

The Maxwell’s equation then influences Poisson's equation as in Equation 3.5. The displacement vector $\vec{D}$ and electric field $\vec{E}$ in Maxwell’s equations are related by the expression:

$$\vec{D} = \varepsilon \vec{E}$$ \hspace{1cm} \text{Equation 3.5}

with the assumption that the material permittivity, $\varepsilon$ is isotropic and homogenous. Hence, $\vec{E}$ can be defined as a spatial rate of change of electrostatic potential, $\psi$ given by;

$$\vec{E} = -\nabla \psi$$ \hspace{1cm} \text{Equation 3.6}

Equating Equation 3.5 and Equation 3.6, this can be written as;

$$\nabla \cdot \vec{D} = -\nabla \cdot (\varepsilon \nabla \psi) = \rho_c$$ \hspace{1cm} \text{Equation 3.7}

or $$\varepsilon (\nabla^2 \psi) = -\rho_c$$ \hspace{1cm} \text{Equation 3.8}

which is well known as Poisson's equation. By taking the $\rho_c$ as a function of elementary charge, $q$ times holes and electron concentrations, and $C$ as the variation in charge density due to generation and recombination mechanisms; hence the Poisson's equation can be written as in Equation 3.9,

$$\rho_c = q(p - n + C)$$ \hspace{1cm} \text{Equation 3.9}

$$\nabla^2 \psi = \frac{q}{\varepsilon} (p - n + C)$$ \hspace{1cm} \text{Equation 3.10}
3.2.3 Carrier Continuity Equations

The continuity equations for electrons and holes are defined by Equation 3.11 and Equation 3.12 [80]:

\[
\frac{\partial n}{\partial t} = \frac{1}{q} \text{div} \vec{J}_n + G_n - R_n \quad \text{Equation 3.11}
\]

\[
\frac{\partial p}{\partial t} = \frac{1}{q} \text{div} \vec{J}_p + G_p - R_p \quad \text{Equation 3.12}
\]

where \( n \) and \( p \) are the electron and hole concentration, \( \vec{J}_n \) and \( \vec{J}_p \) are the electron and hole current densities, \( G_n \) and \( G_p \) are the generation rates for electrons and holes, \( R_n \) and \( R_p \) are the recombination rates for electrons and holes, and \( q \) is the magnitude of the charge on an electron. By default, ATLAS includes both equations in the simulation.

3.2.4 Carrier Transport Equations

Electrons in thermal equilibrium at temperature, \( T_L \), within a semiconductor lattice obey the Fermi-Dirac statistics. Usually, the Boltzmann approximation is used to solve the continuity equations for electron and hole densities. In some cases where \( E - E_F \gg kT_L \), the approximation probability for an available electron state with energy \( \varepsilon \) is occupied by [80]:

\[
F(\varepsilon) = \exp \left( \frac{E_F - E}{kT_L} \right) \quad \text{Equation 3.13}
\]

where \( k \) is the Boltzmann’s constant and \( T_L \) is the lattice temperature.

3.2.4.1 Drift Diffusion Transport Model

The fundamental part of the device simulation is based on the drift diffusion model. It is the basic model for charge transport which is a simplification of Boltzmann
Transport Equation and is adequate for micron level device simulations. The drift diffusion transport model approximates the continuity equations to derive the current densities. However, the non-local transport effects such as velocity overshoot and diffusion due to carrier temperature are not accounted for in this model. The carrier current density \( \vec{J} \) for electrons \( (n) \) is given by;

\[
\vec{J}_n = q\mu_n n \vec{E} + qD_n \nabla n
\]

Equation 3.14

where \( \mu_n \) is the electron mobility, \( \vec{E} \) is the local electric field in \( \text{V/cm} \), and the diffusion coefficient, \( D \) is calculated using Einstein’s relationship as;

\[
D_n = \frac{kT}{q} \mu_n
\]

Equation 3.15

### 3.2.4.2 Energy Balance Transport Model

As a basic solution, the drift-diffusion transport model lacks relation to non-local transport effects such as velocity overshoot, diffusion due to carrier temperature and effect of carrier energy distributions on impact ionization rates. These mechanisms are more pronounced in submicron devices and can be simulated using the energy balance transport equations. The current density expressions from the drift-diffusion model are modified to include this additional physical relationship. The conduction current densities for the energy balance relation and the energy flux relation is expressed in Equation 3.16 and Equation 3.17, respectively;

\[
\vec{J}_n = q\mu_n n \left( \nabla \left( \frac{E_c}{q} - \varphi \right) + \frac{k_B N_{e,0}}{q} n \nabla \left( \frac{nT_n}{N_{e,0}} \right) \right)
\]

Equation 3.16

\[
\nabla \cdot \vec{S}_n = \nabla \left( \frac{E_c}{q} - \varphi \right) \cdot \vec{J}_n - \frac{3k_B}{2} \left( \frac{\partial (nT_n)}{\partial t} + R_{T_n} + n \frac{T_n - T_{\text{L}}}{\tau_{e,n}} \right)
\]

Equation 3.17
3.3 Introduction to ATLAS

Extensive physical models of HEMT devices have been performed using other software tools, i.e. Monte Carlo [81][82], MINIMOS-NT [78], APSPA [22] and DESSIS [39]. In this work, the physical model of pHEMT is generated using ATLAS; a physical device simulator in the SILVACO software package [38]. ATLAS solves the structure definitions, numerical and physical models in 2D and 3D. It has the ability to predict the performance characteristics of a device and provides an insight into the internal physical mechanisms associated with device operation using physically based models, i.e. impact ionization coefficients, trap surface density, Fermi pinning level, etc. It is also able to simulate the electrical, optical, thermal characteristics of a semiconductor device at bias conditions to obtain the DC, RF and time domain response. An input deck was generated in the DECKBUILD™ environment developer, solved through the ATLAS™ routine, and analysed utilizing the TONYPLOT™ tool. DeckBuild provides a text editor platform for ATLAS commands and serves as an interpreter for executing ATLAS statements. Additionally, ATLAS uses the sub-engine BLAZE™ routine, a routine specifically designed for group III-V materials and devices with position dependent band structures was utilized to simulate the InAlAs/InGaAs HEMT. A graphical representation of the ATLAS interfaces is given in Figure 3.1.

![Figure 3.1 ATLAS Input-Output Hierarchy [80]](image-url)
Atlas simulations can be done with two types of input files; Structure file and Text (command file). The text file which is developed in the DeckBuild environment contains the commands for ATLAS to be executed while the structure file defines the structure to be simulated, either using DevEdit or Athena environment. ATLAS simulator provides three output files; Run-time output file, Log file and Solution file. The run-time output file lists out the progress and error and warning messages as the commands are being simulated. The Log file stores all the terminal voltages and currents from the device analysis that have been solved using numerical calculation. The Solution file stores the 2D and 3D data relating to the values of solution variables within the device at a given bias point. Both the log and solution output files generated in the simulations can be visualized in Tony Plot.

![Diagram of ATLAS Command Groups Statement]

Figure 3.2 ATLAS Command Groups Statement [80]
The flowchart illustrated in Figure 3.2 is the flow of instruction to develop a device model in ATLAS. The flow of statement definition must be in order for the execution of device characteristics. The material statements are used to define the physical parameters of the material system which relates the band energy, mobility, recombination, carrier statistics, electron-hole masses and electron affinity.

The model statements specify the physical mechanism, models and other parameter such as temperature and bandgap narrowing. The numerical solution method and data convergence are defined by the METHOD statement to calculate the current-voltage solution under a range of bias points. ATLAS sets up the equations with an initial guess to the parameter values by solving the equilibrium case and then iterates to obtain a converged solution. If data is not converged after a few iteration points, the simulations is stopped. Two types of approaches are used to achieve acceptable correspondence values. One is the Gummel method also known as de-coupled approach, which solves the necessary equations sequentially, providing linear convergence. This approach is useful when there is weak coupling between the resultant equations. The other is the Newton method, which provides quadratic convergence. This kind of approach is used in the case of strong coupling between the resultant equations.

The physical model definition is grouped into five classes, namely MOBILITY, RECOMBINATION, CARRIER STATISTICS, IMPACT IONIZATION, and TUNNELING. The physical models were enabled on a material by material basis. This is useful for heterojunction device simulation and other simulations where multiple semiconductor regions are defined and may have different characteristics [80].

3.4 Structure Definition

A device structure can be defined in ATLAS in three different ways; 1) DevEdit, 2) ATHENA and 3) ATLAS commands in DeckBuild as illustrated in Figure 3.1. The DevEdit environment provides a graphical user interface for the development of structure and the ability to define regions in the form of polygons with at least three
multiple points. It can also perform auto-meshing for the developed structure depending upon the constraints defined by the developer. A structure created in DevEdit can be imported and used in ATLAS for device simulation. However, the user needs to define the material and physical model statement for the structure in DeckBuild. The accuracy of device simulation depends on the material parameter's value and the physical model definition. In ATLAS command, the device structure is modelled by defining the MESH, REGION, ELECTRODES and DOPING statement [80]. Each of the statements will be discussed in the following subtopics.

3.4.1 Epitaxial Layer Structure

The device 2D structure is defined in DeckBuild using the ATLAS command line. The device structure is developed using ATLAS command using REGION statement. Figure 3.3 shows an example of the epitaxial layer, i.e., VMBE2100 epitaxial structure which is used in the pHEMT device fabrication. The information about epitaxial layers, i.e., material composition, layer sequence, thickness, and energy band band gaps are defined in the REGION statement. The complete top-down epitaxial layer, material compositions, bandgap values and the thicknesses used in the physical modelling work for pHEMTs sample VMBE2100 and XMBE131 are given in APPENDIX D.

<table>
<thead>
<tr>
<th>Layer</th>
<th>Bandgap</th>
<th>Value (eV)</th>
<th>Material</th>
<th>Thickness (Å)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cap</td>
<td>Narrow</td>
<td>0.7</td>
<td>In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>50 Å</td>
</tr>
<tr>
<td>Supply</td>
<td>Wide</td>
<td>1.98</td>
<td>In$<em>{0.3}$Al$</em>{0.7}$As</td>
<td>300 Å</td>
</tr>
<tr>
<td>δ-doped</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>10 Å</td>
</tr>
<tr>
<td>Spacer</td>
<td>Wide</td>
<td>1.98</td>
<td>In$<em>{0.3}$Al$</em>{0.7}$As</td>
<td>100 Å</td>
</tr>
<tr>
<td>Channel</td>
<td>Narrow</td>
<td>0.602</td>
<td>In$<em>{0.7}$Ga$</em>{0.3}$As</td>
<td>160 Å</td>
</tr>
<tr>
<td>Buffer</td>
<td>Wide</td>
<td>1.48</td>
<td>In$<em>{0.52}$Al$</em>{0.48}$As</td>
<td>4500 Å</td>
</tr>
<tr>
<td>Substrate</td>
<td>-</td>
<td>-</td>
<td>S.I. InP</td>
<td>2.5µm</td>
</tr>
</tbody>
</table>

Figure 3.3 Epitaxial layer profile for Sample VMBE2100 used for device structure
3.4.2 Electrodes and Contacts

In a HEMT device, the drain and source make ohmic contacts while the gate forms a Schottky contact with the semiconductor materials. In ATLAS, these terminals are defined in the ELECTRODE statement [80,[83]. Table 3.1 shows the electrode definition described in the ATLAS DeckBuild command and Figure 3.4 shows the electrodes and the contact of the device model. $L_{sg}$ and $L_{gd}$ are the distance of the drain and source from the gate which is set to be 2 $\mu$m. The Schottky-gate metal work function, $\phi_m$ is defined as 4.70 eV to achieve a Schottky barrier of 0.65 eV. For the XMBE2100 pHEMT structure 2D simulations, the resistance at the source and drain contact is optimised at 1600 $\Omega$.\mu m which results in 0.16 $\Omega$.\mm for the complete extrinsic device. This parameter value is calibrated and optimised to reproduce an accurate linear region for the pHEMT I-V characteristics as compared to the experimental results.

<table>
<thead>
<tr>
<th>Description</th>
<th>Electrodes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electrodes type</td>
<td>Source</td>
</tr>
<tr>
<td>Electrodes type</td>
<td>Ohmic</td>
</tr>
<tr>
<td>Workfunction (eV)</td>
<td>-</td>
</tr>
<tr>
<td>Resistance ($\Omega$.\mu m)</td>
<td>1600</td>
</tr>
<tr>
<td>Length ($\mu$m)</td>
<td>$L_{sg} = 2$</td>
</tr>
</tbody>
</table>

In ATLAS Silvaco, the schottky contacts can be modelled in two different ways [84]: (1) work-function of electrode metal method or (2) surface recombination method. In the physical modelling, the electrode metal work-function is defined as a potential difference in the electron affinity of the semiconductor, $\chi_S$, and the Schottky barrier height, $\Phi_B$, i.e.,

$$\Phi_m = \chi_S - \Phi_B \quad \text{Equation 3.18}$$

The gate electrode is placed over the supply layer by simulating the cap layer recess etching. In the model, the metal-semiconductor alloying process is expressed as the following steps due to thermal annealing: (1) the region below the source and drain
electrodes are heavily doped (~2x10^{19} \text{ cm}^{-3}) to simulate the diffusion of electrons into the semiconductor and (2) by defining the drain and source electrodes till the channel for simulating the alloying and metal diffusion process [78]. The other two electrodes; Source and Drain are defined as an ohmic contact. Therefore, no metal work function is required in the model statement.

![Diagram of Ohmic Contact and Schottky contact defined in VMBE2100 pHEMT model.](image)

The source and drain electrode are stretched until the end of the channel layer.

In the 2D model simulation, it is assumed that the majority and minority carrier quasi-Fermi potentials, \( \Phi_n \) and \( \Phi_p \) are equal to the applied bias potentials [83]. There are two steps considered in the simulations for the metal semiconductor alloying process due to thermal annealing in the ohmic regions; (1) the region below the source and drain electrodes are heavily doped (~2x10^{19} \text{ cm}^{-3}) till the end of the channel, to simulate the diffusion of electrons into the semiconductor and step (2) by defining the drain and source electrodes till the channel for simulating the alloying and metal diffusion process.
3.4.3 Doping Concentration

The physical HEMT model employed modulation doping mechanism. All the layers of the device are kept undoped except for the δ-doped layer between the supply and spacer layers. The δ-doped layer is heavily doped and supplies the electrons that diffuse through the spacer layer and fall into the quantum well which then forming the 2DEG channel. The doping at the interface(s) between regions can be defined with an analytical profile, which is used with the parameters NAME, MATER, and REGION. The NAME, MATER, and REGION parameters are used to describe the regions that receive the doping concentration. In device structure modelling, the locations of these interface profiles must be defined and is also restricted by the location parameters X.MAX, X.MIN, Y.MAX, and Y.MIN. Table 3.2 tabulated the types of doping profile. An n-type or donor dopant is defined with N.TYPE, N-TYPE, DONOR while for a p-type, P.TYPE, P-TYPE, ACCEPTOR generic statement is used.

Table 3.2 Parameters to specify a doping profile [80]

<table>
<thead>
<tr>
<th>Type of doping</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>GAUSSIAN</td>
<td>Specifies the use of a Gaussian analytical function to generate the doping profile. If GAUSSIAN is specified, the following parameters must also be specified: (i) Polarity parameter: N.TYPE or P.TYPE (ii) One of the following groups of profile specifications: - CONCENTRATION and JUNCTION - DOSE and CHARACTERISTIC - CONCENTRATION and CHARACTERISTIC</td>
</tr>
<tr>
<td>UNIFORM</td>
<td>Specifies the use of uniform (constant) analytical functions to generate the doping profile. If UNIFORM is specified, the N.TYPE, P.TYPE, and CONCENTRATION parameters must be specified. Doping is introduced into a box defined by the boundary parameters.</td>
</tr>
</tbody>
</table>

A uniform or Gaussian doping profile can be defined for the δ-doped region. The conduction band diagram and electron concentration remains unchanged for both the
kind of doping definitions, but it does change with the concentration levels [85]. Figure 3.5 shows the conduction and valence bands as a function of sheet concentration, \( n_s \), as reported in [85]. It can be observed that higher doping concentration in the material system, will result in larger band bending at the heterostructure interface.

![Figure 3.5 Band profile for a HEMT as a function of sheet concentration in the channel (from [85])](image)

A Gaussian doping profile has been selected for VMBE2100 pHEMT device model with a peak doping concentration of \( 2.85 \times 10^{19} \text{ cm}^{-3} \) and characteristic width of 8.4 Å. With this doping concentration, the sheet carrier density in the channel is \( 2.45 \times 10^{12} \text{ cm}^{-2} \). Figure 3.6 illustrates the doping profile and the sheet concentration in the channel layer for the modelled device which is observed in Tonyplot. Increasing the ionized donor in the \( \delta \)-doped layer increases the channel sheet carrier concentration. However, it introduces the parallel conducting channel in the donor layer. The sheet carrier concentration has a direct impact on the device threshold voltage [86].
Figure 3.6 The electron concentration in $\delta$-doped layer and carrier concentration in Channel layer for XMBE2100 structure

### 3.4.4 Heterojunction Band Alignments

The difference in the two bandgaps creates an abrupt discontinuity in the valence and conduction bands. Simulation of heterojunction devices in ATLAS™ is accomplished through BLAZE™, a compound material 2D simulator. BLAZE™ accounts for the effects of positionally dependent band structure by modifications to the charge transport equations [80]. At equilibrium, the energy band diagram of a modelled device gives information about several parameters, such as Schottky barrier height, depth of potential well formed due to the heterojunction in the channel and extent of band bending in the supply and spacer layers due to heavy doping in the $\delta$-doped layer. The band diagram is primarily affected by the material parameters i.e, the electron affinities, energy band gaps, contact work-function for the gate electrode and permittivities. Figure 3.7 demonstrates the energy band diagram of the modelled device at thermal equilibrium.
Figure 3.7 Energy band diagram for the VMBE2100 pHEMT structure model in ATLAS

In ATLAS, the Schottky barrier height is primarily determined by the $\phi_m$ and $\chi_S$. The potential well forming the channel has a conduction band below the Fermi level, thus creating a 2DEG in the channel. The discontinuity in the conduction band at the channel buffer interface provides a barrier for carrier confinement in the channel.

### 3.5  Mobility Model for pHEMT

The HEMT device is very similar to a MESFET, thus the electrons in the pHEMTs sample i.e. VMBE2100 and XMBE131 are accelerated by the electric field. Therefore, electrons lose momentums due to the numerous scattering processes, including lattice vibrations (phonons), impurity ions, other carriers, surfaces or material imperfections [38]. For our modelling purposes, the low field behaviour and high field behaviour have been taken into account.
3.5.1 Low Field Mobility Model

In the low field mobility model, carriers are almost in equilibrium with the lattice and the mobility has a low field characteristic value, $\mu_{n0,p0}$. ATLAS models the low field carrier mobility in a number of ways, the simplest is constant low field mobility that accounts for lattice scattering due to temperature but does not account for other scattering mechanisms. These scattering processes may be caused by impurity ions, surface and material imperfections. The simplistic mobility model is independent of doping concentration, carrier density and electric field. The effective carrier mobility $\mu_{n0}$ is given by;

$$\mu_{n0}(T) = \mu_{n} \left( \frac{T_L}{300} \right)^{-T\mu_{n}}$$  \hspace{1cm} Equation 3.19

where $\mu_{n0}$ is the carrier mobility at 300K, $T_L$ is the lattice temperature and $T\mu_{n}$ is the power coefficient for temperature dependence.

Another model is the Concentration Dependant Low Mobility model, defined as 'CONMOB' in the ATLAS command. It provides the empirical data for the doping dependent low-field mobilities of electrons and holes at T=300K. A relatively advanced model for simulating concentration and temperature dependent mobility in ATLAS are given by Caughey and Thomas or the Arora’s model [80]. The Caughey Thomas Analytic Low Field Mobility model was used for the InAlAs material parameter. The analytical expression given by Caughey and Thomas is:

$$\mu(N,T) = \mu_{1v} \left( \frac{T_L}{300} \right)^{-\alpha_{v}} + \frac{\mu_{2v} \left( \frac{T_L}{300} \right)^{\beta_{v}} - \mu_{1v} \left( \frac{T_L}{300} \right)^{\alpha_{v}}}{1 + \left( \frac{T_L}{300} \right)^{\gamma_{v}} \left( \frac{N}{N_{ref,v}} \right)^{\delta_{v}}}$$  \hspace{1cm} Equation 3.20

In the above expression, $\mu_{1v}$ and $\mu_{2v}$ are the minimum and maximum values for mobility, $N$ denotes the net impurity concentration, $\alpha_{v}$, $\beta_{v}$, $\gamma_{v}$ and $\delta_{v}$ are different power coefficients for temperature and impurity concentration dependence.
Different mobility models are applied to the layers of the modelled device depending upon the presence of ionized impurities [85]. The supply and spacer layers are modelled using CONMOB statement due to the presence of the δ-doped donor layer. As the ionized impurity donors diffuse into the supply and spacer layers, the impurity concentration in these layers rise and the mobility degrades due to ionized impurity scattering [84]. The electron mobility under equilibrium condition is plotted in Figure 3.8.

![Image](image.png)

Figure 3.8 Simulations of Electron Mobility in the Channel Layer (In$_{0.7}$Ga$_{0.3}$As material)

### 3.5.2 High Field Mobility Model

The carrier mobility declines with electric fields as the scattering processes increase with increase of carrier energy. The carrier drift velocity rises slowly at high electric fields and eventually saturates. Various high field mobility models have been used [45], [87] to account for the reduction in mobility at high fields and the smooth transition of mobility value from the low field effect to high field effect. In this work, the Caughey and Thomas high field mobility model is used. The Caughey-Thomas model accounts [80] for the velocity saturation effect with increasing
electric field component parallel to the direction of current. This model provides a smooth transition of carrier mobility between low field and high field behaviour.

In ATLAS, there are two types of field dependent mobility (FLDMOB) models; 
*Standard Mobility Model* and *Negative Differential Mobility*. Both of these models have an appropriate default parameter values for different materials. The models are implemented by defining EVSATMOD along with the FLDMOB model statement. The EVSATMOD statement specifies which parallel field dependent mobility model should be used for the carrier in the device, which is defined as:

- EVSATMOD=0 allows the application of standard mobility model
- EVSATMOD=1 implements the GaAs negative differential mobility saturation model
- EVSATMOD=2 implements the simplified the field dependent velocity model. It applies the standard electric field based mobility model without using the temperature dependent mobility

The standard mobility model was used for the InGaAs region. This model is defined in terms of electron saturation velocity, as a function of applied electric field. In ATLAS, the model is implemented using the Caughey Thomas expression to provide a smooth transition between the low-field and high-field behaviour;

### 3.6 Modelling the Physical Mechanisms

This section explains the physical mechanism employed in the model i.e generation recombination, trap and defects and impact ionisation. Mechanisms other than these three have not been used in this work and thus will not be discussed in this text. Related graphs from the simulations are given and explained in the following sections.
3.6.1 Carrier Generation-Recombination Mechanisms

There are several processes responsible for carrier generation and recombination. These includes phonon transitions, photon transitions, Auger transitions, surface recombination, impact ionization and tunnelling. All of these generation-recombination mechanism are implemented with different models.

Under equilibrium conditions, the carrier concentration of electrons, \( n_0 \), and \( p_0 \) of holes are related to the intrinsic concentration, \( n_i \), which are defined by,

\[
n_0 p_0 = n_i^2 \tag{3.21}
\]

Although the carrier concentrations fluctuate continuously due to the thermal energy, equilibrium is maintained because of generation and recombination mechanisms taking place. However, any external stimulus may disturb this mechanism, hence forcing the carrier concentrations to deviate from their equilibrium values. The physical generation/recombination mechanisms used in the device modelling is listed in Table 3.3.

<table>
<thead>
<tr>
<th>Model</th>
<th>Syntax</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Shockley-Read-Hall</td>
<td>SRH</td>
<td>Phonon transition- Uses fix minority carrier lifetimes.</td>
</tr>
<tr>
<td>Auger</td>
<td>AUGER</td>
<td>Direct transition of three carriers. Important at high current densities</td>
</tr>
<tr>
<td>Impact ionization</td>
<td>IMPACT</td>
<td>Recommended in most cases. Includes temperature dependent parameter (Selberherr Model)</td>
</tr>
<tr>
<td></td>
<td>SELB</td>
<td></td>
</tr>
</tbody>
</table>
3.6.1.1 Shockley-Reed-Hall (SRH) Model

This mechanism proposed by Shockley and Reed, and then by Hall [80] states that phonon transitions take place due to defects (traps) within its forbidden gap. The SRH model involves four partial processes: (1) Electron Capture, (2) Hole Capture, (3) Hole Emission and (4) Electron Release, as described by Selberherr [88]. Process (1) and (2) are recombination processes in which a free carrier no longer remains available for conduction while the latter two processes are generation processes in which carriers become available for conduction. The generation/recombination rate, \( R^{\text{SRH}} \) is given by the relationship:

\[
R^{\text{SRH}} = \frac{np - n_i^2}{\tau p_0 \left[ n + n_i \exp \left( \frac{E_{\text{trap}}}{kT_L} \right) \right] + \tau n_0 \left[ p + n_i \exp \left( -\frac{E_{\text{trap}}}{kT_L} \right) \right]}
\]

Equation 3.22

where \( E_{\text{trap}} \) is the difference between trap energy level and intrinsic Fermi level and \( \tau p_0 \) and \( \tau n_0 \) are respective lifetimes for electrons and holes in equilibrium condition, which were defined for each individual In\(_x\)A\(_{1-x}\)As region.

In the presence of deep-level traps, the expression for SRH recombination is modified to accommodate the variation in concentration of carriers as the carriers are emitted or captured by the acceptor or donor layers. The recombination parameter is then defined as

\[
R^{\text{SRH}} = \sum_{a=1}^{l} R_{D\alpha} + \sum_{\beta=1}^{m} R_{A\beta}
\]

Equation 3.23

\( l \) and \( m \) are the number of donor-like or acceptor-like trap energy level respectively, \( R_{D\alpha} \) denotes the recombination rate for donor-like traps located at an energy level \( E_\alpha \) and similarly \( R_{A\beta} \) denotes the recombination rate for acceptor-like traps located at energy level \( E_\beta \). The terms \( d_\alpha \) and \( d_\beta \) are the trap degeneracy factor. The value is calculated by Equation 3.24 and Equation 3.25 [80]:
The electron and hole lifetimes, indicated by $\tau_n$ (TAUN) and $\tau_p$ (TAUP) that can be found in the Equation 3.26 and Equation 3.27 are related to the capture cross section, SIGN and SIGP which is given by:

\[
\tau_n = \frac{1}{SIGN \, v_n, \text{DENSITY}} \quad \text{Equation 3.26}
\]

\[
\tau_p = \frac{1}{SIGP \, v_p, \text{DENSITY}} \quad \text{Equation 3.27}
\]

The thermal velocities $v_n$ and $v_p$ are calculated from the following electron and hole effective masses,

\[
v_n = \left(\frac{3kT}{m_n m_0}\right)^{1/2} \quad \text{Equation 3.28}
\]

\[
v_p = \left(\frac{3kT}{m_p m_0}\right)^{1/2} \quad \text{Equation 3.29}
\]

In this work, the density of states effective mass is extracted from the density of states ($N_c$ or $N_v$) from parameter value defined in the MATERIAL statement.
3.6.1.2 Auger Recombination Model

Auger or three carrier mechanism is more of a qualitative process in which a mobile carrier is either captured or emitted. In this mechanism, an electron from the conduction band transmits excess energy to another carrier (electron or hole) and itself moves to valence band where it recombines with a hole. Commonly, a standard Auger recombination model is expressed by

\[ R_{auger} = AUGN (pn^2 - n_n^2) + AUGP (np^2 - p_n^2) \]  

Equation 3.30

where the model parameter AUGN and AUGP are material dependent recombination coefficients; is defined in the MATERIAL statement. The AUGER parameter is activated from the MODEL statement.

3.6.1.3 Impact Ionisation

Impact ionisation is purely a generation mechanism that takes place at sufficiently high electric field [45]. The process primarily assumes that under high biased conditions, free carriers accelerate and acquire sufficient energy to generate more carriers by collision with the lattice atoms [80]. The kinetic energy gained by electron, due to high electric field, is mostly imparted in breaking a bond upon impact with the lattice. This energy ionises a valence electron from the valence band to the conduction band, thus generating an electron-hole pair. The generated pair accelerates under the effect of electric field and collides with more lattice atoms, further generating more electron-hole pairs. This recursive process is also referred to as Avalanche process and may even result in device breakdown at considerably high electric fields [89]. The physical simulations consider the impact ionization through the generation term, \( G \). In current continuity equations; \( G \) is given by the electron and hole currents, \( J_n \) and \( J_p \), as in Equation 3.31,

\[ G = \frac{\alpha J_n + \beta J_p}{q} \]  

Equation 3.31

where \( q \) is the elementary charge, \( \alpha \) and \( \beta \) are electron and hole-initiated impact ionization coefficient respectively. The \( \alpha \) can be calculated from the field \( F \) under a uniform electric field by the expression shown in Equation 3.32.
\[ \frac{\alpha}{A_{n}} = \exp\left(-\frac{B_{n}}{F}\right) \]  
Equation 3.32

3.6.2 Traps and Defects

Trapping is generally thought to be due to deep-level electron or hole states in the substrate and/or the surface regions [48,49]. Traps are electrically active defects that result from the discontinuity of lattice periodicity at interfaces and capable of trapping or releasing charge carriers that result in undesired behaviour of the device. They are located within the forbidden energy band and may occupy one or more possible energy state, either filled or empty. Some reported results for deep-level traps in InAlAs/InGaAs systems can be found in [48,50,51]. Traps are classified into two basic types as donor-like traps or acceptor-like traps and they modify the SRH recombination models. Traps are modelled using ‘TRAP’ statement in ATLAS. The trap energy level for donor and acceptor-like trap, \( E_{tD} \) and \( E_{tA} \) in the band energy of the material can be visualised as in Figure 3.9. In this work, acceptor-like traps have been defined in the supply, spacer and buffer layers. The effect of adding traps in the model is discussed below.

![Figure 3.9 Definition of the trap energy level for acceptor and donor traps in reference to the conduction and valence band edges [80]](image)

Acceptor-like traps are usually located close to the conduction band. Such traps are negatively charged when filled with an electron and neutral when empty. A filled or ionized trap can either emit an electron or capture a hole. An otherwise empty or
neutral acceptor-like trap is capable of capturing an electron or emitting a hole. Figure 3.10 illustrates the mechanism of an acceptor-like trap.

![Figure 3.10 Carrier Capturing/Releasing Mechanism in Acceptor-Like Traps [80]](image)

There are few possible trap locations identified in the HEMT device. The traps and defects may be on the surface, the interface between two materials, or even in the epitaxial layer (bulk traps) as suggested in [58,69,71] for an AlGan/GaN HEMTs. The electrons in the channel are trapped when there is enough activation energy that can come from the voltage. The captured electrons reduce the sheet electron density in the 2DEG channel, which in turn leads to a reduction in the drain current density as shown in Figure 3.11. Higher trap density results in a lower drain current.

![Figure 3.11 Modelled I-V characteristics for VMBE2100 with Trap (red line) and without Trap (blue line)](image)
3.6.2.1 Effect on Carrier Concentration

Introducing traps in the supply, spacer and buffer layers, leads to the capture of electrons in these layers that would have otherwise been transported to the channel [84][93]. The carrier concentration changes is accounted for by modifying the recombination rate in the carrier continuity equations [93]. Thus the carrier concentration in the channel is considerably reduced. The trap energy level is defined close to mid band gap from the conduction band. For the purpose of simulation, the donor density in the δ-doped layer is therefore increased to overcome the lack of electrons in the channel at thermal equilibrium. This is achieved by increasing the Gaussian width of the δ-doped region from 8.0 Å to 8.9Å, thus effectively increasing the supplied donors in this region.

Figure 3.12 Trap density, N_T value effects on the current-voltage characteristics

The increase in donor concentration alters the energy band diagram, especially in the δ-doped region as very similar concept explained in section 3.4.3 and the graph that has been illustrated in Figure 3.6. The conduction band energy in the δ-doped region becomes deeper with increased doping concentration. The electron concentration also increases in the δ-doped region. The trap density effects on I-V characteristics is shown in Figure 3.12.
3.6.2.2 Effect on Threshold Voltage

The threshold voltage of the modelled device shifts with the new definition of doping concentration in the δ-doped region as shown in Figure 3.13. This rise in threshold voltage is due to the fact that carriers (electrons) captured by the traps at thermal equilibrium are released on the application of bias. These released electrons become available for conduction in the channel, which increases the net carrier density in the channel, thus requiring higher voltages to deplete the carriers in the channel.

![Figure 3.13 The Shift in Threshold Voltage, $V_T$ due to Trap Density, $N_T$](image)

3.7 Summary

Physical device modelling plays an important role in the understanding of semiconductor devices and their design and development process. The ease and use of device modelling has reduced substantially the time and cost required for developing a specific device by greatly reducing tedious iterations of fabrication for device characterisation. Through the device simulation, certain internal device variables which cannot be observed directly from device terminal $I$-$V$ measurements such as the 2DEG density, energy band diagrams, electric field, etc., can be observed and are able to reproduce the DC and RF output characteristics. In this chapter, the ATLAS Silvaco as a physical device simulator is studied to perform the two-dimensional (2D) physical modelling of fabricated In$_{0.7}$Ga$_{0.3}$As/InAlAs pHEMT
devices. This is done by implementing physical processes such as high field dependent mobility model, carrier generation and recombination, deep level trap and impact ionization. Other appropriate models such as Shockley-Read-Hall, Auger and direct recombination are discussed and employed in the model. Some relevant graphs are presented to provide better understanding and demonstrate how the physical mechanisms is taking place in the modelled device. The detail 2D physical models of the fabricated pHEMT devices will be presented in the next chapter.
4 CHAPTER 4

TWO DIMENSIONAL PHYSICAL MODELLING OF ADVANCED In$_{0.7}$Ga$_{0.3}$As/In$_{0.52}$Al$_{0.48}$As pHEMTs

4.1 Introduction

The device simulation is performed with the main goals of providing a steady state and AC small signal characteristics [19]. The DC and AC characteristics can be reproduced for device characterization and analysed to gain better understanding of the internal behaviour of the device structure, i.e. trap, kink effect, etc [47,48,49,50]. Furthermore, the simulation capabilities can also be expanded for device scaling [78]. The physical modelling of one-micrometer and sub-micrometer gate length pHEMT sample devices were developed using two-dimensional numerical device simulations in ATLAS Silvaco tools [80]. The ATLAS simulator tools and the physical models used for the device structure modelling have been explained in details in Chapter 3.

An accurate model requires a good understanding of device physics and also an accurate model statement for the device. Hence, the simulations considers the electro-physical processes such as high field dependent mobility model, carrier generation and recombination, deep level trap and impact ionization. Appropriate models for Shockley-Read-Hall, Auger and direct recombination are taken into account. In this chapter, the physical model for DC and RF simulations are presented and discussed. Relevant graphs and plots are presented to provide better understanding for the physical mechanisms taking place in the device. In the latter section, the results achieved from the modelled device are compared with the DC and RF experimental data for various In$_{0.7}$Ga$_{0.3}$As/In$_{x}$Al$_{1-x}$As pHEMT devices.
4.2 Epitaxial Layer Structure

In this chapter, there were two pHEMT sample devices (VMBE2100 and XMBE131) employed for the device under test. The pHEMT sample devices are modelled and optimised for low noise amplifier applications which will be further discussed in Chapters 5 and Chapter 6. The 4 x 200 μm VMBE2100 pHEMT sample device has a 1 μm gate length, which was initially developed to fulfil the low-noise amplifier requirements of SKA design in the L-band frequency range (NF~0.6 dB at 1-2 GHz) [53,54]. Conversely, the development and fabrication of submicrometer gate (0.25 μm) pHEMT offers promising performance for application at higher frequency range, i.e. C-band and X-band LNA.

All these epitaxial layers were grown using in-house solid-source Molecular Beam Epitaxy (MBE) on RIBER V100H and V90H systems at the University of Manchester. In this work, the epitaxial structure grown in the V90H system is named with prefix VMBE, whilst prefix XMBE denotes growth performed with the V100H system. The performance enhancement of these devices was achieved through advanced band gap engineering, resulting in low gate leakage and an improvement in the devices’ thermal stability as can be observed in VMBE2100 and XMBE131 pHEMT device characteristics [54, 55]. Additionally, the development and fabrication of submicron devices improves circuit low noise performance by means of gate scaling.

The top-down epitaxial layer structure, material compositions, and the thicknesses used in the simulation work for pHEMTs sample VMBE2100 and XMBE131 are presented in Figure 4.1.
The epitaxial layer structures listed in Figure 4.1 feature identical InP substrate and channel. Conversely, the main differences are in the number of δ-doped layer, in the barrier thickness, in the top cap-layer thickness (and doping) and double spacer layer are developed in XMBE131 structure. The VMBE2100 is a conventional structure with a single δ-doped layer while the other two epitaxial layers are developed with double heterostructures. The channel layer in XMBE131 structure is sandwiched between thin In$_{0.52}$Al$_{0.48}$As layers (10nm).

Over the thick semi insulating InP substrate in VMBE2100 structure, can be found a lattice matched In$_{0.52}$Al$_{0.48}$As buffer layer of 450nm and followed by a strained In$_{0.3}$Ga$_{0.7}$As channel layer. This is followed with a 100 Å undoped In$_{0.3}$Al$_{0.7}$As spacer layer which minimised the columbic scattering between the dopants and carriers in the channel. Above the supply layer, a heavily doped silicon δ-doping layer is defined to serve as a donor layer for the channel. The doping concentration in this δ-doped layer is kept very high ($2.5 \times 10^{12}$ cm$^{-2}$) as to achieve sufficient carriers in the channel for conduction. A strained In$_{0.30}$Ga$_{0.70}$As supply layer with the thickness of 200Å is grown on top of δ-doped layer for the Schottky contact. The top layer of the device is 50Å In$_{0.53}$Ga$_{0.47}$As recessed cap layer.

<table>
<thead>
<tr>
<th>VMBE2100</th>
<th>XMBE131</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Cap) In$<em>{0.53}$Ga$</em>{0.47}$As 50 Å</td>
<td>(Cap) In$<em>{0.53}$Ga$</em>{0.47}$As 50 Å</td>
</tr>
<tr>
<td>(Barrier) In$<em>{0.30}$Al$</em>{0.70}$As 200Å</td>
<td>(Barrier) In$<em>{0.52}$Al$</em>{0.48}$As 150Å</td>
</tr>
<tr>
<td>δ-doped</td>
<td>δ-doped</td>
</tr>
<tr>
<td>(Spacer) In$<em>{0.30}$Al$</em>{0.70}$As 100Å</td>
<td>(Spacer) In$<em>{0.52}$Al$</em>{0.48}$As 100Å</td>
</tr>
<tr>
<td>(Channel) In$<em>{0.70}$Al$</em>{0.30}$As 160Å</td>
<td>(Channel) In$<em>{0.70}$Al$</em>{0.30}$As 160Å</td>
</tr>
<tr>
<td>(Buffer) In$<em>{0.52}$Al$</em>{0.48}$As 4500Å</td>
<td>(Spacer1) In$<em>{0.52}$Al$</em>{0.48}$As 100Å</td>
</tr>
<tr>
<td>δ-doped</td>
<td></td>
</tr>
<tr>
<td>(Buffer) In$<em>{0.52}$Al$</em>{0.48}$As 4500Å</td>
<td></td>
</tr>
<tr>
<td>(Substrate) InP Fe doped</td>
<td>(Substrate) InP Fe doped</td>
</tr>
</tbody>
</table>
The strained Schottky layer offers the advantage of an increase in the band gap and raise the Schottky barrier height, which reduces the gate leakage tremendously as will be shown later.

Figure 4.2 Schematic view of 0.25μm InGaAs/InAlAs/InP pHEMT XMBE131 with Pd/Ti/Au gate scheme as compared to the Ti/Au gate metallisation (Adapted from [98])

Figure 4.2 illustrates the pHEMT sample XMBE131 schematic. The strained channel In$_{0.7}$Ga$_{0.3}$As/In$_{0.52}$Ga$_{0.48}$As pHEMT device is fabricated with both Pd/Ti/Au gate metallisation scheme with conventional thermal evaporation. Kawa et al.[99] showed that the combination of the gate metallisation and the band-gap engineering results in better performance over device reported in [100],[101]. Compared to the pHEMT sample VMBE2100; the XMBE131 sample device has a double delta-doped layer and thin gate-to-channel distance of approximately 25 nm.
The Hall measurement data at 300 K and 77 K for all epitaxial layers is presented in Table 4.1. From the table, the sheet carrier concentration is higher in VMBE2100 and XMBE131, as a consequence of better carrier confinement in both epitaxial layers. It is obvious that the carrier confinement in VMBE2100 is accomplished by using a deeper quantum well, resulting from the wider bandgap material at the schottky and spacer layer. In the case of XMBE131, the carrier confinement is achieved by adapting the almost square-shaped quantum well, resulting from the double δ-doped structures.

Table 4.1 Hall measurement data at 300 K (room temperature) and 77 K for VMBE2100 and XMBE131 pHEMT device

<table>
<thead>
<tr>
<th>Sample</th>
<th>VMBE 2100</th>
<th>XMBE131</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sheet Carrier Concentration ($n_s$) at RT / 77K (x10^{12} cm^{-2})</td>
<td>2.50 / 2.60</td>
<td>2.40 / 2.50</td>
</tr>
<tr>
<td>Hall Mobility ($\mu_n$) at RT / 77K (cm²/V.s)</td>
<td>12,982 / 46,390</td>
<td>13,896 / 47,829</td>
</tr>
</tbody>
</table>

The carrier mobilities shown in Table 4.1 are comparable with each other for the two structures. This is primarily due to the use of the same highly strained In_{0.7}Ga_{0.3}As in the channel material. Referring back to Figure 4.2, the carriers in the 2DEG are separated by the same spacer thickness (100Å) in all epitaxial structures. Therefore the columbic interaction between the electrons and ionised donor atoms at the δ-doped layer are almost the same, and consequently comparable carrier mobilities are recorded in all epitaxial layers.

Investigation of the advantages of each epitaxial layer, in terms of the variation of barrier height, carrier concentration and carrier confinement were completed by the fabrication of transistors with a range of device widths. Several devices with multiple gate fingers and with gate length of 1 µm (L_G = 1 µm) were fabricated on VMBE2100 epitaxial layers, whereas submicron devices with L_G =0.25 µm were fabricated using the XMBE131 epitaxial layer. The devices’ DC and RF characteristics were then modelled, prior to their use in the Low Noise Amplifier (LNA) designs.
4.3 Mesh Definition for Device

Due to the assumption of ideal boundary conditions in this model, there are too large errors for a quantitative evaluation of the HEMT structures. For a more accurate model, the surface states in the gate recess area which affect the electric field distribution have to be considered carefully, and several simulation iterations are required to obtain good agreement with experimental data. Usually, the model parameters have to be adjusted by fitting factors [47,48,60] to find a compromise for the DC and RF behaviour. Fitting of material parameters has to agree with literature data that frequently show large variations.

In the modelling, the fabricated sample devices were defined by a virtual 2D structure whose electro-physical properties are discretized onto a nonuniform mesh of nodes. The 2D ATLAS simulations have a maximum node limit of 100,000 for any modelled device structure. The total nodes created using the mesh statement are 8732 grid points with 17082 triangles. Figure 4.3 shows the mesh nodes created for the pHEMT device structure.
Figure 4.3 Device Mesh for pHEMT structure which defined with non-cylindrical mesh for sample (a) VMBE2100 and (b) XMBE131

4.4 Two Dimensional Device Structure

In the 2D device simulations, the information about epitaxial layers, i.e., material composition, layer sequence and thickness are defined using the REGION statement. The interface of the InGaAs and InAlAs layers is zoomed to clearly visualize the doping concentration which is displayed by the Tony plot visualization window, as shown in Figure 4.5. The initial guess for parameter values is generated by ATLAS by solving a zero bias condition based on the doping profile in the device. From the virtual 2D structure in equilibrium, the thickness of each layer was examined as to make sure an accurate band energy diagram information is created. This step is essential before the DC and RF simulations is performed at other biasing voltage. The XMBE131 pHEMT is a two finger device with 50 μm gate width, 250nm gate length and 3μm source to drain separation (with gate is equally spaced between them). The source and drain contact for both structures are defined further down to the channel layer as to facilitate the electron conduction in the device structure [60].
Figure 4.4 Schematic device structure for VMBE2100 showing epitaxial layers (size not to scale)

Figure 4.5 Schematic device structure for XMBE131 epitaxial layers (size not to scale)
4.5 Band Diagram and 2DEG in Physical Modelling

A vertical cut line drawn across the structure of the device in Figure 4.5 and Figure 4.5 gives all the parameters at this position so that the required ones can be selected. In this way the conduction band diagram which represents the quantum well is obtained. The VMBE2100 and XMBE131 epitaxial layer from Figure 4.1 are simulated with ATLAS Silvaco at 0 V gate biasing and the band diagrams are shown in Figure 4.6 and Figure 4.7 respectively. The calculation of band diagram and electron charge distribution in ATLAS Silvaco is primarily affected by the material parameters, i.e., the electron affinities, energy band-gap, contact work-function for the gate electrode and permittivity. Other important parameters are the dielectric constant, electron and hole effective mass, and conduction band discontinuity between heterojunctions. All these parameters were simulated under thermal equilibrium and varying biasing conditions.

![Energy band diagram](image)

Figure 4.6 Energy band diagram (at thermal equilibrium) for VMBE2100 epitaxial layer simulated with ATLAS Silvaco
The double δ-doped structures is adopted to enhance the carrier confinement in the quantum well [103], and additionally reduced the gate leakage to compensate for the thinner gate to channel thickness particularly in the submicrometer gate length device. It could be observed from the band energy diagram of both structures that the quantum well drops to approximately –0.1 eV energy level to accommodate electron accumulation. The pHEMT’s characteristic in the quantum well reduces electron scattering and increases electron mobility. The energy band diagram at equilibrium gives information about Schottky barrier height, depth of the potential well formed due to the heterojunction in the channel and extent of band bending in the supply and spacer layers due to heavy doping in the δ-doped layer.

The epitaxial layer structures for all the device under test have a large band gap discontinuity at both ends of the channel. This creates a potential well for carrier confinement in the channel where electrons are free to move in parallel to the plane of heterojunctions. Hence, a 2DEG layer with very high electron mobility is established because electrons from the δ-doped layer diffuse into the channel and accumulated in the 2DEG. Figure 4.8 visualises the single- and double δ-doping concentration and the sheet density formation in the 2DEG for VMBE2100 and
Knowing the behavior of the 2DEG density as a function of the gate voltage, the 2D electron mobility as a function of the gate voltage along the channel can be obtained [79]. The simulated sheet carrier concentration (2DEG density) is adjusted to match the actual experimental values, which is \( \sim 2.5 \times 10^{12} \text{ cm}^2 \). Essentially, this will facilitate the carrier transport and charge control calculations for an accurate prediction of the pHEMT device characteristics and performance.

The heavily doped pseudomorphic In_{0.70}Ga_{0.3}As channel exhibits very good transport properties and the \( \Delta E_C \) with the In_{0.52}Al_{0.48}As is pretty high \( \sim 0.6 \text{ eV} \). Due to the lattice constant difference in these materials, it could be solved with the growth of a very thin pseudomorphic layer so that the lattice strain can be accommodated without deteriorating the carrier transport properties. The undoped In_{0.52}Al_{0.48}As layer acts as a barrier. The cap layer is an undoped In_{0.53}Ga_{0.48}As which can support a good ohmic contact for the source and drain. They are removed in the gate area to allow the gate Schottky contact. Figure 4.9 shows the band diagram and sheet carrier concentration at different biasing voltage (\( V_{gs} \) at \(-0.12 \text{ V}, -0.48 \text{V} \) and \(-1.08 \text{ V} \)). The relationship for the sheet carrier density, \( n_s \) with the biasing voltage can be explained.
from Equation 4.1, where $\varepsilon_r$ is the relative permittivity, $\varepsilon_0$ indicates permittivity of space and $d^*$ is the distance of metal from delta-doped layer.

$$n_S = \frac{\varepsilon_r \varepsilon_0}{qd^*} (V_{GS} - V_{TH})$$  \hspace{1cm} \text{Equation 4.1}

![Figure 4.9 (a) Sheet concentration (2DEG) and (b) Band diagram simulated at different biasing voltage (for VMBE2100 structure)](image-url)
4.6 Modeling DC Characteristics

Once the model was complete and analysed, a subroutine in ATLAS was created to generate the I-V curves, in which each of the biasing points are defined. The data extracted from the device model were imported to TONYPLOT for analysis and comparison. The simulation of the two-dimensional device model is performed with the same DC parameters that were utilized during the device measurements. The experimental DC characteristics of the VMBE2100 and XMBE131 pHEMT device; the leakage current, on-state current, threshold voltage, I-V characteristics and the transconductance are presented in Figure 4.10 and Figure 4.11 respectively. These data were used to validate the modelled device.

(a)

(b)
Figure 4.10 pHEMT sample VMBE2100 (1 μm gate length) characteristics
(a) Normalized current-voltage characteristics (b) Threshold Voltage, $V_{TH}$, (c) Normalized transconductance, $g_m$ with $g_m=940$ mS/mm at $V_{DS}=2$ V and (d) on-state leakage current where $V_{DS} = 0$ to 2 V with 250 mV steps.
Figure (a): Id-Vd characteristic for XMBE131 Pd Gate

Figure (b): Threshold Voltage for XMBE131, Pd-250nm

Figure (c): Transconductance for XMBE131, Pd-250nm
Figure 4.11 pHEMT sample XMBE131, 0.25μm gate length (Pd gate metallisation)
(a) Normalized current-voltage characteristics with maximum drain current, (b) Threshold Voltage, $V_{TH}$, (c) Normalized transconductance, $g_m$ with $g_m=940\, \text{mS/mm}$ at $V_{DS}=2\, \text{V}$, (d) on-state leakage current where $V_{DS}=0$ to $2\, \text{V}$ with $250\, \text{mV}$ steps and (e) off-state leakage current
4.6.1 Ideality factor and gate leakage current

The upper gate region of a HEMT transistor behaves as a Schottky diode. The Schottky barrier height can be determined experimentally from the I-V characteristics, photoelectric and capacitance measurements [104]. The Schottky diode measurement is normally carried out after the formation of Schottky contact, which is vital for monitoring of the gate quality. In this process, a gate voltage, $V$ applied across the gate and source terminals and the change of gate current, $I$ is recorded. Depending on the polarity of gate voltage, the Schottky diode behaviour can be divided into forward ($V>0$) and reverse ($V<0$) bias regions. The Schottky barrier height ($\Phi_B$), ideality factor ($n$) and series resistance ($r_s$) can be extracted from the log scale plot of the forward region, as shown in Figure 4.12.

![Figure 4.12 Typical Schottky diode forward current characteristic of InP pHEMT](image)

The near-unity ideality factor indicates that a good Schottky diode interface exists, which shows that thermionic emission is the sole transport mechanism. For a baseline transistor, any discrepancies from unity shows that current flow is due to other transport mechanisms such as Thermionic-Field Emission (TFE) current. Starting from the base diode formula, the ideality factor ($n$) can be calculated using Equation 4.2 and Equation 4.3.
Where $I_s$ = saturation current for $V = 0$, $A$ = area of the Schottky diode contact, $A^*$ is the Richardson constant (material dependent, In$_{0.52}$Al$_{0.48}$As = 10.26 Acm$^{-2}$K$^{-2}$ [105]). The output current, $I$ (from Figure 4.21) will exhibit a linear behaviour in the log plot when the applied voltage ($V$) is $>3kT/q$. In the linear region, the output current is given by Equation 4.4 and it can be rearranged into Equation 4.3.

$$I = I_s \left( \frac{qV}{e^{\frac{qV}{nkT}}} - 1 \right) \quad \text{Equation 4.2}$$

$$I_s = AA^*T^2 \frac{q\Phi_B}{e^{\frac{q\Phi_B}{nkT}}} \quad \text{Equation 4.3}$$

The slope of the linear region and thus the ideality factor ($n$) are given by Equation 4.6 and Equation 4.7:

$$\text{slope} = \frac{\Delta \ln I}{\Delta V} = \frac{qV}{nkT} \quad \text{Equation 4.6}$$

$$n = \frac{\Delta V}{\Delta \ln I} \frac{qV}{kT} = \frac{qV}{kT} \frac{1}{\text{slope}} \quad \text{Equation 4.7}$$
Figure 4.13 Schottky diode forward current characteristic of XMBE131 pHEMT modelled with different work function value.

The Schottky diode characteristics for XMBE131 pHEMT sample is shown in Figure 4.13 and the ideality factor for this device which was calculated based on the experimental data and simulation with various work function value is tabulated in Table 4.2. The ideality factor and the off-state leakage current for the modelled device with the highest applied metal work function value (for Palladium at WF=5.25) contributes to a good agreement as compared with calculated data from the forward bias measurement. The other pHEMT structure which was modelled with 4.85 and 5.10 metal work function results in a lower off-state leakage current than that of the measured device by approximately an order of magnitude.

Table 4.2 Ideality factor (n) measurement data vs. modelled with various metal work function

<table>
<thead>
<tr>
<th>Device (XMBE131, 2x50µm)</th>
<th>Ideality factor, n</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pd-250nm (measured)</td>
<td>1.47</td>
</tr>
<tr>
<td>Pd-250nm (modelled, WF=4.85)</td>
<td>1.38</td>
</tr>
<tr>
<td>Pd-250nm (modelled, WF=5.10)</td>
<td>1.33</td>
</tr>
<tr>
<td>Pd-250nm (modelled, WF=5.25)</td>
<td>1.26</td>
</tr>
</tbody>
</table>
Although the Schottky barrier $\Phi_B$ used in the model is correct and corroborates with the InAlAs, the Schottky diode model for tunnelling and thermionic emission may be improved. Deep level traps are the important parameter to be probed in the gate leakage current study. Similarly, the surface trap level also plays a considerable role because the surface of the channel between the gate and drain/source of the pHEMT device is ungated. It has been considered as a boundary of the active region of the device. These access regions can make a significant contribution to the total source–drain resistance. The gate bias varies the trapping/detrapping of surface states in the ungated region [106] as discussed earlier in Chapter 3.

During the device breakdown characterization, electron-hole pairs are generated in the high field area related to impact ionization [107]. While the generated electrons move towards the drain contact being part of the drain current $I_D$, holes contribute to the gate current, $I_G$ and source current, $I_S$. Holes may recombine with incoming channel electrons or are drawn-off to the source or gate contact.

### 4.6.2 Current-Voltage Characteristics

The VMBE2100 and XMBE131 pHEMT device was simulated under matching gate biases and I-V curves are presented to show a general correspondence between modelled and measured results. The drain current, $I_{ds}$ and gate current,$I_g$ are calculated at each bias point. Numerous combinations of electron mobility and velocity saturation were tried to improve model accuracy. A Gummel iteration is used to improve initial guess for the Newton solution, however the calculations performed are slower than Newton. Both GUMMEL and NEWTON are applied in the METHOD statement as the iteration because convergence is slow [80].

The behaviour of $I_{ds}$ with varying bias conditions is primarily dependent on the carrier mobility and concentration in the channel, as given by the current continuity equations [33]. The I-V curve simulated with mobility model is shown in Figure 4.14. The drain current does not saturate when the high field mobility model is not applied because the carrier velocity increases with increasing lateral field. The gradient of drain current with drain voltage, however, decreases at certain $V_{ds}$ as the carriers in the channel are depleted.
However, at higher electric fields, the drain current saturates at much earlier value of $V_{ds}$, compared to the case where the field dependent mobility model is not applied. This is because the carrier mobility reduces considerably at high electric fields and this effectively saturates the current through the channel [108].

![Figure 4.14 Simulated I-V Curve (with and without) Mobility Model for VMBE2100](image)

Introducing traps in the barrier and buffer layers [109] leads to the capture of electrons in these layers that would have otherwise been transported to the channel. Thus the carrier concentration in the channel is considerably reduced. For the purpose of simulation, the donor density in the $\delta$-doped layer is therefore increased to overcome the lack of electrons in the channel at thermal equilibrium. This is achieved by either increasing the Gaussian width or by increasing the doping concentration ($N_d$). Hence, this will effectively increase the supplied donors in this region. Fitting in the linear region of the I-V characteristics is done by defining the contact resistance, $R_S$ and $R_D$ in the 2D device structure. The contact resistance for XMBE131 pHEMT structure was optimised at 600 $\Omega$.$\mu$m which results of 0.12 $\Omega$.mm for the entire device width.

The captured electrons in trapping mechanism reduce the sheet electron density in the 2DEG channel, which in turn leads to a reduction in the drain current density. Higher trap density results in lower drain current as can be seen in Figure 4.18. At $V_{GS}$=0 V, the modelled current is lower than the maximum measured current.
Figure 4.15 Current-Voltage Characteristics for normalised 4x200μm VMBE2100 pHEMT when only trapping mechanism activated, N_T=2e17cm^3 (without impact ionisation)

The kink effect is visible in the measured results of VMBE2100 for V_GS=-1.02 V and -1.36 V. The V_GS is biased from 0V to -1.2V with 0.12V step voltage. Figure 4.16 is the I-V curve and the threshold voltage plot is given in Figure 4.17.

Figure 4.16 Modelled vs Measured I-V Characteristic for VMBE2100
The results presented in Figure 4.16 and Figure 4.17 shows reasonable agreement between the model and measured data by employing TRAP and IMPACT ionization statement in the models. The surface traps was activated with the activation energy, \( E_a = 0.34 \) eV with respect to conduction band minimum, \( E_a = 0.76 \) eV (for deep level traps), electron and hole capture cross section, \( \sigma_e = \sigma_p = 2 \times 10^{-17} \) cm\(^2\) and trap concentration, \( N_T = 2 \times 10^{16} \) cm\(^{-3}\) [86][110].
Based on the modelling that has been performed for the VMBE2100 1µm device structure, the knowledge was used to improve the physical modelling of the XMBE131 pHEMT. The optimised 2D physical modelling for this structure resulted in a very good agreement in the I-V characteristics as compared to the experimental data which can be observed from Figure 4.18. The maximum drain current for modelled device is slightly higher compared to the experimental one at $V_{GS}=0.6$ V, whilst higher by about ~0.02 mA at $V_{GS}=0$V. However, the fitting of drain current at other bias points is excellent (overlapped between measured and modelled) and pinched completely at $V_{GS}=-0.2$V.

4.6.3 **Threshold Voltage and Transconductance**

The device threshold voltage, $V_T$ can be approximately determined by plotting $I_{ds}$ against $V_{GS}$ at constant $V_{DS}$. The threshold voltage is taken at the point where a straight line drawn with the drain current intersects the gate-source voltage axis, as illustrated in Figure 4.10 (b) where the simulated $I_{DS}$ is plotted against $V_{GS}$. It shows that the carrier mobility model does not affect the device threshold voltage. In other words, the threshold voltage is not a function of carrier mobility, but rather depends upon the ionized doping concentration and other regional and band parameters as given by Equation 2.14 in Chapter2. Results presented in Figure 4.19 is the threshold voltage biased at $V_{DS}=1$V. From Figure 4.19, the I-V curve in the modelled structure result is in very good agreement with the experimental data. Hence, the extracted threshold voltage, $V_T$ from the simulations is approximately -0.2V although the maximum current slightly deviates from the measured $I_{DS}$.

The threshold voltage of the modelled device shifts with the new definition of doping concentration in the δ-doped region (from 7.4Å to 8.0Å) to compensate for the reduction of electrons in the channel due to the trapping mechanism. This rise in the maximum current (which also correspond to threshold voltage shift) is due to the fact that carriers (electrons) captured by the traps at thermal equilibrium are released on the application of bias. These released electrons become available for conduction in the channel, which increases the net carrier density in the channel, thus requiring higher voltages to deplete the carriers.
The transconductance performance from the physical modelling is plotted at the biasing voltage, \( V_{DS}=1V \). The results for both modelled and measured \( g_m \) are shown in Figure 4.22. The maximum transconductance (from modelled structure) is slightly higher (but less than 10\% ) of the results from the experimental data. The higher \( g_m \) value is expected due to the higher drain current obtained from the I-V characteristics.

Figure 4.19 \( I_D - V_G \) at \( V_{DS}=1V \) for normalised 2x50\( \mu m \) XMBE131pHEMT (optimised modelled vs. measured)

Figure 4.20 Transconductance (meas. Vs modelled) for normalised 2x50\( \mu m \) XMBE131pHEMT at \( V_{ds}=1V \)
4.6.4 Modelling Impact Ionization in ATLAS

The impact ionization model is implemented due to the kink anomalies which are observed at higher \( V_{GS} \) biasing point (\( V_{GS} > 0V \)) in the I-V characteristics of VMBE2100 and XMBE131 pHEMT device (from experimental data) depicted in Figure 4.10 and Figure 4.11. In this work, Selberherr’s model for impact ionization has been used as a guideline [78][80]. This model is enabled by defining the parameter 'SELB' in the 'IMPACT' statement. The ionization rates for carrier generation are computed using analogous expressions for electrons and holes as explained in Chapter 3 and the relationship is given by Equation 3.28. The impact ionization parameter from Suemitsu et.al [45] is referred and given in Table 4.3.

### Table 4.3 Impact Ionization Parameters Applied for the Modelling [45]

<table>
<thead>
<tr>
<th>Parameters</th>
<th>[unit]</th>
<th>InGaAs</th>
<th>InAlAs</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Electron</td>
<td>Hole</td>
<td>Electron</td>
</tr>
<tr>
<td>Mobility, ( \mu )</td>
<td>[cm(^2)/Vs]</td>
<td>10000</td>
<td>100</td>
</tr>
<tr>
<td>Saturation velocity, ( V_{sat} )</td>
<td>[cm.s(^{-1})]</td>
<td>2.7x10(^7)</td>
<td>1x10(^7)</td>
</tr>
<tr>
<td>Ionization Parameters A</td>
<td>[cm.s(^{-1})]</td>
<td>6.9x10(^4)</td>
<td>1.2x10(^6)</td>
</tr>
<tr>
<td>Ionization Parameters B</td>
<td>[V.cm(^{-1})]</td>
<td>9.0x10(^5)</td>
<td>1.7x10(^6)</td>
</tr>
<tr>
<td>Energy relaxation time</td>
<td>[fs]</td>
<td>250</td>
<td>250</td>
</tr>
<tr>
<td>Recombination lifetime</td>
<td>[ns]</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

The impact ionization is mostly present towards the drain side of the gate, in the channel region, for higher magnitudes of drain-source voltage. The ionization rate is very low at \( V_{GS} = -1.2 \) V as the threshold condition is reached and the channel is depleted of carriers. The graphical illustration of the ionization rate for various bias points is given in Figure 4.21 (a) - (c).
Figure 4.21 2D Contour of Impact Ionisation rate in VMBE2100 Device Model:
(a) $V_{GS} = -0.12V$, (b) $V_{GS} = -0.72V$ and (c) $V_{GS} = -1.2V$
The ionization process results in generation of carriers that increases the carrier concentration in the channel. Without impact ionization, the carriers deplete with the initial application of drain-source voltage and then saturate at a certain voltage. While in the presence of impact ionization, the carrier concentration in the channel increases with $V_{\text{DS}}$, after the initial carrier loss due to the carrier generation mechanism. The increasing carrier concentration gives rise to drain current that is reflected in the form of output conductance Figure 4.22 shows the drain current response for simulations with impact ionization.

![I-V Characteristic with Impact Ionization](image)

**Figure 4.22** I-V Characteristic with Impact Ionization

### 4.6.5 Kink Effect in Physical Modelling

The kink effect is due to a threshold voltage shift which increases due to hole pileup in the extrinsic source and ensuing charging of the surface. In the device simulations, the kink is reproduced by taking into account the impact ionization (i.i) and sufficient surface trap density of the device physics model [86]. The trap parameter values applied in the 2D device model development is described in Section 4.6.2. Under DC conditions, the kink arises as surface traps partially discharged by impact ionization generated holes which results in an increase in drain current. Due to the small band gap of InGaAs, these devices are very susceptible to suffer impact ionization processes, with the subsequent hole transport in the channel, both supposedly implicated in the kink effect.
At higher $V_{DS}$, holes generated by impact ionization tend to pile up in the channel under the source side of the gate due to the attracting potential caused by the surface charge at the recess and, mostly, by the gate potential. Due to this pile up of positive charge, the potential barrier controlling the current through the channel is lowered, so that the channel is further opened and $I_{DS}$ increases, leading to the well known kink effect in the I-V characteristics [60]. Kink anomalies mechanism can be visualised in Figure 4.23.

![Figure 4.23 Kink mechanism as explained by Somerville [38] (a) Simplified device cross-section used for the model. (b) Energy bands within the extrinsic source adjacent to the gate as a function of time. (c) Drain current characteristics as a function of time.](image)

At the $V_{DS}$ value for which channel impact ionization becomes significant, surface deep acceptors get discharged due to hole capture. This in turns reduces the depletion region under the ungated surfaces. The kink becomes smaller as the trap density ($N_T$) is reduced [86]. The hole pile-up which is generated by the impact ionization taken
place mainly on the drain side of the buffer. This leads to the reduction of the gate-induced channel depletion and results in a drain current enhancement. BG Vasallo et al [60] found that the generation of holes by impact ionization and their further recombination lead to fluctuations in the charge of the hole pile-up, which provoke an important increase in the drain current noise, even when the kink effect is hardly perceptible in the output characteristics. Figure 4.24 and Figure 4.25 illustrates the relation of $N_T$ with the kink anomalies at lower $V_{DS}$ region. In Figure 4.24 (b), the kink effect is clearly visible at lower drain voltage region (at $V_{GS}$=-0.36V). From the comparison of I-V characteristics in Figure 4.25 with different trap concentration, the kink current intensity ($\Delta I_{Kink}$) increases with defects concentration decreases [111].

![Graph showing I-V characteristics](image)
Figure 4.24 Kink Effect Anomalies in I-V Characteristics as a Function of Trap Density: (a) ∆I_{kink} is higher for high N_T [111] for AlGaN/GaN HEMT and (b) Simulated I-V characteristics with N_T=5x10^{17} cm^{-3}

Figure 4.25 The ∆I_{kink} analysis on I-V Characteristics with different trap N_T value
4.7 RF Modelling for pHEMT device

The RF modelling is performed for XMBE131 pHEMT. The unity current gain (h21) plot and the maximum frequency, \( f_{\text{max}} \) versus frequency for sample XMBE131 is illustrated in Figure 4.26 and Figure 4.27 respectively. Since \( f_T \) is inversely proportional to \( L_G \), the short gate length contributes to the high cutoff frequency of 90GHz (extrapolated). The modelled S-parameter performance for the gain S21 and reflection S12 plotted in Figure 4.28 also shows good agreement with the measured data. Hence, this device is a promising component for the LNA design at higher frequency as it will have a reduced noise figure (NF).

![Figure 4.26 Measured vs modelled cut-off frequency, \( f_T \) for XMBE131 pHEMT sample](image)

![Figure 4.27 Measured vs modelled maximum frequency, \( f_{\text{max}} \) for XMBE131 pHEMT sample](image)

123
To further improve the physical device model, following detailed theoretical studies or measurements can be addressed in future modelling:

a) Although the Schottky barrier $\Phi_B$ used in the model is correct and corroborates with the InAlAs, the Schottky diode model for tunnelling and thermionic emission may be improved.

b) Only bulk trap at the supply, spacer and buffer have been employed in the model and successfully generate the output log file. In this model, the impact
Ionization model parameters are defined and optimised using fitting mechanism and trial and error.

c) The Drift Diffusion model may be replaced by more accurate Energy balance transport model which takes into account the velocity overshoot and other non-local effects. Similarly Boltzmann’s approximation may be replaced by more accurate Fermi-Dirac models [80] [89].

d) The temperature dependent model should be included in the design. This is due to the material parameters and coefficients determining the device characteristics are highly sensitive to temperature variations. Thus the device performance varies significantly with changes in temperature.

4.8 Summary

In this chapter, a two-dimensional physical model for DC and RF simulations were presented and discussed. The preliminary work of the physical model was developed for VMBE2100 pHEMT sample with a 1 μm gate length and 4x200 μm device. This model is further extended for the double δ-delta doped XMBE131 pHEMT device with 0.25 μm gate length. The simulations have considered physical processes such as high field dependent mobility model, carrier generation and recombination, deep level trap and impact ionization. Appropriate models for Shockley-Read-Hall, Auger and direct recombination were included in the simulation. Comparisons between the modelled and measured devices for each epitaxial layer were also presented. The 0.25 μm gate length InGaAs/InAlAs XMBE131 pHEMT device has shown very high cut-off frequency while keeping a very low NF_{min} value.

The simulated I–V characteristics as well as transfer characteristics are shown to be in agreement with experimental data. The key features, such as the threshold voltage (V_T), transconductance (g_m) and drain current in the saturation region are reproduced and in a good agreement with the experimental data. In the last section, the simulation results achieved from the modelled device are compared and validated with the experimental data. By having a good agreement between modelled and experimental results for both 1 micron and submicron device; it attests that the 2D physical pHEMT model developed is accurate. With some improvement, it could be used for further investigation such as gate scaling and circuit analysis.
5 CHAPTER 5

EMPIRICAL MODELLING OF SUB-MICROMETER
In\textsubscript{0.7}Ga\textsubscript{0.3}As/In\textsubscript{0.52}Al\textsubscript{0.48}As pHEMTs

5.1 Introduction
While the fabrication process is the most important aspect of device production, device modelling becomes essential in understanding the semiconductor device physics, as well as device fabrication process and characterization. In addition, device modelling is greatly important in analysing device output characteristics and adequate prediction of device performance. Modelling allows the designer to understand the semiconductor behaviours and properties by using computational systems so that it accurately reflects device behaviour. In addition, accurate modelling is required to predict the linear and nonlinear behaviour of the device and microwave circuits such as in Low Noise Amplifiers (LNA) [112]. By cutting the iteration number of fabrication for device characterization, device modelling reduces the time and cost required for developing a specific device or circuit. In the previous chapter, physical device modelling was performed using 2-dimensional ATLAS Silvaco [80] device simulator. The empirical modelling for the pHEMT sample devices which established in ADS software will be explained in detail in this chapter. The extraction of linear and nonlinear parameters from the small signal and large signal pHEMT equivalent model will be presented. The optimized pHEMT model is use in the MMIC LNA circuit design.

5.2 Empirical Device Modelling
Empirical Device Models (EDMs) simulate the external behaviour of devices with equivalent circuits to accurately reflect the device behaviour under bias [113]. Practically, it is obtained by optimizing the component values to closely match the measured S-parameters for the device. The S-parameter models for the transistors’ two-port network can be found in APPENDIX A. Nowadays, empirical modelling
is widely used in device performance analysis such as noise, gain, cut-off frequency, and also in designing microwave circuits. In the small signal model, several linear and non-linear elements are connected in an organized and established topology such that the performance of the equivalent circuit matches the device output characteristic [68,69]. The parasitic element produces degradation in the transistor AC performance [115].

5.3 HEMT Small Signal Equivalent Circuit

The small signal model for HEMTs links the measured S-parameters with the electrical processes occurring within the device. Each component of the model provides an approximation to some aspect of the device physics. Figure 5.1 illustrates the conventional HEMT structure with its equivalent small signal model. This model is significant to evaluate and analyse device performance, such as gain, noise, bandwidth, stability at given biasing point, etc. The topology assumed for building an equivalent circuit model of the device, along with physical correlation to the device, provides an excellent match over a wide frequency range.

![Figure 5.1 Physical origin of the HEMT small signal equivalent circuit model [110]](image)

Using ICCAP standard computer-aided design (CAD) tools, the linear small signal models (intrinsic and extrinsic) parameters were extracted from the measured S-
parameter data. The intrinsic model parameters were obtained from hot (active) device bias point, while the extrinsic elements were extracted from the cold (pinched) device measurement [47]. The final element values for linear models were determined by optimisation of the initial value to accurately fit the measured data.

5.4 Small Signal Model Parameters

The small signal model or linear model of a HEMT consists of passive devices that can be categorized into intrinsic elements and extrinsic elements. These small signal models give advantages to the IC designer to accurately measure S-parameters of the device. The small signal model presented in this dissertation is the most commonly used and followed technique developed by Dambrine et.al [18]. A standard small signal equivalent circuit for HEMT is given in Figure 5.2. Elements in the green box are extrinsic elements (cold/pinched) which are independent of biasing conditions, while the bias dependant intrinsic (hot) elements are grouped in the red box.

![Figure 5.2 Standard form of HEMT small signal equivalent circuit [18]](image)

Figure 5.2 represents a standard form of the same small signal model with seven intrinsic elements ($G_m$, $R_i$, $\tau$, $R_{ds}$, $C_{ds}$, $C_{gs}$, and $C_{gd}$) and eight extrinsic elements ($R_S$, $C_{pg}$, $C_{gd}$, $C_{gs}$, $R_d$, $L_d$, $R_g$, $C_{pd}$, $R_{ds}$, $C_{ds}$, $G_{m}$, $R_i$, $\tau$, $R_{ds}$, $C_{ds}$, $C_{gs}$, and $C_{gd}$).
Intrinsic parameters are bias dependent and extrinsic or parasitic parameters are bias independent. The parasitic parameters account for the ohmic contacts as well as the transistor gate, drain and source pad. The extrinsic parameters for small signal equivalent models can be listed as follows:

a) **Parasitic Resistances:** $R_s$ and $R_d$ are the series source and drain resistances respectively, and extracted by considering the depletion region effect below the gate under forward bias. The resistances exist due to the contact resistance of the ohmic contacts between the metal electrodes and the cap layer and also include any bulk resistance to the active channel. $R_g$ is the gate resistance which results from the metallisation of the Schottky contact at the gate terminal.

b) **Parasitic Inductances:** $L_s, L_d$ and $L_g$ are the source, drain and gate inductances respectively. These inductances result from the metallisation of the contacts with the device surface. The gate inductance, $L_g$, is usually large for short gate length devices.

c) **Capacitances:** The gate-source capacitance, $C_{gs}$ and gate-drain capacitance, $C_{gd}$ represent the variation of the depletion charge with respect to the gate-source and gate-drain voltages. The drain-source capacitance, $C_{ds}$, arises because of the capacitive effect between the drain and source electrodes.

d) **Input Channel Resistance:** $R_i$ is the input channel resistance that exists under the gate, between the source and the channel. Normally, the input channel resistance value will have a direct effect on the input reflection coefficient, $S_{11}$ of the device.

e) **Transconductance:** The transconductance, $g_m$, is defined as the change of $I_{ds}$ over the change of $V_{gs}$. It is also a measure of how the input voltage is successfully converted to the output current as given by

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}}$$

Equation 5.1
f) **Transconductance Delay:** \( \tau \), is the response time for the transconductance, \( g_m \), to the changes in gate voltage or it can be explained as the time taken for charges to re-arrange themselves upon the variation of the gate voltage.

\[ \text{g) Bond Pad Capacitances:} \text{ The bond pad capacitance at the gate, } C_{pg} \text{ and the bond pad capacitance at the drain, } C_{pd} \text{ are required for probe measurement systems.} \]

### 5.4.1 Extrinsic Elements Extraction

The Eight extrinsic elements (\( L_g, L_d, L_s, C_{pg}, C_{pd}, R_g, R_s, R_d \)) from the measured cold FET S-parameters are extracted. The cold FET measurements are taken at zero drain bias, \( V_{ds}=0 \text{V} \) and gate voltage below the device pinch-off state, i.e. \( V_{gs}<V_p \). Under this bias conditions, the equivalent circuit model for the device is as shown in Figure 5.3 [18].

![Figure 5.3 Equivalent Circuit Model for FET Cold Bias Condition [18]](image)

The impedance matrix for the cold FET equivalent circuit model is given by:

\[
Z_e = \begin{bmatrix}
R_g + R_s + j [ \omega L_s + L_r ] + [ \frac{1}{\omega C_{ab}} ] & R_s + j [ \omega L_s + \frac{1}{\omega C_a} ] \\
R_s + j [ \omega L_s + \frac{1}{\omega C_b} ] & R_d + R_s + j [ \omega ( L_s + L_r ) + \frac{1}{\omega C_{ab}} ]
\end{bmatrix}
\]

Equation 5.2

where

\[
C_{ab}^{-1} = C_a^{-1} + C_b^{-1}
\]

Equation 5.3
\[ C_{bc}^{-1} = C_b^{-1} + C_c^{-1} \]  

Equation 5.4

The extrinsic equations are expressed as follow,

\[ R_x = \Re (Z_{e11} - Z_{e12}) \]  

Equation 5.5

\[ R_x = \Re (Z_{e11}) \]  

Equation 5.6

\[ R_d = \Re (Z_{e22} - Z_{e12}) \]  

Equation 5.7

\[ \omega \cdot \Im (Z_{e11}) = \omega^2 L_x + L_x - \frac{1}{C_{ab}} \]  

Equation 5.8

\[ \omega \cdot \Im (Z_{e12}) = \omega^2 L_x - \frac{1}{C_b} \]  

Equation 5.9

\[ \omega \cdot \Im (Z_{e22}) = \omega^2 L_x + L_x - \frac{1}{C_{bc}} \]  

Equation 5.10

where \( \Re (\quad) \) is the real part and \( \Im (\quad) \) is the imaginary part. The parasitic resistances, \( R_x, R_g, \) and \( R_d, \) from Equation 5.5 to Equation 5.7 can be solved using the measured value of \( Z \)-parameters from the cold/pinched device. Taking the simplest equation i.e. eq. (3.8), the slope of the line will give the \( L_x \) value while the y-intercept of the line gives the \( C_b \) value. By knowing \( L_x \) value, the values for \( L_d \) and \( L_g \) will then easily be obtained. The bond pad capacitances, \( C_{pg} \) and \( C_{pd}, \) from the Equation 5.11 to Equation 5.13 can be directly extracted because of the fact that the value of \( C_b \) is already known from the previous calculation.

\[ \Im (Y_{11}) = j \omega \left( C_{pg} + 2 C_b \right) \]  

Equation 5.11

\[ \Im (Y_{12}) = \Im (Y_{21}) = - j \omega C_b \]  

Equation 5.12

\[ \Im (Y_{22}) = j \omega \left( C_{pd} + C_b \right) \]  

Equation 5.13

5.4.2 Intrinsic Elements Extraction

After extracting the eight extrinsic elements from the cold (pinched) device, the next procedure in small signal parameter extraction is to extract the seven intrinsic
elements from the measured S-parameter. The intrinsic elements can be modelled using $Y_{\text{int}}$ as follows:

$$Z_{\text{i}} = \begin{bmatrix} R_x + R_y + j \omega \left( L_x + L_y \right) + \frac{1}{\omega C_{ss}} & R_z + j \omega L_z + \frac{1}{\omega C_{ss}} \\ R_x + j \omega L_x + \frac{1}{\omega C_{ss}} & R_y + R_z + j \omega \left( L_y + L_z \right) + \frac{1}{\omega C_{ss}} \end{bmatrix}$$  \hspace{1cm} \text{Equation 5.14}$$

where

$$D = 1 + \omega^2 C_{gs}^2 R_i^2$$  \hspace{1cm} \text{Equation 5.15}$$

The expressions for all seven intrinsic parameters are expressed as [14, 20]:

$$C_{gs} = \frac{\Im \left( Y_{\text{int}21} \right)}{\omega}$$  \hspace{1cm} \text{Equation 5.16}$$

$$C_{gs} = \frac{\Im \left( Y_{\text{int}11} \right) - \omega C_{gd}}{\omega} \left[ 1 + \frac{\left\{ \Re \left( Y_{\text{int}11} \right) \right\}^2}{\left\{ \Im \left( Y_{\text{int}11} \right) - \omega C_{gd} \right\}^2} \right]$$  \hspace{1cm} \text{Equation 5.17}$$

$$R_i = \frac{\Re \left( Y_{\text{int}11} \right)}{\left\{ \Im \left( Y_{\text{int}11} \right) - \omega C_{gd} \right\}^2 + \left\{ \Re \left( Y_{\text{int}11} \right) \right\}^2}$$  \hspace{1cm} \text{Equation 5.18}$$

$$g_m = \sqrt{\left\{ \Re \left( Y_{\text{int}21} \right) \right\}^2 + \left\{ \Im \left( Y_{\text{int}21} \right) + \omega C_{gs} \right\}^2 D}$$  \hspace{1cm} \text{Equation 5.19}$$

$$\tau = \frac{1}{\omega} \arcsin \left( \frac{-\omega C_{gd} - \Im \left( Y_{\text{int}21} \right) - \Re \left( Y_{\text{int}21} \right) \omega C_{gs} R_i}{g_m} \right)$$  \hspace{1cm} \text{Equation 5.20}$$

$$C_{ds} = \frac{\Im \left( Y_{\text{int}22} \right) - \omega C_{gd}}{\omega}$$  \hspace{1cm} \text{Equation 5.21}$$

$$R_{ds} = \frac{1}{\Re \left( Y_{\text{int}22} \right)}$$  \hspace{1cm} \text{Equation 5.22}$$

All the equations for intrinsic and extrinsic parameter extraction explained in this work have been programmed in Advance Design System (ADS) software tools from
Agilent. This can save a lot of time as well as reducing the possibility of errors in manual calculations.

After extracting the eight extrinsic elements of the cold (pinched) device, the next procedure in linear parameter extraction is to extract the seven intrinsic elements from the measured S-parameters. According to Dambrine, the determination of the intrinsic admittance matrix (Yint) can be carried out using simple matrix manipulations if the extrinsic elements are known. The extraction procedure carried out by Dambrine et al. is listed below [18]:

i. Measurement of the S-parameters of the extrinsic device

ii. Transformation of the S-parameters to Z parameters and subtraction of \( L_g \) and \( L_d \), which are series elements

iii. Transformation of Z to Y parameters and subtraction of \( C_{pg} \) and \( C_{pd} \) which are in parallel

iv. Transformation of Y to Z parameters and subtraction of \( R_g \), \( R_s \), \( L_s \), and \( R_s \), which are in series

v. Transformation of Z to Y parameters which correspond to the desired matrix

Figure 5.4 shows the diagram for extracting intrinsic parameter as proposed by Dambrine et al. [18].
\[
\begin{bmatrix}
Z_{11} - j\omega L_g & Z_{12} \\
Z_{21} & Z_{22} - j\omega L_d
\end{bmatrix}
\]

\[
\begin{bmatrix}
Y_{11} - j\omega C_{pg} & Y_{12} \\
Y_{21} & Y_{22} - j\omega C_{pd}
\end{bmatrix}
\]

\[
\begin{bmatrix}
Z_{11} - R_s - R_g - j\omega L_s & Z_{12} - R_s - j\omega L_s \\
Z_{21} - R_s - j\omega L_s & Z_{22} - R_s - j\omega L_s
\end{bmatrix}
\]

\[(Y_{int}) = Z \rightarrow Y(Z_{int})\]

Figure 5.4 Method for extracting the device intrinsic Y matrix [105]

The transformation of the Z matrix to the Y matrix is given in APPENDIX B. The effects of extrinsic parameters are then subtracted from the measured hot (intrinsic) S-parameters to obtain the admittance \((Y_{int})\), written as:

\[
Y_{int} = \begin{bmatrix}
\frac{R_i^2 C_{gs}^2 \omega^2}{D} & \frac{j\omega}{D} \left( C_{gs} + C_{gd} \right) & -j\omega C_{gd} \\
g_m e^{-j\omega \tau} & \frac{g_{ds} + j\omega (C_{ds} + C_{gd})}{1 + j\omega R_i C_{gs}} - j\omega C_{gd} & g_{ds} + j\omega (C_{ds} + C_{gd})
\end{bmatrix}
\]

Equation 5.23
Where

\[ D = 1 + \omega^2 C_{gs}^2 R_i^2 \]  
Equation 5.24

The term \( \omega^2 C_{gs}^2 R_i^2 \) is less than 0.01 at frequencies below 5 GHz and hence \( D=1 \) [64].

The expressions for all seven intrinsic parameters are expressed as [64]:

\[ C_{gd} = Im(Y_{int21}) \]  
Equation 5.25

\[ C_{gs} = \frac{Im(Y_{int11}) - \omega C_{gd}}{\omega} \left( 1 + \frac{\{Re(Y_{int11})\}^2 - \omega C_{gd}}{\{Im(Y_{int11}) - \omega C_{gd}\}^2} \right) \]  
Equation 5.26

\[ R_i = \frac{Re(Y_{int11})}{\{Im(Y_{int11}) - \omega C_{gd}\}^2 + \{Re(Y_{int11})\}^2} \]  
Equation 5.27

\[ g_m = \sqrt{\{Re(Y_{int21})\}^2 + \{Im(Y_{int21}) + \omega C_{gd}\}^2} D \]  
Equation 5.28

\[ \tau = \frac{1}{\omega} \arcsin \left[ \frac{-\omega C_{gd} - Im(Y_{int21}) - Re(Y_{int21}) \omega C_{gs} R_i}{g_m} \right] \]  
Equation 5.29

\[ C_{ds} = \frac{Im(Y_{int22}) - \omega C_{gd}}{\omega} \]  
Equation 5.30

\[ R_{ds} = \frac{1}{Im(Y_{int22})} \]  
Equation 5.31

All of the equations for intrinsic and extrinsic parameter extraction explained in this work have been programmed in Advance Design System (ADS) software. This software reduces the possibility of errors in manual calculations. ADS also include an optimisation tool, in order to obtain the best performance of the linear model.
5.5 Large Signal Model for HEMTs

Large signal model (or also called nonlinear model) is used to predict and optimize the power performance of the device that cannot be obtained from the small signal model. An accurate nonlinear or large signal model of a transistor is an essential requirement for any circuit design. Therefore there is a continuous effort from circuit designers to produce efficient nonlinear models [116]. The first empirical nonlinear model for MESFET, established in 1980, was developed by Curtice [117]. This is followed by development of SPICE model for GaAs FET device by H. Statz et al. [118]. A SPICE model for GaAs MESFET devices over a wide range of bias conditions has been introduced by McCamant, et al. [119] by modifying the model equations proposed in [118]. A decade later, several empirical nonlinear models had been developed in order to allow the model being extracted to use Computer Aided Design (CAD) tools including the one reported by I. Angelov [17].

There are several CAD packages available for modelling devices in conjunction with the use of foundry modules in the design process [74]. Therefore, all designers have the freedom to choose any of the available CAD tools depending on whether the software has an accurate model built in. Nonlinear models for microwave and millimeter wave devices are commonly based on DC and S-parameter measurements. The model used in this work was developed by Agilent, the EEsof EE-HEMT model in Advance Design System (ADS) [75]. The EE-HEMT is an empirical analytic model based on the fitting of the measured electrical characteristics of HEMTs.

The nonlinear element, i.e., drain-source, gate-source and gate-drain current functions in addition to nonlinear capacitances are depend on the instantaneous bias conditions ($V_{GS}$ and $V_{DS}$). As the bias changes, the signal deviates from the static operating point which in turn changes the device’s performance characteristics. A relation of current-voltage for the bias conditions is then developed that approximates the measured data. In this work, the large signal is modelled using the Agilent’s EE-HEMT Nonlinear Model for GaAs FET. The details of the nonlinear parameters and characteristics of this model are presented in APPENDIX C.
5.6 Steps in Device Modelling

A complete device modelling process begins with the selection of the epitaxial layer structure. This structure is then used for device fabrication, where large number processing steps are involved. After the devices have been through all of the processing steps, the DC and S-parameters measurements are performed to verify the device’s performance. These parameter measurements are required for the next step of device modelling.

The device modelling task begins with the extraction of extrinsic and intrinsic parameters from the measured RF data. The initial linear model is then produced, after substitution of the measured extrinsic and intrinsic values, followed by tuning of the model’s parameters until the S-parameters show an excellent agreement with the measured data. Next, the linear model is optimised in order to reduce the modelling error between measured and modelled data. After this, the nonlinear modelling is carried out, where the parasitic resistances from the linear model are substituted into the nonlinear model. The task continues with the fitting of DC and RF results with the measured data. During this process the nonlinear model is constantly being optimised so that the modelling errors are reduced and finally the device model is completed.

5.7 pHEMT Device Structure

Modelling a device structure is significant in the characterization and optimisation of device performances. The empirical device modelling performed in this chapter is for various gate length devices. This includes 1 μm gate length VMBE1998 with 2x100 μm and 2x200 μm gate width, XMBE56 pHEMT sample with 0.5 μm gate length and various device size, and a 250nm T-gate pHEMT structure which is fabricated by utilizing conventional 1μm i-Line lithography and a novel solvent reflow technique [97]. The XMBE131 pHEMT is a two finger device with 50 μm gate width, 250nm gate length and 3 μm source-to-drain separation. It has a double delta-doped layer and thin gate-to-channel distance of approximately 25 nm. It is very identical to the VMBE1998 sample except for the thinner Channel layer and a doped Cap layer is developed in VMBE1998 to provide better contact resistance.
XMBE56 is a conventional single delta doped structure and was designed with a low temperature (LT) InAlAs buffer. The Channel layer in XMBE56 is the thinnest (130Å) among these three structures.

The epitaxial structure for the VMBE1998, XMBE56 and XMBE131 pHEMT is shown in Table 5.1. The epitaxial structure of XMBE131 is made of a thin channel layer and double doping layer. It consists of a semi insulating InP layer, lattice matched In\textsubscript{0.52}Al\textsubscript{0.48}As buffer layer, 140Å highly compressively strained In\textsubscript{0.7}Ga\textsubscript{0.3}As channel layer, 2.5x10\textsuperscript{-12} cm\textsuperscript{2} of silicon δ-doping layer, lattice matched In\textsubscript{0.52}Al\textsubscript{0.48}As supply layer of 150Å and 100Å spacer layer, and 50Å undoped In\textsubscript{0.53}Ga\textsubscript{0.47}As cap layer. The drain and source terminal spacing is 3μm. The device pinch off voltage is -1.2 Volt and exhibits great enhancement in the unity current gain frequency, \(f_T\) of 90 GHz and current drivability (I\textsubscript{DS}) of 580 mA/mm [97].

<table>
<thead>
<tr>
<th>Table 5.1 Epitaxial structure for various pHEMT samples fabricated at the University of Manchester</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>VMBE1998</strong></td>
</tr>
<tr>
<td>(Cap-doped) In\textsubscript{0.53}Ga\textsubscript{0.47}As 50Å</td>
</tr>
<tr>
<td>(Barrier) In\textsubscript{0.52}Al\textsubscript{0.48}As 150Å</td>
</tr>
<tr>
<td>δ-doped</td>
</tr>
<tr>
<td>(Spacer2) In\textsubscript{0.52}Al\textsubscript{0.48}As 100Å</td>
</tr>
<tr>
<td>(Channel) In\textsubscript{0.70}Al\textsubscript{0.30}As 140Å</td>
</tr>
<tr>
<td>(Spacer1) In\textsubscript{0.52}Al\textsubscript{0.48}As 100Å</td>
</tr>
<tr>
<td>δ-doped</td>
</tr>
<tr>
<td>(Buffer) In\textsubscript{0.52}Al\textsubscript{0.48}As 4500Å</td>
</tr>
<tr>
<td>(Substrate) InP Fe doped</td>
</tr>
</tbody>
</table>
The incorporating of In$_{0.7}$Ga$_{0.3}$As compressively strained channel in these epitaxial structures is an excellent choice for fabricating high frequency and low noise devices, owing to its high mobility and high saturation velocity, resulting from the high Indium content in the InGaAs channel [10]. Additionally, this reduces the gate leakage current to compensate for the thinner gate to channel thickness. The sheet carrier concentration is very high in XMBE131, as a consequence of better carrier confinement in both epitaxial layers. The carrier confinement in XMBE131 is achieved by adapting the almost square-shaped quantum well, resulted from the double δ-doped structure [14]. The carrier mobility is predominantly due to the use of highly strained In$_{0.7}$Ga$_{0.3}$As in the channel material. The Hall measurement for these pHEMT samples is tabulated in Table 5.2.

<table>
<thead>
<tr>
<th>Sample</th>
<th>VMBE 1998</th>
<th>XMBE 56</th>
<th>XMBE 131</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sheet Carrier Concentration (n$_s$) at RT / 77K ($x10^{12}$ cm$^{-2}$)</td>
<td>2.4 / 2.5</td>
<td>2.47 / 2.61</td>
<td>2.4 / 2.5</td>
</tr>
<tr>
<td>Hall Mobility ($\mu_n$) at RT / 77K (cm$^2$/V.s)</td>
<td>13896 / 47829</td>
<td>13169 / 42906</td>
<td>13896 / 47829</td>
</tr>
</tbody>
</table>

To minimize the undesired effects caused by device scaling, (such as channel length modulation), the aspect ratio between gate length and gate to channel distance must be greater than 5 [104]. The ratio between the 250nm gate and gate-to-channel thickness for this epitaxial layer is shown in equation 5.32.

$$A = \frac{\text{gate length}}{\text{gate to channel thickness}} = \frac{250\text{nm}}{25\text{nm}} = 10$$  
Equation 5.32

The pHEMT device is realized using a T-gate head with the foot print for the T-gate being 0.25μm as illustrated in Figure 5.5. The T-gate or mushroom gate is a technique of providing very short effective gate length, while providing low gate resistance [120]. The gate resistance is a parasitic element that affects the maximum
available gain of a FET, and is inversely proportional to the cross-sectional area of the metal along the gate finger. While providing low gate resistance, the short gates in the XMBE131 pHEMT device are suitable for higher-frequency applications, such as C-band and X-band LNA which will be discussed in later sections.

![Figure 5.5 An illustration of a submicron device with a T-gate structure. The T-gate footprint is 0.25 µm. (Thickness not to scale)](image)

### 5.8 DC and RF Characteristics

The DC and RF characteristics of the devices fabricated and modelled are presented in this section. The measured parameters of these devices were extracted using the Agilent Integrated Circuit Characterization and Analysis Program (ICCAP). This powerful program is used to analyse device performance, which provides a simple extraction module for DC characteristic and S-parameters data. The measured data were taken for 201 bias points to derive small signal equivalent circuit models as a function of terminal voltages. The bias point taken for the transistor is shown in Table 5.3.
Table 5.3 Biasing for in-house fabricated pHEMT sample devices (a V_DS=1V)

<table>
<thead>
<tr>
<th>Epi.layer</th>
<th>Gate fingers x width (µm)</th>
<th>Gate Length (µm)</th>
<th>% $g_m$(max)</th>
<th>V_GS (mV)</th>
<th>I_DS (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>VMBE1998</td>
<td>2x200</td>
<td>1</td>
<td>80</td>
<td>-582</td>
<td>25.45</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>90</td>
<td>-512</td>
<td>25.45</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100</td>
<td>-330</td>
<td>73.81</td>
</tr>
<tr>
<td></td>
<td>2x100</td>
<td>1</td>
<td>80</td>
<td>-568</td>
<td>13.91</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>90</td>
<td>-498</td>
<td>20.35</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100</td>
<td>-148</td>
<td>56.86</td>
</tr>
<tr>
<td>XMBE56</td>
<td>2x200</td>
<td>0.5</td>
<td>80</td>
<td>-820</td>
<td>21.60</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>90</td>
<td>-694</td>
<td>38.00</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100</td>
<td>-470</td>
<td>70.69</td>
</tr>
<tr>
<td></td>
<td>2x50</td>
<td>0.5</td>
<td>80</td>
<td>-834</td>
<td>4.89</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>90</td>
<td>-736</td>
<td>8.51</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100</td>
<td>-470</td>
<td>19.46</td>
</tr>
<tr>
<td>XMBE131</td>
<td>2x50</td>
<td>0.25</td>
<td>80</td>
<td>-560</td>
<td>10.02</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>90</td>
<td>-520</td>
<td>13.43</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100</td>
<td>-420</td>
<td>22.28</td>
</tr>
</tbody>
</table>

The DC and RF characteristic of the device is modelled prior to the LNA design which will be discussed in detail in the next chapter. The normalized output characteristic and the transconductance, $g_m$ for sample XMBE131 pHEMT are shown in Figure 5.6 (b) and Figure 5.6 (c) respectively. The superior recorded $g_m$ value (940mS/mm) for the sample is related to the increase in I_ds value due to the smaller L_G size and the smaller gate to channel distance. The barrier height, $\Phi_b$ is 0.62 eV extracted from measurement data [98]. Due to the thin barrier $\Phi_b$, thin spacer layer and also shorter gate-to-channel layer distance, this produced a smaller threshold voltage, $V_{TH}$ of approximately -0.8V. Thus the depletion region under the gate terminal, which already exists when the gate bias is 0 V, will grow wider as the reverse bias gate voltage is increased. As a result, a smaller negative gate voltage is needed to pinch the channel and consequently turn OFF the device.
Figure 5.6  pHEMT sample XMBE131 (Ti/Au gate metallisation)

(a) Normalized I-V characteristics with maximum $I_{DS}=540mA/mm$ at $V_{ds}=1V$, (b) Threshold Voltage, $V_T$, (c) Normalized transconductance, $g_m$ with $g_m=940mS/mm$ at $V_{ds}=2V$ and (d) on-state leakage current where $V_{ds}=0$ to 2V with 250mV steps
From Figure 5.6 (d), the device is OFF below $V_{th}$ and the leakages are due to carriers tunnelling through the Schottky barriers. Above $V_{th}$, the devices are ON and the leakage is mainly due to impact ionisation, where carrier multiplication takes place and a bell-shaped current profile is measured [121]. Although the current performance is excellent, however the submicron epitaxial layer does contributes to the higher leakage current due to the short gate to channel distance.

The unity current gain (h21) plot versus frequency for sample XMBE131 is illustrated in Figure 5.6. Since $f_T$ is inversely proportional to $L_G$, the short gate length contributes to the higher cutoff frequency ($f_T$) of 90GHz (extrapolated). Hence, this device is a promising component for the LNA design at higher frequency as it will have a reduced noise figure (NF).

![Graph showing unity gain frequency and maximum frequency for XMBE131 pHEMT](image)

**Figure 5.7** Unity gain frequency, $f_T$ and maximum frequency, $f_{max}$ at $V_{ds}=1V$, $I_{ds}=13.19 \text{mA}$ for sample XMBE131
Figure 5.8  pHEMT sample VMBE1998 (a) Normalized I-V characteristics with maximum $I_{DS}=321$ mA/mm$^2$ (2x50μm) and $I_{DS}=309$ mA/mm$^2$ (2x200μm) at $V_{ds}=1$V, (b) Threshold Voltage, $V_T$ at -0.89V for both device size, (c) Normalized transconductance, $g_m$ with $g_m=529$ mS/mm (2x50μm) and $g_m=500$ mS/mm (2x200μm) at $V_{ds}=2$V and (d) Off-State Gate Current Leakage :Forward and Reversed.

<table>
<thead>
<tr>
<th>Device size</th>
<th>Gate current leakage (μA/mm) @ $V_{GS} = -4$ V</th>
<th>$V_{on}$ (V) @ $I_{GS} = 0.1$ mA/mm</th>
<th>$V_{br}$ (V) @ $I_{GS} = 0.1$ mA/mm</th>
<th>Ideality Factor (n)</th>
<th>Barrier Height (eV), $\phi_B$</th>
</tr>
</thead>
<tbody>
<tr>
<td>2x 50 μm</td>
<td>573</td>
<td>0.19</td>
<td>0.7</td>
<td>1.58</td>
<td>0.36</td>
</tr>
<tr>
<td>2x200 μm</td>
<td>595</td>
<td>0.19</td>
<td>0.7</td>
<td>1.58</td>
<td>0.39</td>
</tr>
</tbody>
</table>

It is observed from Figure 5.8 (a) that the I-V characteristics have a well-behaved behavior with a sharply defined pinch-off. No kink effect observed for both devices is highly contributed to the high indium content in the thin channel layer for the 1 μm device VMBE1998. In Figure 5.8 (d), The normalized gate current leakage for the mentioned devices is about 573 to 595 μA/mm at $V_{GS} = -4$ V. The ideality factor and barrier height, $\phi_B$, shown in Table 5.4 are comparable across devices, although a low barrier height (typically around 0.5 eV) gives higher leakage current.
Figure 5.9  RF characteristics for pHEMT sample VMBE1998, 2x50 μm and 2x200 μm  
(a) Cut-off frequency, $f_T$ at $V_{DS}=1\,\text{V}$, 80% $g_{m\text{max}}$ and (b) Maximum frequency, $f_{\text{max}}$  
extrapolated at $V_{DS}=1\,\text{V}$, 80% $g_{m\text{max}}$
(a) 

(b) 

(c)
Figure 5.10 pHEMT sample XMBE56: (a) Normalized I-V characteristics with maximum \( I_{DS} = 450 \text{ mA/mm}^2 \) (2x50\( \mu \text{m} \)) and \( I_{DS} = 385 \text{ mA/mm}^2 \) (2x200\( \mu \text{m} \)) at \( V_{ds} = 1 \text{V} \), (b) Threshold Voltage, \( V_T \) at -0.98V (2x50\( \mu \text{m} \)) and \( V_T \) at -1.0V (2x200\( \mu \text{m} \)), (c) Normalized transconductance, \( g_m \) with \( g_m = 430 \text{ mS/mm} \) (2x50\( \mu \text{m} \)) and \( g_m = 380 \text{ mS/mm} \) (2x200\( \mu \text{m} \)) at \( V_{ds} = 1 \text{V} \), (d) Off-State Gate Current Leakage: forward and reverse and (e) on-state leakage current for \( V_{ds} = 0 \) to 2V.

The DC characteristics for 0.5 \( \mu \text{m} \) gate length XMBE56 pHEMT samples are given in Figure 5.10. Figure 5.10 (a) shows the I-V characteristics for both device size with a sharply defined pinch-off. There is kink effect observed at significantly higher \( V_{GS} \) (for \( V_{DS} \) below 1.0 V) indicating little carrier loss under gate-bias. Obviously, the maximum drain current is higher compared to the 1 \( \mu \text{m} \) gate length VMBE1998.
samples as the gate length is reduced to submicron. However, it’s less by almost half of the maximum current for XMBE131. This is due to the carrier concentration in XMBE56 is lower, which contributes less electrons available for current conduction, and consequently the output current is reduced. Since $g_m$ is directly proportional to the rate of change of $I_{DS}$, the $g_m$ for XMBE56 is increased, as illustrated in Figure 5.10 (c). The $I_{DS}$ current in both the linear and saturation region is inversely proportional to the device’s gate length. In Figure 5.10(d), the normalized gate current leakage for the 2 x 50 $\mu$m XMBE56 device is about 25 $\mu$A/mm and 30 $\mu$A/mm for 2 x 200 $\mu$m sample at $V_{GS} = -4$ V. This is a low leakage device as compared to the other two point structure, XMBE131 and VMBE1998, due to the high barrier and thicker spacer layer adopted in the epitaxial layer. The ideality factor and barrier height, $\phi_B$, calculated from the measured current characteristic are shown in Table 5.5. The RF characteristics, $f_T$ and $f_{max}$ for both XMBE56 device samples are presented in Table 5.6.

Table 5.5 Ideality factor and Barrier height for XMBE56 pHEMT sample

<table>
<thead>
<tr>
<th>Device size</th>
<th>Gate current leakage (µA/mm) @ $V_{GS} = -4$ V</th>
<th>Ideality Factor (n)</th>
<th>Barrier Height (eV), $\phi_B$</th>
</tr>
</thead>
<tbody>
<tr>
<td>2x50 µm</td>
<td>25</td>
<td>1.46</td>
<td>0.50</td>
</tr>
<tr>
<td>2x200 µm</td>
<td>30</td>
<td>1.28</td>
<td>0.57</td>
</tr>
</tbody>
</table>

Table 5.6 Transconductance and RF characteristics XMBE56 pHEMT sample

<table>
<thead>
<tr>
<th>Device size</th>
<th>Biasing at 100% $g_m$ max (5 um S-D spacing)</th>
<th>Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$g_m$ (mS/mm) - Normalized-</td>
<td>$V_{GS}$ (V)</td>
</tr>
<tr>
<td>2x50um</td>
<td>433.3</td>
<td>-0.400</td>
</tr>
<tr>
<td>2x200um</td>
<td>380.3</td>
<td>-0.470</td>
</tr>
</tbody>
</table>
5.9 Linear Model for device under test

The linear modelling of pHEMT device is performed by extraction of extrinsic and intrinsic parameters from pinched and biased dependent S-parameter measurements. This will eventually avoid the frequency dispersion effect of the drain conductance $g_{ds}$ and transconductance, $g_m$. The generated initial linear model is optimised by fitting the modelled and measured S-parameter data which will consequently reduce the modelling error. The intrinsic data of the 2x50μm XMBE131 pHEMT are extracted from measured S-parameter using ICCAP and the measured data are compared with the simulated models.

![Diagram](image)

Figure 5.11 (a) Schematic and (b) Equivalent transistor linear model [122]

The intrinsic model parameters were obtained from hot (active) device bias points, while the extrinsic (parasitic) elements were obtained from cold (pinched) device measurements [17]. Figure 5.11 shows the linear model of a transistor. The final element values for linear models were determined by optimisation of the initial value to accurately fit the measured data. Voltage dependent $C_{gs}$, $C_{ds}$ and $C_{gd}$ are modelled and parameterized in the linear model simulations.

The circuit setup for XMBE131 pHEMT extrinsic element extraction is shown in Figure 5.12. The equations that have been derived from the small signal model were defined in this setup using MeasEqn element. The two-port network circuit setup was terminated with 50 $\Omega$ resistance at both input and output port. The measured dataset files from ICCAP is saved in the S2P components. For other pHEMT sample,
i.e., XMBE56 and VMBE1998, the S2P data set file is defined according to the measured pHEMT data set. The frequency range is set from 400MHz to 20 GHz for the S-parameter simulations.

Figure 5.12 Circuit Setup for Extrinsic element extraction (pinched) in ADS for XMBE131.
Table 5.7 tabulated the extrinsic elements of the sample device which are bias independent. These elements are the capacitance, resistance and inductance at the electrodes which results from metallisation of the contact with the surface, resistance due to ohmic contact and variation of depletion charge with respect to the gate-source and gate-drain voltages. The gate inductance, $L_g$ is usually large for short gate length devices.

Table 5.7 Table of Extrinsic values for various pHEMT sample devices

(V$_{DS}$=1V,Idss = 20%)

<table>
<thead>
<tr>
<th>Sample Device</th>
<th>C$_{pg}$ (fF)</th>
<th>C$_{pd}$ (fF)</th>
<th>R$_S$ (Ω)</th>
<th>R$_g$ (Ω)</th>
<th>R$_d$ (Ω)</th>
<th>L$_S$ (pH)</th>
<th>L$_g$ (pH)</th>
<th>L$_d$ (pH)</th>
</tr>
</thead>
<tbody>
<tr>
<td>VMBE1998 2x100 µm</td>
<td>13.39</td>
<td>23.26</td>
<td>0.78</td>
<td>1.34</td>
<td>1.18</td>
<td>12.86</td>
<td>9.61</td>
<td>0.42</td>
</tr>
<tr>
<td>VMBE1998 2x200 µm</td>
<td>18.75</td>
<td>53.25</td>
<td>1.02</td>
<td>1.6</td>
<td>0.956</td>
<td>25.91</td>
<td>41.37</td>
<td>53.86</td>
</tr>
<tr>
<td>XMBE56 2x50 µm</td>
<td>16.66</td>
<td>25.70</td>
<td>0.9</td>
<td>1.4</td>
<td>0.9</td>
<td>15.39</td>
<td>47.96</td>
<td>27.31</td>
</tr>
<tr>
<td>XMBE56 2x200 µm</td>
<td>7.27</td>
<td>89.63</td>
<td>0.85</td>
<td>1.02</td>
<td>0.9</td>
<td>3.31</td>
<td>110.94</td>
<td>120.4</td>
</tr>
<tr>
<td>XMBE131 2x50 µm</td>
<td>7.73</td>
<td>6.62</td>
<td>0.69</td>
<td>0.83</td>
<td>0.32</td>
<td>18.70</td>
<td>27.20</td>
<td>23.84</td>
</tr>
<tr>
<td>XMBE131 2x200 µm</td>
<td>69.04</td>
<td>24.58</td>
<td>1.81</td>
<td>0.89</td>
<td>1.45</td>
<td>18.91</td>
<td>47.72</td>
<td>61.69</td>
</tr>
</tbody>
</table>

From the Table 5.7, it can be observed that the capacitance values increase as the total device width is increased. Since the capacitance value is proportional to the contact area, the capacitance increases as the contact pad areas become larger. The terminal resistances are also reduced as the device size is increased. As the gate width is increased, the total gate area will increase, and consequently it will decrease.
the terminal resistances. The sub-micrometer gate length devices show comparable gate resistances due to the implementation of a T-gate structure at the gate terminal.

Figure 5.13 Parameter extraction setup for Hot measurement
(XMBE131 for 2 x 50 μm device at V_{DS} = 1 V, 90% g_{mmax})

The setup for the hot model is illustrated in Figure 5.13. The extraction of intrinsic parameters can be obtained from the bias dependent (hot) measurement. For example, the device is biased in the low power and low noise region, where V_{DS} = 1 V and I_{DS} = 20 % I_{DSS} (about 80% - 90% of maximum g_m). The biasing points for all of the studied devices are tabulated in Table 5.3.
Table 5.8 shows the intrinsic values for sample XMBE131 with 2x200 \( \mu \)m (taken only for parasitic comparison) and 2x50 \( \mu \)m gate width pHEMT device. From the results, the capacitance values increase as the total device width increased because the capacitance value is proportional to the contact area. Hence the capacitance increases as the contact pad areas become larger. The terminal resistances increase with increase in device size. As the gate width is increased, the total gate area will increase and consequently it will decrease the terminal resistances [95]. A significant reduction in the resistance between drain and source, \( R_{ds} \) values is observed with the increasing of device width. There is a direct correlation between device width increases with the total area increased which consequently reduced the channel resistance.

<table>
<thead>
<tr>
<th>Sample Device</th>
<th>Total width</th>
<th>( g_m ) (mS)</th>
<th>( T ) (psec)</th>
<th>( R_i ) (( \Omega ))</th>
<th>( R_{ds} ) (( \Omega ))</th>
<th>( C_{gs} ) (pF)</th>
<th>( C_{ds} ) (pF)</th>
<th>( C_{gd} ) (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>VMBE1998 (1( \mu )m)</td>
<td>2x100 ( \mu )m</td>
<td>69</td>
<td>1.52</td>
<td>4.55</td>
<td>580</td>
<td>0.538</td>
<td>0.02</td>
<td>0.044</td>
</tr>
<tr>
<td></td>
<td>2x200 ( \mu )m</td>
<td>175</td>
<td>1.93</td>
<td>0.9</td>
<td>192.5</td>
<td>1.36</td>
<td>0.055</td>
<td>0.101</td>
</tr>
<tr>
<td>XMBE56 (0.5( \mu )m)</td>
<td>2x50 ( \mu )m</td>
<td>27.00</td>
<td>1.330</td>
<td>4.556</td>
<td>484</td>
<td>0.068</td>
<td>0.024</td>
<td>0.036</td>
</tr>
<tr>
<td></td>
<td>2x200 ( \mu )m</td>
<td>123.00</td>
<td>0.440</td>
<td>2.720</td>
<td>132.5</td>
<td>0.344</td>
<td>0.021</td>
<td>0.081</td>
</tr>
<tr>
<td>XMBE131 (0.25( \mu )m)</td>
<td>2x50 ( \mu )m</td>
<td>64.8</td>
<td>1.53</td>
<td>4.33</td>
<td>316.0</td>
<td>0.12</td>
<td>0.01</td>
<td>0.02</td>
</tr>
<tr>
<td></td>
<td>2x200 ( \mu )m</td>
<td>321.8</td>
<td>2.98</td>
<td>2.82</td>
<td>65.6</td>
<td>0.08</td>
<td>0.03</td>
<td>0.03</td>
</tr>
</tbody>
</table>

At this stage, the linear model is completed and the parameter value a ready for the nonlinear model optimisation. However, only the 2x50 \( \mu \)m gate width device will be discussed in details and applied in the LNA designs in this work.
5.10 Nonlinear Modelling

Nonlinear model consists of optimisation of the model for the DC and RF characteristics of the device. For the nonlinear modelling to be performed, the parasitic values which were defined and optimised earlier in the linear model are very important. The parasitic components were extracted from the S-parameter data set measured under different DC current. The parasitic values implemented in the nonlinear modelling have been shown in the Table 5.5. The following section present and discuss the results for both DC and RF characteristics for the 0.25µm gate XMBE131 pHEMT.

5.10.1 DC Characteristics

To develop the DC model, firstly the \( R_s \), \( R_d \) and \( R_g \) resistances obtained from the linear model are substituted into the ADS EE-HEMT model. The EE-HEMT model equations were developed concurrently with parameter extraction techniques to ensure the model parameters was extractable from the measured data. The drain-source parameters and transconducance, \( g_m \) compression parameters are then extracted from the measured \( g_m \) versus \( V_{GS} \) value as illustrated in Figure 5.14. These parameters provide the initial point of the nonlinear device model. The parameters are then tuned for optimum fit between the measured and modelled DC characteristics. Figure 5.14 shows the modelling setup using an EEHEMT model for the XMBE131 DC model.
In the DC modelling, two types of graph from the DC measurements are used: the IV and transconductance ($g_m$) curves. Figure 5.15 (a) shows the comparison between the measured and modelled I-V characteristics. The graph shows excellent agreement between the two sets of data, except around the kink area. The kink effect is as expected for a short channel device as a result of impact ionization [18]. These show extremely well-behaved curves with a sharply defined pinch-off, a small output conductance and a very small amount of kink effect (indicating little carrier loss under low gate-bias). Nevertheless, for the bias conditions required, the low noise zone in this work ($V_{DS} = 1$ V) is safely outside the kink region.

Figure 5.15 (b) depicts the threshold voltage which shows excellent fitting between measured and the DC empirical model. In Figure 5.15 (c), the curve fitting between the measured and modelled $g_m$ is presented. The model demonstrated a very good agreement between the two data specifically at higher gate voltage, $V_{GS}$. Nonetheless, there is a marginal divergence at lower $V_{GS}$ due to the limitations in the DC model [11] where kink anomalies are usually observed.
Figure 5.15 Measured versus modelled XMBE131 pHEMT (a) I-V characteristics (for $V_{GS}=0.1$ V to -0.8 V, -0.1 V steps), (b) threshold voltage (for $V_{DS}=1$ V to 2 V, 0.25 V steps) and (c) Transconductance ($g_m$) for both measured versus modelled for XMBE131 pHEMT

5.10.2 RF Performance

The RF performance is extracted from the nonlinear model simulations. However, here the fitted components result in parameters that are totally different from the results of the intrinsic parameters fitting in the linear modelling work. Therefore, the S-parameter curve fitting in the RF model is a much more difficult task than the curve fitting in linear model. Additionally the model is validated via modelling of the S-parameters over several bias points. Moreover, the drain-source currents ($I_{DS}$) for every bias point are also monitored because sometimes good matching of S-
parameter data can be obtained, although a large difference between modelled and measured $I_{DS}$ values still exists.

The biasing point is taken based on the percentage of maximum $g_m$. In this work, the extracted S-parameter for 80% $g_m$ and 90% $g_m$ bias point (~20% to 30% $I_{DSS}$) is taken into consideration. The comparison of modelled and measured S-parameter for the nonlinear model of the XMBE131 device is depicted in Figure 5.16 over the frequency range of 40 MHz to 20 GHz.

![Graph showing Gain (dB) vs. Frequency (GHz)](image1)

(a)

![Graph showing Reflection Coefficient (dB) vs. Frequency (GHz)](image2)

(b)

Figure 5.16 Curve fitting for 2x50μm XMBE131 (a) Forward and Reverse Gain and (b) Input and output reflection coefficient over frequency 40 MHz to 20 GHz measured at 80% of maximum $g_m$
The forward gain (S21), reverse gain (S12), input reflection coefficient (S11) and output reflection coefficient (S22) is illustrated in Figure 5.16. The gain curve (S21) is about 20 dB in the range of 1 ~ 3GHz. The gain starts to decrease with the frequency and the input reflection coefficient (S11) is below -10dB. The modelled data for the bias point show excellent agreement with the measured data with very small percentage errors. The excellent curve fitting in DC and RF characteristics is important in order to obtain an optimised active device. The optimised transistor model presented in Figure 5.17 is now complete and ready to be implemented in the LNA circuit design which will be discussed in the Chapter 6.

![Transistor Model](image)

**Figure 5.17** A Complete transistor model for XMBE131 2 x 50 µm pHEMT

Figure 5.18 and Figure 5.19 shows some example of the DC and RF fitting for the other devices. The summary of modelled data shows excellent agreement with the measured data with very small percentage errors.
Figure 5.18 Summary of curve fitting for 2 x 200 μm on VMBE1998  (a) I-V curve (b) Transconductance (c) Forward and reverse gain and (b) Reflection coefficient against frequency
Figure 5.19 Summary of curve fitting for 2 x 200 μm on XMBE56 (a) I-V curve (b) Transconductance (c) Forward and reverse gain and (b) Reflection coefficient against frequency
5.11 Noise Model

The Noise Figure (NF) is a measure of the level of noise generated from an active device when RF signal is applied. The noise characteristics of the fabricated devices are summarised in this section. The device’s minimum Noise Figure (NF$_{\text{min}}$) is plotted against device width at a certain frequency to analyse the relationship and advantage of device scaling. For optimum device matching, NF$_{\text{min}}$ can be viewed as the minimum Noise Figure (NF) that can be produced from the device. Thus, it is important to have optimum RF matching, as improper matching can make NF larger than NF$_{\text{min}}$. Fukui’s [123] NF$_{\text{min}}$ expression is used to find the minimum noise figure (NF$_{\text{min}}$) parameter for the fabricated devices and is derived as Equation (5.33 – 5.34) with a constant, $k_1$ is equal to 3.5 [124]:

$$NF_{\text{min}} = 10 \ast \log \left( 1 + k_1 \frac{f}{f_T} \sqrt{g_m(R_s + R_g)} \right)$$  \hspace{1cm} \text{Equation 5.33}$$

where, $f_T$ is the unity current gain cut-off frequency given by Equation 5.34:

$$f_T = \frac{g_m}{(C_{gs} + C_{gd})}$$  \hspace{1cm} \text{Equation 5.34}$$

The values of $g_m$, $R_s$, and $R_g$ can be obtained from the linear model. Table 5.20 illustrated the plot of NF$_{\text{min}}$ against transistor’s width for all epitaxial layers under study at 2 GHz. The calculation is also done for the NF$_{\text{min}}$ at 5.8 GHz and 10 GHz so that the noise figure at the C- and X-band frequency can be predicted. In general, a larger device will exhibit higher NF$_{\text{min}}$ characteristics. In the calculation of NF$_{\text{min}}$, the noise characteristic depends on $g_m$ and the summation of $R_s$ and $R_g$ values. From the extrinsic and intrinsic parameter extraction in section 5.9, the device’s $g_m$ increases with the increasing total device width. On the other hand, as the device’s total width is increased, the summation of $R_s$ and $R_g$ reduced. However, the increases in $g_m$ outweigh the decrease in $R_s$ and $R_g$ values. Thus, NF$_{\text{min}}$ follows the trend of the square root of $g_m$, where larger values are obtained for larger devices as shown in Table 5.9.
From the Table 5.9, the 1 μm devices show higher noise characteristics than the submicron devices. Since the $f_T$ for the submicron devices is more than double that of the 1 μm devices, from Equation 5.33, it is clear that the $NF_{\text{min}}$ for submicron devices has been successfully reduced (including the larger device periphery). The $NF_{\text{min}}$ difference at 2 GHz between the 1 μm gate device (VMBE1998) and 0.25 μm gate device (XMBE131) is about 0.4 dB with a reduction of almost 90%. At higher frequency (above 5.8 GHz), the $NF_{\text{min}}$ difference for these devices is almost 50%. This is why the submicron devices dominate an excellent performance over 1 μm gate length pHEMT in low noise amplifier design.

Another important equation in discussing the noise characteristic is given by Equation 5.35,

$$NF = NF_{min} + \frac{4R_n}{Z_0} \left[ \Gamma_S - \Gamma_{opt} \right]^2 \left[ 1 + \Gamma_{opt} \right]^2 \left[ 1 - \Gamma_S \right]^2$$

Equation 5.35
Where the four noise parameters are:
\[ \Gamma_S = \text{complex source reflection coefficient}, \]
\[ \Gamma_{\text{opt}} = \text{complex optimum reflection coefficient}, \]
\[ \text{NF}_{\text{min}} = \text{minimum noise figures when } \Gamma_S = \Gamma_{\text{opt}} \text{ in dB}, \]
\[ R_n = \text{the noise resistance}, \]
\[ Z_o = \text{the system impedance (50 W)}. \]

Equation 5.35 shows the relationship of NF with respect to the four noise parameters. It can also be interpreted as the how far the NF value can deviate with respect to NF_{min}. In practice, \( \Gamma_S \neq \Gamma_{\text{opt}} \), hence the second term will never be zero. In other words, if the four noise parameters are small, the second term in Equation 5.35 will be small, thus NF will be closer to NF_{min}. \( R_n \) plays an important role in determining the NF of the device and the mismatch between NF and NF_{min} can be reduced if \( R_n \) is reduced. The \( R_n \) value will change depending on the device widths [95]. A large device periphery is preferable, not just because it can provide high circuit gain, but also because it gives better RF matching, resulting in NF being closer to NF_{min}. However, in this work the 2x50 \( \mu \)m submicron gate length XMBE131 device is chosen as it provides the lowest NF_{min} over the frequency of interest.

5.12 Summary

The empirical models for various gate length (1\( \mu \)m and 0.25 \( \mu \)m) and device width size pHEMT samples were developed in ADS using the EEHEMT model. The linear and nonlinear parameters of the small signal and large signal pHEMT equivalent model for the 1 \( \mu \)m VMBE1998, 0.5 \( \mu \)m XMBE56 and 0.25 \( \mu \)m XMBE131 are presented and compared with the experimental results from ICCAP. The DC characteristics and S-parameter acquired from the models is closely matched with the experimental results. Based on the model, the noise figure (NF) of the device is calculated at certain frequencies to predict the minimum noise figure it might contribute when integrated into an LNA circuit. The optimized nonlinear pHEMT model obtained for XMBE131 pHEMT sample will be used as an active device in the MMIC LNA circuit design which will be explained in Chapter 6.
CHAPTER 6

DESIGN OF MONOLITHIC MICROWAVE INTEGRATED CIRCUIT LOW NOISE AMPLIFIER USING In$_{0.7}$Ga$_{0.3}$As/In$_{0.52}$Al$_{0.48}$As pHEMTs

6.1 Introduction

The low noise amplifier (LNA) is a crucial component in RF transceiver design which characterises the whole performance of the RF receiver. It is the most important block in any receiving system because the receiving system sensitivity is generally determined by its gain and noise figure. Most of the high frequency LNAs, such as those used in L-band, X-band and Ku-band are designed with CMOS, JFET, pHEMT and MESFET technologies. They are used in a wide variety of applications like military aircraft, wireless communications, radar communication, GPS applications and radio astronomy [69,70,71]. In general, the noise figure, NF, available gain, and stability over wide range of frequency are key elements in LNA designs. Low noise figure without adequate gain or poor return loss degrades system performance while high gain without adequate noise figure also compromises system performance [38,72]. According to Haus and Adler [128], the lowest possible NF that can be achieved for an LNA is not better than the NF$_{\text{min}}$ of the transistor inside the LNA.

The performance of LNAs is measured by a number of figures of merit (FOM) as discussed in Chapter 5. This chapter also describes important considerations and procedures to meet the stringent performance requirement of LNA in order to successfully implement the LNA design. A theoretical study of preferred LNA circuit topologies and the design specifications and selection of the active device are also discussed. This is followed by the concept of DC biasing at an appropriate operating point as explained in Chapter 5. Furthermore, the DC bias points will depend on the circuit applications such as low noise, high gain or high power. Tradeoffs between noise figure, gain, bandwidth, linearity, supply voltage, and
power consumption has to be considered carefully especially in high-frequency frequency LNA designs. Since noise is the primary concern in this project, the biasing network and impedance matching are defined so that the designs’ system impedances are optimised, the circuits are stable, and, of particular importance, give the lowest possible noise characteristics. The proposed design and development of Monolithic Microwave Integrated Circuit (MMIC) LNA which is implemented using the in-house fabricated 0.25-μm gate length In$_{0.7}$Ga$_{0.3}$As/InAlAs XMBE131 pHEMT device is explained in detail in the subsequent sections.

6.2 MMIC Technology

The Monolithic Microwave Integrated Circuit (MMIC) is the technology solution selected for this LNA circuit design. The fundamental principle of MMIC design suggests that all of the passive (such as capacitors and inductors) and active components (e.g. transistors) are fabricated on the same semiconductor substrate. The integrated circuit which consists of both active and passive components is fabricated on the same circuit [43] which typically operates in the frequency range of 300 MHz to 300 GHz, and corresponds to a wavelength of 1 m to 1 mm. Particularly in low noise applications, the HEMT together with the advances in MMIC technology, is driving future high volume, low cost, high performance millimetre-wave applications with high prospects [129]. For the past decades, the use of pHEMT in MMIC LNA was established mainly with GaAs pHEMTs. However, the excellent performance of InP-based pHEMTs has now become the state-of-the-art of MMIC LNA and other high speed design. With the superior performance of InP-over GaAs-based pHEMT, it has made it possible for MMIC LNA with THz range cut-off frequencies ($f_T$) to be developed as reported in [70, 71].

Monolithic Microwave Integrated Circuits (MMICs) have been widely used due to their advantages over other microwave technologies. MMICs are suitable for many applications such as smart cards and receiver modules [77,78,79] due to their compact size, thus they can be mass produced. Besides, MMIC LNAs offer excellent performances due to the reduced number of parasitic elements caused by wire bonds and embedded active devices within the printed circuit. The reproducibility is also excellent as all of the active and passive components are produced using the same
photolithography masks. An accurate model of active and passive devices contributes to the successful MMIC circuit. The modelling of the active device pHEMT has been addressed in Chapter 4 and Chapter 5. Therefore, the following subtopics will discuss in detail the modelling and design of MMIC passive elements.

6.3 Passive Component Design

A brief description of lumped passive components, i.e., thin film resistors, spiral inductors, and MiM capacitors which are used in MMIC design will be covered in this section. These passives are critical for circuit performance and reliability as they provide impedance matching, attenuation, filtering, DC bypassing and DC blocking [38, 127]. Moreover, these lumped components also determine the bandwidth, centre frequency and other important electrical characteristics of the system. Other than the basic lumped components such as inductors, capacitors and resistors, passives also include more advanced components such as chokes, resonators, directional couplers, baluns and EMI filters that play critical roles in RF microwave circuitry [127]. The use of passive components in microwave circuit design requires preparation of accurate physical models based on practical measurements of the fabricated components to avoid significant errors in the design process. Due to the non-ideal nature of the lumped components, their equivalent circuit model comprises more than the prime element, the values of which are highly process dependent rather than following particular design equations.

At RF frequencies, these passive components have parasitic effects which start to dominate as the frequency is increased. Therefore, each component has its own equivalent circuit model. The choice of these components is based upon its quality factor and resonant frequency. For low frequencies each of these components behaves as predicted by its impedance formulas. However at higher frequencies resistors change their impedances as a function of frequency, inductors become capacitive and capacitors show inductive responses [136].

167
6.3.1 MMIC NiCr Resistor

MMIC resistors are usually fabricated from Tantalum Nitride (TaN) or Nickel Chromium (NiCr) [43]. However, NiCr resistors are widely used in circuit design due to their low temperature coefficient of resistance (TCR) and small parasitic value [137]. In this project, NiCr is used to produce MMIC resistors by following the approach of Sharma et al. as outlined in [138] for which the equivalent circuit model is shown in Figure 6.1.

\[ Y_{11} + Y_{21} = j \omega C \]  \hspace{1cm} \text{Equation 6.1}

\[ Y_{21} = -\frac{1}{(R + j \omega L_s)} \]  \hspace{1cm} \text{Equation 6.2}

Assuming \( \omega^2 L_s^2 \ll R^2 \) then the \( Re \) and \( Im \) part of \( Y_{21} \),

\[ Re|Y_{21}| = -\frac{1}{R} \]  \hspace{1cm} \text{Equation 6.3}

\[ Im|Y_{21}| = \frac{\omega L_s}{R^2} \]  \hspace{1cm} \text{Equation 6.4}

Figure 6.1 Equivalent circuit model for NiCR resistor

From Figure 6.1, \( R \) is the real value of resistance, \( L_s \) is the series inductance and \( C_{sh} \) is the shunt capacitance to ground. The structure is assumed to be symmetrical. The parameters for a two port network are applied to extract all of the values. The equations are listed as follows:
The Equation 6.1 to Equation 6.4 were modelled using the ADS software. Several NiCr resistors were modelled for a wide frequency range to ensure they can be implemented in the C- and X-band frequency range as depicted in Figure 6.2.

![Figure 6.2 NiCr resistors modelled in ADS](image)

Figure 6.2 NiCr resistors modelled in ADS

Figure 6.3 shows the layout design for the NiCr resistor. The resistance value ($R$) is 8 kΩ and $L_s$ is 32 pH. The values for $C_{sh}$ were very small and therefore can be neglected.

![Figure 6.3 Layout design of MMIC NiCr resistor (7.5 kΩ) with total wire length, L=3100 μm and wire width, W=20 μm.](image)

Figure 6.3 Layout design of MMIC NiCr resistor (7.5 kΩ) with total wire length, $L=3100$ μm and wire width, $W=20$ μm.
6.3.2 MMIC Capacitance

The ability of passive component to store charge is measured in terms of capacitance and determines its impedance to RF signals. RF signals pass through capacitors by charging and discharging them. A larger capacitor provides lesser impedance. In MMIC circuits, capacitors are formed by two main methods: the coupled lines or interdigital capacitors and metal-insulator-metal (MIM) capacitors. The interdigital capacitor, shown in Figure 6.4 [139], mainly relies on fringing capacitance between the interdigital metal strips referred to as fingers.

![Figure 6.4 An example for coplanar interdigital capacitor for MMICs [139]](image)

These capacitors use the same metallisation plane as used for transmission lines. The fringing capacitance is fairly low and hence these capacitors reach very low capacitance (~1 pF) and are usually used in high frequency applications. The advantage of interdigital capacitors is that they are simpler to fabricate in MMIC process since they require a single metal layer and its capacitance value is fairly insensitive to process variations. Compared to interdigital capacitors, the MIM capacitor has the ability of achieving much higher capacitance values and are usual choice in MMIC for DC blocking, decoupling and feedback purposes.

The MIM capacitors are designed by sandwiching a layer of dielectric between two metal plates (bottom and top). The dielectric layers are usually silicon nitride, polyimide or silicon dioxide [97]. In this LNA design, silicon nitride was used as the
dielectric material. The equivalent circuit model for the MIM capacitor is illustrated in Figure 6.5.

![Equivalent circuit for MMIC Capacitance](image)

Figure 6.5 Equivalent circuit for MMIC Capacitance

R_{11} and R_{22} are the resistances for the top and bottom plates respectively. L_{11} is the series inductance of the top plate, and L_{22} is the series inductance for the bottom plate. The the capacitances of the top and bottom plates are denoted with C_{11} and C_{22} respectively. The main capacitor, C is calculated as:

\[ C = \varepsilon_0 \varepsilon_r \frac{W L}{t_d} \]  

Equation 6.5

Where \( \varepsilon_0 \) is the free space permittivity, \( \varepsilon_r \) is the relative permittivity of the dielectric, \( t_d \) is the thickness of the dielectric material, and \( W \) and \( L \) are the width and length of the overlapped metal plates respectively.

The loss in conductance, \( G \) due to the capacitance of the dielectric is computed by calculating the product of the loss tangent (\( tan\delta_d \)) in Equation 6.6.

\[ G = \omega C tan\delta_d \]  

Equation 6.6

The metal plate loss resistances \( R_{11} \) and \( R_{22} \) are given by:

\[ R_{11} = R_{22} = \frac{\rho L}{W t_p} \]  

Equation 6.7
Where $r$ is the metal resistivity and $t_p$ is the thickness of either the top or bottom plate.

The metal plate inductance and parallel capacitance can be obtained from [98]:

$$L_{11} = L_{22} = \frac{0.4545Z_0L}{C}$$  \hspace{1cm} \text{Equation 6.8}

$$C_{11} = C_{22} = \frac{0.5\varepsilon_{\text{eff}}L}{CZ_0}$$  \hspace{1cm} \text{Equation 6.9}

Where $Z_0$ is the characteristic impedance = 50$\Omega$. The values of 0.4545 and 0.5 from Equation 6.8 and Equation 6.9 is the proposed model parameters.

All of the MIM capacitor equations were modelled using the ADS software. Figure 6.5 shows the modelled circuit for MMIC passive MIM capacitor setup in the ADS. The S-parameter simulation result for 2 pF modelled capacitor is presented in Figure 6.7.

![Figure 6.6 Modelled circuit for MIM Capacitor setup in ADS](image)

172
Figure 6.7 S-parameter results for an 8pF MIM capacitor over the frequency

6.3.3 Spiral Inductor for MMIC Inductance

The inductors are essential for bias injection into oscillators, amplifiers and microwave switches. Moreover, they are also used as circuit components for matching networks in microwave circuit design. In hybrid MIC designs, low-loss inductors are essential for developing low cost, low-noise amplifiers with high power added efficiency. In MMIC designs, there are certain limitations in achieving a low loss inductor. Inductors in MMIC are designed in several forms such as narrow tracks, meandered lines, single loop or multilayered spiral inductors. Spiral inductors typically comprise a transmission line in a spiral shape.

The spiral structure can be realised in many different forms such as rectangular, circular, hexagonal, square shape and octagonal [99]. Rectangular shaped spiral inductors will be discussed here that have been used in MMIC LNA designs for this work. The Spiral inductor requires at least two metal layers to prevent a shorted connection. Figure 6.8 shows the equivalent circuit model for the spiral inductor which consists of the series combination of an inductor and a resistor in parallel with a capacitor. Typically, an ideal inductor has a linear impedance as a function of frequency. However, a real inductor will have nonlinearity at high frequency.
Figure 6.8 Equivalent circuit for spiral inductor

$L$ denotes the primary inductance is which in series with the resistance $R_s$. $C_p$ is the feedback capacitance and $C_F$ is the capacitance of the metal to the ground.

$$L = 2.34 \times \frac{\mu_0 n_L^2 ((D_L + d_L)/2)}{1 + 2.75 \rho}$$  \hspace{1cm} \text{Equation 6.10}

and

$$\psi = \frac{D_L - d_L}{D_L + d_L}$$  \hspace{1cm} \text{Equation 6.11}

Where $\mu_0$ is the permeability of free space, $n_L$ is number of turns, $k_{L1}$ and $k_{L2}$ are the processing dependent fitting factors and $\psi$ is the ratio of the difference between outer diameter, $D_L$ and inner diameter, $d_L$ of the spiral inductor. Values for $k_{L1}$ and $k_{L2}$ are 2.34 and 2.75 respectively as reported in [99].

$R_s$, $C_p$ and $C_{sub}$ can be calculated using the equations listed below:

$$R_s = \frac{P_L \rho}{t_p W_L}$$  \hspace{1cm} \text{Equation 6.12}

$$C_p = n_L \varepsilon_0 \varepsilon_r \left( \frac{W_L x L_L}{t_p \text{-dielectric}} \right)$$  \hspace{1cm} \text{Equation 6.13}

and
\[ C_F = \frac{W_L P_L C_o}{2} \]

Equation 6.14

Where \( \rho \) is the metal resistivity, \( t_p \) is the metal thickness, \( t_{p\text{-dielectric}} \) is the silicon nitride thickness, \( P_L \) is the length of metal, \( W_L \) is the width of the square metal and \( C_o \) is a process dependent fitting parameter. The equivalent circuit is modelled in ADS and shown in Figure 6.23. In the modelling, usually \( C_F \) is very small and can be omitted. The parameters used in this project are summarised in Table 6.1.

![Figure 6.9 Schematic of equivalent circuit for spiral Inductor modelled in ADS.](image)

Table 6.1 Parameter value used for in-house fabricated spiral inductor

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>( P )</td>
<td>( 2.44 \times 10^{-8} \Omega \cdot m )</td>
</tr>
<tr>
<td>( t_p )</td>
<td>( 450 \text{nm} )</td>
</tr>
<tr>
<td>( t_{p\text{-dielectric}} )</td>
<td>( 90 \text{nm} )</td>
</tr>
<tr>
<td>( \varepsilon_r )</td>
<td>( 7.5 )</td>
</tr>
<tr>
<td>( C_o )</td>
<td>( 5 \times 10^{-6} \text{F} )</td>
</tr>
</tbody>
</table>

A number of spiral inductors were designed and fabricated at the University of Manchester to verify the equivalent circuit model which will be used for the LNA design. However, only one value, a 14 nH inductor, is included in this chapter as an example. The S-parameters results for the 14 nH spiral inductor is shown in Figure
6.10. This indicates that the model is accurate and can be used over the intended C- and X-band frequency range up to 12 GHz and hence, can be used with confidence in the design process. The layout design for the 14 nH spiral inductor is shown in Figure 6.11.

Figure 6.10 S-parameter for 14 nH Spiral inductor over wide range frequency

Figure 6.11 Layout design for 14 nH Spiral inductor
6.4 LNA Figure of Merits

The performance of an LNA is measured in a number of figures of merit, the most prominent of which is the noise figure and gain. Other performance characteristics include return loss, stability, linearity and dynamic range. The following section discusses in details about the LNA figures of merit.

6.4.1 Power Gain

The power gain of an amplifier can be expressed using Equation 6.15 and Equation 6.16. The LNA signal flow graph for a microwave amplifier can be represented as in Figure 6.12. The transducer power gain, \( G_T \), is the most important gain and is expressed as the ratio of power delivered to the load to the power available from the source, i.e.

\[
G_T = \frac{\text{Power delivered to the load}}{\text{Power available from the source}} = \frac{P_L}{P_{AVS}} \quad \text{Equation 6.15}
\]

\[
G_T = \frac{1 - |\Gamma_2|^2}{|1 - \Gamma_{IN} \Gamma_S^*|^2} |S_{21}|^2 \frac{1 - |\Gamma_L|^2}{|1 - S_{22} \Gamma_L|^2} \quad \text{Equation 6.16}
\]

![Figure 6.12 Power reflection coefficients for a 2-port microwave network [110]](image)

The operating power gain, \( G_P \), of an LNA is defined as the ratio of the power delivered to the load to the power input to the network, and expressed by:
\[ G_P = \frac{\text{Power delivered to the load}}{\text{Power input to network}} = \frac{P_L}{P_{IN}} \quad \text{Equation 6.17} \]

\[ G_P = \frac{1}{|1 - \Gamma_{IN}|^2} |S_{21}|^2 \frac{1 - |\Gamma_L|^2}{1 - S_{22} \Gamma_L^2} \quad \text{Equation 6.18} \]

The ratio of power available from the network to the power available from a source is called the available power gain, \( G_A \).

\[ G_A = \frac{\text{Power available from network}}{\text{Power available from source}} = \frac{P_{AVN}}{P_{AVS}} \quad \text{Equation 6.19} \]

\[ G_A = \frac{1 - |\Gamma_S|^2}{|1 - S_{11} \Gamma_S|^2} |S_{21}|^2 \frac{1}{1 - |\Gamma_{OUT}|^2} \quad \text{Equation 6.20} \]

In the above expressions,

\[ \Gamma_{IN} = S_{11} + \frac{S_{12} S_{21} \Gamma_L}{1 - S_{22} \Gamma_L} \quad \text{Equation 6.21} \]

\[ \Gamma_{OUT} = S_{22} + \frac{S_{12} S_{21} \Gamma_S}{1 - S_{11} \Gamma_S} \quad \text{Equation 6.22} \]

A unilateral amplifier is one in which the reverse transmission coefficient is negligibly small, i.e. \( S_{12}=0 \). For such conditions, the Equation 6.21 and Equation 6.22 simplifies to \( \Gamma_{IN} = S_{11} \) and \( \Gamma_{OUT} = S_{22} \). The unilateral transducer power gain, \( G_{TU} \), from Equation 6.16 therefore, be written as:

\[ G_{TU} = \frac{1 - |\Gamma_S|^2}{|1 - S_{11} \Gamma_S|^2} |S_{21}|^2 \frac{1 - |\Gamma_L|^2}{1 - |1 - S_{22} \Gamma_L|^2} \quad \text{Equation 6.23} \]

To achieve maximum gain of an amplifier, the input and output ports must be conjugately matched i.e. \( \Gamma_S = \Gamma_{IN}^* \) and \( \Gamma_L = \Gamma_{OUT}^* \).
6.4.2 Noise Figure

The Noise Figure (NF) describes the signal-to-noise degradation due to a noisy microwave component. The noise figure is defined as the ratio of the total available noise power at the output of the amplifier to the available noise power at the input due to thermal noise from the input termination. The noise figure, NF, can be expressed as in Equation 6.24 in terms of: (a) the signal to noise ratio at the input and output, SNR_i and SNR_o of the components and (b) total available power at the output of the amplifier, P_No, noise power due to the input termination, P_Ni, and G_A is the Available Power Gain:

\[ F = \frac{SNR_o}{SNR_i} = \frac{P_{No}}{P_{Ni}G_A} \]

Equation 6.24

Alternatively, noise figure can be calculated using the expression,

\[ F = F_{\text{min}} = \frac{4r_n|\Gamma_s - \Gamma_{opt}|^2}{(1 - |\Gamma_s|^2)(1 + \Gamma_{opt})^2} \]

Equation 6.25

F_{\text{min}}, r_n, and \Gamma_{opt} denotes the noise parameter which is given by the manufacturer for commercial transistors or can be derived experimentally from the fabricated device. In many cases, in order to achieve the minimum noise figure, \( \Gamma_s = \Gamma_{opt} \) condition is chosen. However in a practical design, one has to sacrifice either to achieve for minimum noise figure or for the maximum gain. Therefore, the reflection coefficient, \( \Gamma_s \) can be selected to compromise between the Noise Figure and Gain performance.
3.3.1 Stability

In any LNA circuit design, it is mandatory for the designer to achieve unconditionally stable circuit at a complete range of frequencies where the device has a substantial gain. Stability is the measure of a device to avoid oscillations. Oscillations may arise in a device at a set of frequency band(s) for a certain DC bias, if either the input or output port impedance has a negative real part i.e. \(|\Gamma|_{IN} > 1\) or \(|\Gamma|_{OUT} > 1\). In a two port network, i.e., S-parameter for pHEMT device shown in Figure 6.13, the following condition must be satisfied by the source and load impedances, \(\Gamma_S\) and \(\Gamma_L\) for unconditional stability:

\[
|\Gamma|_{IN} = \left| S_{11} \frac{S_{12}S_{21}}{1 - S_{22} \Gamma_L} \right| < 1
\]

Equation 6.26

\[
|\Gamma|_{OUT} = \left| S_{22} \frac{S_{12}S_{21} \Gamma_S}{1 - S_{11} \Gamma_S} \right| < 1
\]

Equation 6.27

![Microwave 2-port network diagram](image)

Figure 6.13 Reflection coefficients for a general microwave 2-port network

Unconditional stability means that with any load present to the output or output of the device, the circuit will not become unstable (will not oscillate). An unstable circuit is primarily caused by three phenomena; the internal feedback of the transistor, external feedback around the transistor caused by external circuit, or excess gain at frequencies outside of the band of operation [43].
The S-parameter of a transistor device is used with numerical analysis to calculate the Rollett Stability Factor (K-factor). When K-factor is greater than unity, the circuit will be unconditionally stable for any combinations of source and load impedance.

\[
K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1
\]

Equation 6.28

and

\[
|\Delta| < 1
\]

Equation 6.29

where

\[
\Delta = S_{11}S_{22} - S_{12}S_{21}
\]

Equation 6.30

When K-factor is less than unity, the circuit is potentially unstable and oscillation may occur with a certain combination of the source and /or load impedance present of the transistor. The K-factor represents a quick check for stability at given biasing condition. A sweep of the K-factor over frequency for a given biasing point should be performed to ensure unconditional stability outside of the band of operation.

6.5 LNA Design Specifications

An optimal LNA design must have low NF, high gain, wide bandwidth, low power dissipation, compact size and must be unconditionally stable over the desired frequency range. Proper selection of network topology and the frequency of interest are key to the LNA circuit design. For this project, two frequency ranges are selected; 4 - 8 GHz (C-band LNA) and 8.0 - 12 GHz (X-band LNA). An accurate model, biasing technique and circuit topology are crucial to achieve very low noise (∼ NF_{min} of the transistor). Although HEMT technologies alone cannot meet all of these requirements simultaneously [28], the LNA can be designed to meet most of the system requirements.

The most critical parameter, NF depends on the correct selection of the active device, in this case the 0.25 µm gate length XMBE131 pHEMT. The noise figure is targeted to be better than 1 dB over a very wide range of frequencies in the band of interest. However, for higher frequency band i.e X-band LNA design, higher NF is
expected. The LNA must also provide stable gain and small signal loss over the entire operating bandwidth. The LNA circuit gain in this project was chosen to be at a moderate range of around 25 dB to 35 dB. The upper gain value is to prevent the circuit from oscillating, which commonly happens in very high gain circuits. Input and output return losses are specified to be better than -5 dB.

6.6 MMIC LNA Circuit Design

The design process includes selection of a proper device, stability check of the device, biasing, and design of matching networks. One of the most practical approaches for improving the overall performance of the LNA is by selection of the most appropriate active device, which has an optimized epitaxial layer structure and biasing conditions (from optimised non-linear pHEMT model). Then, the topology profile which provides the best combination of performance is selected. Device size will affect the LNA's bandwidth, DC power consumption, noise figure and nonlinear performance. As the device gets smaller, resistive losses for matching circuits and interconnections will increase relative to the device impedance, effectively increasing the noise figure.

Device size greatly impacts the MMIC LNA performance mainly in the noise level and amplifier gain. The direct correlation can of this is due to $I_{\text{DSS}}$ is proportional to device size; bigger device consumes relatively high current compared to a smaller device. Generally, $I_{\text{DSS}}$ biasing at 15% - 20% set the trading off of gain to noise temperature. Although device size selection is crucial, however, in this project only the in-house fabricated 2x50 $\mu$m$^2$ gate width pHEMT is selected to be implemented in the LNA design. An advanced designing system (ADS 2009) tool is used to design a two stage MMIC LNA circuit; the first stage is for minimum noise figure and the second stage is designed to achieve maximum gain.
6.6.1 Active Device

One of the most practical approaches for improving the overall performance of the LNA is by the selection of the appropriate active device; which has an optimised epitaxial layer structure and biasing conditions. In this project, the active device is selected from the novel high breakdown, low leakage current InGaAs/InAlAs/InP pHEMTs which have been developed and fabricated using conventional optical lithography at the University of Manchester [96][140]. The epitaxial layer structure has been presented in section 5.2 of Chapter 5. Initially, the fabrication work had been focussed on the one micron pHEMT structure which was optimised and grown on the VMBE2100 sample. The advanced epitaxial layer offers better gate leakage performance, due to its wider bandgap material in the supply layer and also showed better thermal stability when compared to other fabricated device i.e. XMBE144, XMBE171 [96][98][141]. As an extension to the successful fabrication of this device, the submicron devices namely XMBE131 and VMBE1998 have been produced using optical lithography and reflow processes, which will help the LNA design to meet the low noise requirement at high frequency operation.

6.6.2 LNA Topology

In the LNA design, the important goals are minimizing the noise figure of the amplifier [26], producing higher gain, low power consumption and producing stable 50 Ω input impedance. To achieve all these goals, different LNA architectures are available. Several circuit design techniques have demonstrated their robustness, such as the capacitive peaking technique, the inductive peaking technique, the common-gate (CG) input configuration, and the common-drain (CD) input configuration [29]. The Figure 6.14 shows a few LNA topology available for LNA circuit design with a single transistor (Single stage LNA) or double stage LNA (cascaded single stage LNA) as in Figure 6.14 (b) - (d).
Note that the common-gate (CG) and common-drain (CD) input configurations relax the effect of large input parasitic capacitance better than the conventional common-source (CS) input. The inductive peaking topology can offer higher bandwidth, however, compromise of higher NF compared to a single stage amplifier. The schematic diagram of inductive peaking is shown in Figure 6.15.
The CS amplifier is implemented in the design which has a noise measure close to the transistor’s $\text{NF}_{\text{min}}$ measure over the wide bandwidth. The disadvantage of the common source configuration is that it suffers from a lack of gain flatness as the gain is very high at low frequency and tends to be very low at high frequency. This disadvantage can be corrected by using a proper matching network in the LNA designs and biasing on Common-Source (CS) configurations on both stages to provide good RF survivability and good linearity.

### 6.6.3 Biasing Network

The drain bias current affects the noise figure more as compared to the drain voltage. Additionally, drain bias also affects the amplifier gain. With insufficient current, gain will be low. A graph of an operating bias point for HEMT is shown in Figure 6.16. Typically, LNAs are biased in Region I at 15 to 20 % of the drain saturation current ($I_{\text{DSS}}$) as a compromise between gain and noise [43]. This also to improve the noise performance.

![Figure 6.16 Graph of typical I-V characteristic and operating bias point for HEMT](image)

For the maximum gain, transistor is biased at Region II where $V_{\text{GS}}$ is close to 0 V. Region III biases the transistor in the middle of I-V curves and allows the amplifier
to work linearly. Region IV is biased for maximum efficiency with an increased $V_{DS}$ and $\sim 40\%$ of $I_{DSS}$. Since only a small amount of current is required for efficient biasing, this bias condition is a good choice in order to maintain low-power dissipation. The $I_{DSS}$ scales with device size, so a larger device will consume more power than a smaller device. By reducing the device size while maintaining the $I_{DSS}$ bias, DC power consumption can be reduced. As a result of improper network biasing, the LNA will oscillate or the noise will increase.

A DC biasing network using an inductor as bias chokes is displayed in Figure 6.17. The DC blocking capacitors are used at the input and the output bias circuit to isolate the bias. The decoupling capacitors are used to prevent the leakage of RF signals into the power supplies. These DC blocking and decoupling capacitors are crucial, especially with regard to the circuit layout, since leakage from either the power supplies or RF signal can cause the circuit to behave incorrectly. This bias network can be modified as a high resistor biasing circuit by substituting the chokes with a high value resistor.
Matching Network

Matching circuits are designed using a simulator and the appropriate device model. An amplifier must be unconditionally stable which can be designed with a proper matching network and terminations [16]. The optimized scattering coefficients of XMBE131 pHEMT were determined to design the input/output matching network. The input circuit should match to the source and the output circuit should match to the load in order to deliver maximum power to the load. Input/output matching circuit is essential to reduce the unwanted reflection of signal and to improve efficiency of the transmission from source to load [32]. The general input/output circuit for an LNA is shown in Figure 6.18.

![Figure 6.18 General Input and output circuit of 2-port network](image)

Where, $\Gamma_{in}$ and $\Gamma_{out}$ indicates reflection coefficient of load at the input port and output port of 2-port network while $\Gamma_s$ is reflection coefficient of power supplied to the input port and $\Gamma_L$. The noise figure of the first stage of the receiver overrules noise figure of the whole system. To get minimum noise figure using transistor, power reflection coefficient should match with $\Gamma_{opt}$ and load reflection coefficient should match with $*\Gamma_{out}$. The calculation of these coefficients can be found using:

$$\Gamma_{out} = \Gamma_L^* = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1-S_{11}\Gamma_S} \quad \text{Equation 6.31}$$

$$\Gamma_{in} = \Gamma_S^* = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1-S_{22}\Gamma_L} \quad \text{Equation 6.32}$$

$$\Gamma_S = \Gamma_{opt} \quad \text{Equation 6.33}$$
\[ \Gamma_L = \Gamma_{out}^* = S_{22} + \frac{S_{12} S_{21} \Gamma_S}{1 - S_{11} \Gamma_S} \]  

Equation 6.34

A lossless matching network on both sides of the transistor must be designed to transform the input and output impedance, \( Z_0 \) to the source and load impedance, \( Z_S \) and \( Z_L \) required in the design specifications.

6.7 MMIC LNA Design for C-band Frequency (4-8 GHz)

The proposed MMIC LNA is designed based on the s-parameters obtained from ADS circuit simulation tools. Table 6.2 shows the target specification of the LNA design and compared to other LNA designs reported in the literature for the same frequency range. The single stage single-ended (SSLNA) MMIC LNA is shown in Figure 6.19. The LNA was designed for a frequency range of 4 - 8 GHz, with optimum performance up to 5.8 GHz. The active device used was the 2 x 50 μm depletion mode pHEMT fabricated on sample XMBE131. The design includes on-chip matching network.

<table>
<thead>
<tr>
<th>S-parameter (dB)</th>
<th>Freq. (GHz)</th>
<th>Center freq. (GHz)</th>
<th>( S_{11} ) (dB)</th>
<th>( S_{12} ) (dB)</th>
<th>( S_{21} ) (dB)</th>
<th>( S_{22} ) (dB)</th>
<th>NF (dB)</th>
<th>K</th>
</tr>
</thead>
<tbody>
<tr>
<td>This work (SSLNA)</td>
<td>4-8</td>
<td>5.8</td>
<td>-12</td>
<td>&lt; -15</td>
<td>&gt; 10</td>
<td>&lt; -10</td>
<td>&lt; 1.5</td>
<td>&gt; 1</td>
</tr>
<tr>
<td>SSLNA [143]</td>
<td>Bandwidth BW=1.24</td>
<td>5.8</td>
<td>-12.8</td>
<td>-20.2</td>
<td>17</td>
<td>-10.1</td>
<td>1.2</td>
<td>1.02</td>
</tr>
<tr>
<td>This work (DSLNA)</td>
<td>4-8</td>
<td>5.8</td>
<td>-15</td>
<td>&gt;10</td>
<td>&gt;25</td>
<td>&lt; -10</td>
<td>&lt; 1.5</td>
<td>&gt; 1</td>
</tr>
<tr>
<td>Cascode &amp; cascade [143]</td>
<td>Bandwidth BW=1.24</td>
<td>5.8</td>
<td>-11.4</td>
<td>-42.5</td>
<td>36.3</td>
<td>-27.7</td>
<td>1.20</td>
<td>1.59</td>
</tr>
</tbody>
</table>
The active device was biased at $V_{GS}=1 \text{ V}$, $13 \text{ mA} \ I_{DS}$ (90% $g_m$ or 20% $I_{dss}$) and $3 \text{ V} \ V_{DS}$. The transistor was biased with Common-Source (CS) configuration to provide good voltage gain and provides low NF by selection of a proper matching network. The DC bias network utilises a high gate resistor value, preferably to achieve unconditional circuit stability while the drain side of the LNA is designed to use only a single low value of inductor and resistor, without compromising the output return loss [14].

This topology prevents a large current flowing to the input gate of the transistor, and hence the optimum DC gate voltage is injected to the transistor ($V_{GG} = -0.52 \text{ V}$). Therefore, the transistor was biased for optimum low noise performance. The increased gate resistance can also minimise the oscillation at low frequency.

The series capacitor, $C_i$ at the input terminal acts as a DC-block to isolate the DC signal from the DC source, $V_{GG}$, to the RF input. The coupling capacitor, $C_{dc}$, prevents RF leakage to the DC sources. The drain capacitor, $C_1$, was used to improve the input return loss, as well as to provide output matching for the amplifier. The resistor located at the drain side, $R_1$, prevents oscillations. Since this resistor is placed at the output side of the LNA, it will not affect the noise. However, it can slightly reduce the overall gain of the amplifier. Therefore, to minimise the gain loss, the value of $R_1$ was minimised which in the design, $R_1$ is a 40 $\Omega$ resistor.
The drain inductor, \( L_1 \), and drain resistor, \( R_2 \), was used to provide an adequate output match over the wide frequency band, and hence ensure the unconditional stability of the LNA. The use of spiral inductors at the source of an active device can improve the input return loss. However, due to their internal resistance, the noise is degraded. For this reason, the use of spiral inductors was avoided for the critical paths. The output capacitor, \( C_o \), is a DC-block to the drain current, and behaves as an output matching network for the output return loss.

The simulation recorded that the amplifier gain \( S_{21} \) is \( \sim 10 \text{dB} \). The input insertion loss \( S_{11} \) was 10.3dB, overall noise figure (NF) is 1.2dB at 5.8 GHz and the output insertion loss, \( S_{22} \) is -13.8dB. The reflection loss, \( S_{12} \) is 25dB. These values were within the design specification and were acceptable. The output s-parameter and noise figure results are shown in Figure 6.20.

In the SSLNA design, minimum noise figure is achieved. However, the gain for this configuration is also small. Therefore, to improve the gain, the second transistor is cascaded in series with the first which results in a double stage LNA (DSLNA) as shown in Figure 6.21.
The double staged single-ended MMIC LNA is designed to improve the gain and optimise the noise performance. The first LNA stage is biased near the lowest $\text{NF}_{\text{min}}$, which for this process was $\sim 0.4 \text{ dB}$ for $V_{\text{gs}}=-0.52\text{V}$ and $I_{\text{ds}}=13.2\text{mA}$ as NF of the first stage dominates the noise performance of the entire design (as well as its sensitivity). Therefore, the second stage was biased to optimise the gain and matching is done by adding a capacitor between these two stages. The circuit is terminated with $50\ \Omega$ impedance and the component’s value, biasing voltage and supply voltage are given in Table 6.3.

![Double Stage LNA circuit for 4-8 GHz frequency range](image)

Table 6.3 Component values used in C-band DSLNA design

<table>
<thead>
<tr>
<th>Component</th>
<th>Value used in design</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Capacitor, $C_i$</td>
<td>35.15 pF</td>
</tr>
<tr>
<td>Output Capacitor, $C_o$</td>
<td>4.5 pF</td>
</tr>
<tr>
<td>Coupling Capacitor, $C_{dc}$</td>
<td>15.4 pF</td>
</tr>
<tr>
<td>Inter-stage Capacitor, $C_M$</td>
<td>9.6 pF</td>
</tr>
<tr>
<td>Gate Inductor, $L_G$</td>
<td>2.66 nH</td>
</tr>
<tr>
<td>Gate Resistor $R_{G1}, R_{G2}$</td>
<td>8200 $\Omega$</td>
</tr>
<tr>
<td>Drain Resistor, $R_D$</td>
<td>230 $\Omega$</td>
</tr>
<tr>
<td>Supply Voltage, $V_{DD}$</td>
<td>3 V</td>
</tr>
<tr>
<td>Bias Voltage, $V_{GG}$</td>
<td>-0.52 V</td>
</tr>
</tbody>
</table>

The capacitor ($C_M$) and resistor ($R_{d1}$) act as the inter-stage matching network of the LNA. Additionally, $C_M$ is used to isolate the gate DC supply of the second stage from the RF output of the first stage.
The DSLNA design results in amplifier gain, $S_{21}$ of 26dB. The input insertion loss, $S_{11}$ is 21dB, overall noise figure (NF) is 1.15 dB at 5.8 GHz, the output insertion loss, $S_{22}$ is -11.2dB and reflection loss, $S_{12}$ is 25dB. The circuit is very stable with stability factor of 2.9. Overall, these values are acceptable and in line with the specification in Table 6.2. Figure 6.22 shows the s-parameter results for the DSLNA circuit design.

![Forward Coefficient](image1)

![Reflection Coefficient](image2)

![Gain and Stability](image3)

Figure 6.22 The gain, input and output reflection results for C-band Double-stage LNA
6.8 MMIC LNA Design for 8-12 GHz (NF @ 8.4 GHz)

Circuit design method of the X-band LNA is similar to RF circuit design techniques where lumped elements are employed for matching networks. The noise figure is kept at minimum since noise figure is an important metric for a satellite receiver. This amplifier normally used in the first stage of a receiver array for the X-band wireless communications service (WCS) and industrial, scientific, and medical (ISM) frequencies [144]. In the X-band LNA, design of a new input matching network is proposed that obviates the need of the gate inductance [144]. The gate inductance is an important noise contributor due to its finite quality factor, a resistance appears in series with (R_s), adding directly to the noise of the system. The X-band LNA was design based on the following performance criteria listed in Table 6.4.

<table>
<thead>
<tr>
<th>S-parameter (dB)</th>
<th>Device size</th>
<th>Freq. (GHz)</th>
<th>Center freq. (GHz)</th>
<th>S_11 (dB)</th>
<th>S_12 (dB)</th>
<th>S_21 (dB)</th>
<th>S_22 (dB)</th>
<th>NF (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>This work (SSLNA)</td>
<td>L_g=250nm 2x50μm</td>
<td>8-12</td>
<td>8.4</td>
<td>-12.8</td>
<td>-20.2</td>
<td>&gt; 10</td>
<td>&lt; -10</td>
<td>&lt; 1.5 @ 8.4 GHz</td>
</tr>
<tr>
<td>SSLNA [145]</td>
<td>L_g=100nm 2x50μm</td>
<td>7-11</td>
<td>9.8</td>
<td>-11.3</td>
<td>-</td>
<td>9 ±0.9</td>
<td>-10.1</td>
<td>1.48 @ 9.8 GHz</td>
</tr>
<tr>
<td>This work (DSLNA)</td>
<td>L_g=250nm 2x50μm</td>
<td>8-12</td>
<td>8.4</td>
<td>&lt; -12.8</td>
<td>-20.2</td>
<td>&gt; 20</td>
<td>&lt; -15</td>
<td>&lt;2</td>
</tr>
<tr>
<td>DSLNA [146]</td>
<td>L_g &lt; 200 nm W=160 μm</td>
<td>7.8 - 9.4</td>
<td>8.6</td>
<td>-26</td>
<td>-</td>
<td>&gt; 30</td>
<td>-27</td>
<td>&lt; 0.6</td>
</tr>
</tbody>
</table>

The single stage single-ended (SSLNA) MMIC LNA for the frequency range of 8 - 12 GHz, with center frequency set at 8.4 GHz is shown in Figure 6.23. The optimised s-parameter is obtained from the 2 x 50 μm XMBE131 pHEMT sample. The active device was also biased at V_GS=-0.52V, 13mA I_DS (90% g_m) and the source-drain voltage, V_DS of 3 V. The NF_min calculated for the XMBE131 pHEMT at the frequency of 8 GHz is ~0.5 dB.
Figure 6.23 Single Stage circuit for 8-12 GHz frequency range

Figure 6.24 Gain, Noise figure and Input/output reflection results for SSLNA at 8-12 GHz frequency range

The simulation recorded that the amplifier gain, $S_{21}$ is ~10dB and flat gain is maintained in the frequency range. The input insertion loss, $S_{11}$ was 2.9dB, overall noise figure (NF) is 1.9dB at 8.4 GHz and the output insertion loss, $S_{22}$ is -11.25dB.
The reflection loss, $S_{12}$ is 20dB. These values were within the design specification, except for very low input insertion loss. The output s-parameter and noise figure result is shown in Figure 6.24.

To improve the output gain and noise performance, a double staged single-ended X-band MMIC LNA is designed. The design topology without inductor at the drain side is similar to the C-band DSLNA as this design compromises the noise figure and high gain performance. This LNA is using the same biasing configuration as employed in the SSLNA X-band design where $V_{gs}=-0.52$ V and $I_{ds}=13.2$ mA. The DSLNA for X-band LNA is presented in Figure 6.25.

![Figure 6.25 Double Double Stage LNA (DSLNA) circuit for 8-12 GHz frequency range](image)

The DSLNA design results in an overall gain, $S_{21}$ of 20dB. The input insertion loss, $S_{11}$ is 29dB, overall noise figure (NF) is 1.9 dB at 8.4 GHz, the output insertion loss, $S_{22}$ is -11.3dB and reflection loss, $S_{12}$ is ~41 dB. The circuit stability factor is 4.6. Overall, these values are acceptable as what has been expected in the specification in Table 6.4. Figure 6.26 presents the s-parameter results for the DSLNA circuit design.
Figure 6.26 Maximum Gain, Noise Figure, Stability factor, and input and output reflection results for DSLNA operating at 8-12 GHz
6.9 Summary

The simplest topology for the MMIC LNAs which is designed in the C-band (4–8 GHz) and X-band (8–12 GHz) described in this chapter meets the project specifications of: high gain, unconditional stability, low power dissipation, and most fundamentally, low noise figure. The design is optimised using Common-Source configurations. The simulation results of the two stages LNA design for C-band and X-band is acceptably reaching all the target specifications. For both designs, the first stage was designed for low NF and the second stage is to provide high gain.

The MMIC LNA design was optimized for operation at the drain voltage of 3 V and biased at $V_{GS}=-0.52$ V and $I_{DS}=13.2$ mA. For C-band LNA, the simulation results recorded that the overall amplifier gain, $S_{21}$ is 26 dB. The input insertion loss, $S_{11}$ is 21 dB, noise figure (NF) is 1.15 dB at 5.8 GHz, the output insertion loss, $S_{22}$ is ~11.2 dB and the reflection loss, $S_{12}$ is 25 dB. The circuit is very stable with a stability factor of 2.9. In the X-band MMIC LNA design, the overall amplifier gain $S_{21}$ is ~20 dB. The input insertion loss $S_{11}$ was 29 dB, overall noise figure (NF) is 1.9 dB at 8.4 GHz and the output insertion loss, $S_{22}$ is ~11.3 dB. The reflection loss, $S_{12}$ is ~41 dB. However, some improvement might be done in the X-band LNA design to boost the overall gain performance i.e using inductive peaking or inductive degenerative technique to improve all the target specifications.
7 CHAPTER 7

MODELLING OF ADVANCED In$_{0.7}$Ga$_{0.3}$As/AlAs RESONANT TUNNELLING DIODE IN ATLAS SILVACO

7.1 Introduction

The simple one dimensional structure and the quantum phenomena have made resonant tunnelling diodes (RTD) very attractive and widely investigated for quantum device study. The very fast tunnelling process and its Negative Differential Resistance (NDR) unique property was first discovered by Esaki and Tsu in the 70’s [147]; This device allows a remarkable reduction in circuits’ complexity and permits ultra high speed operations. The unique property of NDR has encouraged further studies of the double barrier quantum well (DBQW) RTD to exploit its unique property in THz application [148]. Due to the small effective mass and low band offset in III-V heterostructures, high current density, large NDR and high cutoff frequency have been observed for these structures. For these reasons III-V based RTD have been extensively explored. The RTD also has a great potential in THz applications [149], i.e. oscillator, self-oscillating mixers, multiplier, etc.

While tunnelling is a critical effect, it can be difficult to model the non-unique relationship between current and the applied voltage. Continuing efforts [150][151] in quantum transport modelling of RTD’s is motivated by the need to understand device behaviour, characterisation and optimisation [151] of RTD fabricated using various types of material system i.e SiGe, InAlAs/InAs, InGaAs/InAs, etc. In this chapter, the simulation of RTD is carried out to extend the study of advanced III-V material particularly in the quantum well layer and validated with experimental results [152]. The dependence of current-voltage characteristics on structural parameters, i.e. the variable parameters are barrier and spacer thicknesses are discussed in details.
7.2 Principle of operations

Basically, an RTD device consists of an undoped quantum well sandwiched between two undoped barrier layers. The emitter and collector contact regions are heavily doped. All types of RTD use some form of electron tunnelling mechanism. Quantum tunnelling is the passing of electrons through a potential barrier which is thin compared to the electron wavelength. If the “electron wave” is large compared to the barrier, there is a possibility that the wave appears on both sides of the barrier. The strong quantum confinement between the two barriers gives rise to the quantised energy level in the well, as shown in Figure 7.1. At zero biasing, the Fermi levels in the emitter and collector are perfectly aligned, the energy levels (\(E_{r1}\) and \(E_{r0}\)) are still above the Fermi levels and current cannot flow through the double barrier.

![Figure 7.1 Schematic of RTD Structure](image)

Electrons tunnel through a well sandwiched between two barrier layers in flowing from emitter to collector. The flow of electrons is controlled by the external diode bias, \(V\). Figure 7.2 shows the conduction band of a DBQW structure for different applied voltage and the resulting conduction state of the device on the I-V characteristics. By increasing the collector bias while the emitter is kept grounded, the position of the different sub-band and Fermi levels are modified. Peak current is achieved when the emission region conduction band is at the same energy at the resonant level and most electrons tunnel from the emission region into the resonant level. From Figure 7.2, \(E_c\), \(E_f\), \(E_1\) and \(E_2\) are the conduction band, Fermi and quantisation energies respectively.
Figure 7.2 Energy band diagrams of an RTD and the corresponding IV curve [153-154]

Under zero external bias in Figure 7.2 (a), the electrons on both sides of the barriers form a Fermi-sea of electrons above the conduction band edge due to the high doping concentration of the electrodes. The quantised energy states inside the quantum well are greater than the electron Fermi energy. The energy level in the quantum well is quantized due to electron confinement in the growth direction. Consider electron flows from left to right of the barriers. With no applied external bias, the bands in Figure 7.2(a) are flat and the conduction band electrons to the left of the barrier do not have an available bound state in the well to tunnel into and no current will flow.

When a small amount of external bias is applied as in Figure 7.2 (b), the number of electrons with enough energy to overcome the barrier increases. Also, as the first resonant state is lowered to match the Fermi energy, a small amount of current starts
to flow through the diode. As the bias voltage increases further, the external bias sweeps the alignment of the electron energy to match the quantised state energy as in Figure 7.2 (c). The conduction band electrons have lined up with the lower bound state inside the well. When the energy levels are equal, a resonance occurs, tunnelling will commence - allowing more electrons to flow through the barriers resulting in a peak current ($I_{\text{peak}}$). The voltage, at which current flow is maximum, is called the peak voltage ($V_{\text{peak}}$). When the first resonant energy falls below conduction band offset as shown in Figure 7.2 (d), the current drops (ideally to zero) due to off resonance condition with an increase of voltage.

In Figure 7.2 (e), the incident electrons are now above the bound state and the current will reduce to the valley current ($I_{V}$) with corresponding valley voltage ($V_{\text{valley}}$). Current will keep reducing with an increase in voltage until other mechanisms take place. The current will then increase rapidly above $V_{\text{valley}}$. With an increase in voltage, the population of electrons with high enough kinetic energy to tunnel through the barrier increases, hence current starts to rise. At this point, with an increase in voltage, current flow is determined mainly by thermionic emission over the barrier as depicted in Figure 7.2 (f).

7.3 Current-Voltage Characteristics

The tunnelling effects in semiconductor lead to a phenomenon called the negative differential resistance. This was first suggested by Tsu and Esaki in 1973 [147]. At large biases, current flow follows thermal diffusion current characteristics similar to that of traditional diodes. However, there are several large deviations in current flow at small and reverse biases. There are three basic parameters used to characterize tunnel diode characteristics; namely (i) the peak, (ii) the valley, and (iii) the peak-to-valley current ratio (PVCR) as shown in Figure 7.3.
Figure 7.3 Generic I-V characteristic of an RTD, showing peak and valley characteristics [155]

The peak and valley voltages are referred to as $V_p$ and $V_v$, respectively. The peak and valley currents ($I_p$ and $I_v$) are often divided by the cross-sectional area ($A$) to obtain the effective current density, $J_p$ and $J_v$ of the devices [154]. Ideally, $J_p$ and $J_v$ are independent of device geometries. Ideally, to have a large peak-to-valley-current ratio (PVCR), the peak current, $I_p$ must be large while the valley current, $I_v$ must be small.

$$PVCR = \frac{I_p}{I_v}$$  \hspace{1cm} \text{Equation 7.1}

The PVCR is an important figure of merit of RTD for both analog and digital application. In particular for memory and logic functions a large PVCR is suitable to choose operation points and in order to optimize noise margins. In addition, switching applications also require large PVCR, as a small valley current is needed to minimize the off state power dissipation [140]. A high peak current is required for high speed applications and for many analog applications in order to ensure high output power. However, too large peak current, $I_p$ might contribute to high power dissipation. This can be compensated by designing RTD with very low peak voltage, $V_p$ [152]. Large NDR is suitable for digital applications (memory, analog to digital converter, logic circuits, etc.) and analog application (as oscillators) that exploit the natural instability of RTD in this region.
The negative differential conductance, $G_d$ can provide the gain necessary to sustain oscillation. Together with a small device capacitance and small intrinsic delay, the RTD can oscillate at very high frequency.

$$G_d = \frac{1}{R_d} = \frac{|I_P - I_V|}{|V_P - V_V|}$$

Equation 7.2

To obtain high RF output power, the $\Delta I$ ($I_P - I_V$) and $\Delta V$ ($V_P - V_V$) must be made as large as possible. Understandably, in practical circuit implementation, the RF power will be much less due to imperfection such as the effect of parasitic resistance and impedance mismatch.

### 7.4 RTD Device Structures

Through proper selection of material system, the performance of a particular DBQW RTD can be maximised by adjusting the barrier height and doping concentration of the contact regions [156]. Other than that, the size of the epitaxial layers, namely barrier thickness ($t_b$), quantum well thickness ($t_{qw}$), spacer thickness ($t_s$) and doping concentration [144,145,146] can be varied to optimise device capability. The relationship of these parameter thicknesses in the RTD structure with the output characteristics is discussed in the following topics.

Figure 7.4 illustrates an example of the generic DBQW studied in this project, which was grown on semi-insulating InP is grown by MBE at 430 °C at the University of Manchester [140,143]. The advanced RTD structure is formed as a single compressively strained In$_{0.8}$Ga$_{0.2}$As quantum well structure sandwiched between two very thin tensile strained barrier layers (AlAs). The other doped layers are In$_{0.53}$Ga$_{0.47}$As lattice-matched to InP semi-insulating substrate.
Figure 7.4 Generic epilayer structure of RTD using In$_{0.8}$Ga$_{0.2}$As/AlAs material system studied in this project.

7.4.1 Structure with Various AlAs barrier Thickness

The large size (3μm × 3μm) RTD device on samples XMBE230 ($t_b$=12Å, ~ 4 ML), XMBE277 ($t_b$=13 Å, ~4.8 ML), and XMBE276 ($t_b$=16Å, ~6 ML) were fabricated to investigate the effect of the barrier thickness on the I-V characteristics. In this section, only sample XMBE277 will be discussed in details. The epitaxial structures, doping concentration and layer thickness for sample XMBE277 are shown in Table 7.1. The In$_{0.8}$Ga$_{0.2}$As quantum well thickness is kept constant (45Å) for each sample while the other region such as emitter and collector regions are similar to the structure described in Table 7.1.
Table 7.1 RTD Epitaxial Structure (XMBE277, $t_b=13$ Å, 1ML ~ 2.7 Å [143])

<table>
<thead>
<tr>
<th>Region</th>
<th>Epitaxial</th>
<th>Doping (cm$^{-3}$)</th>
<th>Thickness (Å)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cap</td>
<td>$\text{In}<em>{0.53}\text{Ga}</em>{0.47}\text{As(n++)}$</td>
<td>2.00E+19</td>
<td>450</td>
</tr>
<tr>
<td>Emitter 2</td>
<td>$\text{In}<em>{0.53}\text{Ga}</em>{0.47}\text{As(n+)}$</td>
<td>3.00E+18</td>
<td>250</td>
</tr>
<tr>
<td>Spacer</td>
<td>$\text{In}<em>{0.53}\text{Ga}</em>{0.47}\text{As}$</td>
<td>undoped</td>
<td>$t_b$</td>
</tr>
<tr>
<td>Barrier</td>
<td>AlAs</td>
<td>undoped</td>
<td></td>
</tr>
<tr>
<td>Quantum Well</td>
<td>$\text{In}<em>{0.8}\text{Ga}</em>{0.2}\text{As}$</td>
<td>undoped</td>
<td>45</td>
</tr>
<tr>
<td>Barrier</td>
<td>AlAs</td>
<td>undoped</td>
<td></td>
</tr>
<tr>
<td>Spacer</td>
<td>$\text{In}<em>{0.53}\text{Ga}</em>{0.47}\text{As}$</td>
<td>undoped</td>
<td>200</td>
</tr>
<tr>
<td>Collector 2</td>
<td>$\text{In}<em>{0.53}\text{Ga}</em>{0.47}\text{As(n+)}$</td>
<td>3.00E+18</td>
<td>250</td>
</tr>
<tr>
<td>Collector 1</td>
<td>$\text{In}<em>{0.53}\text{Ga}</em>{0.47}\text{As(n+)}$</td>
<td>1.00E+19</td>
<td>4000</td>
</tr>
<tr>
<td>Substrate</td>
<td>InP</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

From Figure 7.5, the barrier height extracted is approximately 1.07 eV. All the contacts, barrier and quantum well are successfully constructed according to the structure defined in Table 7.1. The different doping concentration applied at the emitter and collector contact results in a higher energy gap at the collector region. Very high peak current density is expected due to excellent electron confinement (very high barrier).

Figure 7.5 Band diagram and doping profile for XMBE277 RTD (size $3\mu$m × $3\mu$m)
The experimental IV characteristics for the three sample device are presented in Figure 7.6. In the forward bias, the highest $I_P$ is observed in sample XMBE230 which has the thinnest barrier layer while sample XMBE267 produces lowest peak current, $I_p$. Table 7.2 summarizes the figure of merits for sample XMBE230, XMBE277 and XMBE267 [140].

![IV Characteristics for various samples RTD with different barrier thicknesses](image)

**Figure 7.6** IV Characteristics for various samples RTD with different barrier thicknesses

**Table 7.2** Peak current density and PVCR for various RTD sample [142]

<table>
<thead>
<tr>
<th>Sample</th>
<th>Barrier Thickness (Å)</th>
<th>Peak Current Density, $J_P$ (kA/cm²)</th>
<th>Peak Voltage, $V_P$ (mV)</th>
<th>Peak-to-Valley-Current Ratio PVCR</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>forward</td>
<td>reverse</td>
<td>forward</td>
</tr>
<tr>
<td>XMBE230</td>
<td>12</td>
<td>143</td>
<td>245</td>
<td>224</td>
</tr>
<tr>
<td>XMBE267</td>
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<td>735</td>
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<tr>
<td>XMBE277</td>
<td>13</td>
<td>678</td>
<td>N/A</td>
<td>644</td>
</tr>
</tbody>
</table>

### 7.4.2 RTD Structure with Various Spacer Thicknesses

One of the reasons for the inclusion of the undoped spacer is to prevent diffusion of dopants to the subsequent layer during growth, i.e. from the n- InGaAs into the AlAs barrier. With the presence of undoped spacer, the electron mean free path is clear from ionised donors. By having undoped spacer layer (or even low-doped spacer) between the contact, say emitter (negative) and barrier, under large applied bias, a
triangular well will be formed near the emitter barrier. For the relationship between spacer thickness and IV, sample XMBE301, XMBE302 and XMBE308 were fabricated. The epitaxial structure for RTD sample XMBE308 is shown in Table 7.3. This RTD structure employs very thin spacer layer (25 Å). Other sample device, XMBE301 and XMBE302 have \( t_S = 200 \) Å and \( t_S = 50 \) Å respectively. Sample XMBE308 will be used in the discussion.

<table>
<thead>
<tr>
<th>Region</th>
<th>Epitaxial</th>
<th>Doping ((\text{cm}^{-3}))</th>
<th>Thickness (Å)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cap</td>
<td>( \text{In}<em>{0.53}\text{Ga}</em>{0.47}\text{As} (n++) )</td>
<td>(2.00E+19)</td>
<td>450 C</td>
</tr>
<tr>
<td>Emitter 2</td>
<td>( \text{In}<em>{0.53}\text{Ga}</em>{0.47}\text{As} (n+) )</td>
<td>(5.50E+18)</td>
<td>250 Å</td>
</tr>
<tr>
<td>Spacer</td>
<td>( \text{In}<em>{0.53}\text{Ga}</em>{0.47}\text{As} )</td>
<td>undoped</td>
<td>( t_S ) Å</td>
</tr>
<tr>
<td>Barrier</td>
<td>( \text{AlAs} )</td>
<td>undoped</td>
<td>12 Å</td>
</tr>
<tr>
<td>Quantum Well</td>
<td>( \text{In}<em>{0.8}\text{Ga}</em>{0.2}\text{As} )</td>
<td>undoped</td>
<td>45 Å</td>
</tr>
<tr>
<td>Barrier</td>
<td>( \text{AlAs} )</td>
<td>undoped</td>
<td>12 Å</td>
</tr>
<tr>
<td>Spacer</td>
<td>( \text{In}<em>{0.53}\text{Ga}</em>{0.47}\text{As} )</td>
<td>undoped</td>
<td>( t_S ) Å</td>
</tr>
<tr>
<td>Collector 2</td>
<td>( \text{In}<em>{0.53}\text{Ga}</em>{0.47}\text{As} (n+) )</td>
<td>(5.50E+18)</td>
<td>250 Å</td>
</tr>
<tr>
<td>Collector 1</td>
<td>( \text{In}<em>{0.53}\text{Ga}</em>{0.47}\text{As} (n+) )</td>
<td>(1.00E+19)</td>
<td>4000 Å</td>
</tr>
<tr>
<td>Substrate</td>
<td>( \text{InP} )</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

For sample XMBE308 \( (t_S = 25 \) Å\), the \( I_P \) and \( V_P \) obtained are the highest at 678 kA/cm\(^2\) and 644 mV respectively in the forward-direction. As the spacer thickness increases to 50 Å, \( I_P \) and \( V_P \) voltage reduced to 434 kA/cm\(^2\) and 350 mV respectively. For the larger spacer of 200 Å, \( I_P \) reduced further to 143 kA.cm\(^2\) and \( V_P \) reduced to 224 mV. The PVCR drastically improved with increasing spacer thickness as can be seen in Figure 7.7. PVCR of 1.3 for \( t_S = 25 \) Å is increased to 4.6 for spacer thickness, \( t_S = 200 \) Å. The figures of merit for those RTD sample is summarised in Table 7.4.
Figure 7.7 IV Characteristics for various samples RTD with different spacer thicknesses

Table 7.4 Figure of merits for various RTD samples

<table>
<thead>
<tr>
<th>Sample</th>
<th>Spacer Thickness (Å)</th>
<th>Peak Current Density, $J_p$ (kA/cm$^2$)</th>
<th>Peak Voltage, $V_P$ (mV)</th>
<th>Peak-to-Valley-Current Ratio PVCR</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>forward</td>
<td>reverse</td>
<td>forward</td>
</tr>
<tr>
<td>XMBE301</td>
<td>200</td>
<td>143</td>
<td>245</td>
<td>224</td>
</tr>
<tr>
<td>XMBE302</td>
<td>50</td>
<td>434</td>
<td>735</td>
<td>350</td>
</tr>
<tr>
<td>XMBE308</td>
<td>25</td>
<td>678</td>
<td>N/A</td>
<td>644</td>
</tr>
</tbody>
</table>
7.5 Analytical Modelling for RTD

7.5.1 Basic Tunnelling Current Equations

The natural expression of tunnelling current expression can be derived from the quantum model. The standard current equation in the mass approximation is given by Equation (7.3 - 7.5). Tunnelling current is calculated by integrating the transmission electron velocity over the electron distribution in \( k \)-space. The simplified expression is given by Equation 7.5,

\[
J = \frac{em^*kT}{4\pi^2\hbar^3} \int_0^{\infty} dET(E,V) \cdot \ln \left[ \frac{1 + e^{(E_F-E)/kT}}{1 + e^{(E_r-E-eV)/kT}} \right]
\]

Equation 7.3

\[
T(E,V) = \frac{(\Gamma/2)^2}{[E - (E_r - eV/2)]^2 + (\Gamma/2)^2}
\]

Equation 7.4

\[
J = \frac{em^*kT}{4\pi^2\hbar^3} \cdot \ln \left[ \frac{1 + e^{(E_F+E_r+eV/2)/kT}}{1 + e^{(E_F-E_r+eV/2)/kT}} \cdot \frac{\pi}{2} + \tan^{-1} \left( \frac{E_r - eV}{\Gamma/2} \right) \right]
\]

Equation 7.5

Where \( \Gamma \), \( E_r \), \( E_F \), \( m^* \), \( \hbar \) and \( H \) are the resonance width, the energy in the In\(_{0.8}\)Ga\(_{0.2}\)As well resonance level, the energy of the Fermi level in two contacts, the effective mass, the reduced Plank constant and the saturation current respectively. \( E \), is the energy of the resonant level relative to the bottom of the well at its centre [138].

7.5.2 Physic-based Analytical Modelling

As an initial work to model the fabricated device, an analytical modelling was performed for the XMBE277 RTD to characterise the I-V characteristics using the physic-based current Equation 7.3 to Equation 7.5. The fitted modelling is performed for \( 2\mu m \times 0.35\mu m \) and \( 3\mu m \times 3\mu m \) RTD mesa areas. A simple curve-fitting model [138] with the tunnelling probability \( T(E) \) obtained using the Wentzel-Kramer-Brillouin (WKB) approximation. From Equation 7.5, the formulation is simplified as the following.
\[ J = J_1 + J_2 \]

\[ J_1(V) = A \ln \left[ \frac{1 + e^{\frac{(B-C+n_1) e}{kT}}}{1 + e^{\frac{(B-C-n_1) e}{kT}}} \right] \left\{ \frac{\pi}{2} + \tan^{-1}(C - n_1) \right\} \]

\[ J_2(V) = H \left( e^{\left( n_2 eV / kT \right)} - 1 \right) \]

\[ A = \frac{e m^* kT \Gamma}{4 \pi^2 \hbar^3}, \quad B = \frac{E_F}{e}, \quad C = \frac{E_r}{e}, \quad D = \frac{\Gamma}{2e} \]

\[ \Gamma = 4E_r e^{2k_rL_B} \left( kL_w + 2 \frac{k_r}{k_r} \right)^{-1} \]

This formulation successfully models the resonant current, \( J_1 \), and thermionic current, \( J_2 \). Parameters \( A, B, C, \) and \( D \) are the dependent fitting parameters based on the device’s physics. Parameters \( H, n_1 \) and \( n_2 \) cannot be obtained easily from analytical method, therefore are obtained by fitting \([138, 147]\). However, the value of parameter \( H \) is adjusted to be as close as possible to the saturation current value from experimental data. The dimensions of the double barrier quantum well (DBQW) structure is independent of parameters \( H, n_1 \) and \( n_2 \) while parameter \( B \) is expected to be constant as it depends on the temperature and doping concentration. By applying a voltage bias on the collector side, and maintaining the emitter grounded, the position of the different sub-band and Fermi levels are modified. The relation with physical dimensions of the DBQW structure and the doping concentration is shown in Equation 7.11 to Equation 7.13:

\[ k_r = \frac{\sqrt{2m^* E_r}}{\hbar} \quad \text{and} \quad k_r = \frac{\sqrt{2m^* (\Phi - E_r)}}{\hbar} \]

\[ E_r = \frac{\pi^2 \hbar^2}{3m^* L_w^2} \quad \text{and} \quad E_F = E_C - KT \ln \frac{N_C}{N_d} \]

\[ N_C = 2.5 \times 10^{19} \left( \frac{m^*}{m_0} \right)^{3/2} \left( \frac{T}{300} \right)^{3/2} \]
The fitted I-V curve for both large area and submicron area are shown in Figure 7.8. The I-V characteristics were well reproduced; particularly in the NDR region, the peak width, and also in terms of the peak and valley current values.

![Diagram](image1)

**Figure 7.8** Modelled and measured current density for sample XMBE277 (a) on large area mesa (3µmx3µm) and (b) on sub-micrometer area mesa (2µmx0.35µm)

The large area RTD has a normalised peak current density of 20 kA/cm² which occurs at a peak voltage of 140 mV, and the sub-micron RTD has a normalised peak current density of 24 kA/cm² which occurs at peak voltage of 120 mV. The PVCR for both RTDs are 5.0 and 3.8 respectively. The plateau-like region in the negative differential resistance region with sudden drop of current at about 0.3 V was not the internal characteristic of the RTD. This was caused by the low frequency bias oscillation originated from the measurement setup [156]. Therefore, in the modelling, the valley current was reproduced without the plateau-like region.
Considering this, there is a small variance in the valley current fitting in the submicron RTD as compared to the measured result. The fitting parameters used in the large area and submicron RTD models are listed in Table 7.5. The value of parameter $n_1$ affects the widening and narrowing of resonant voltage in the NDR region. Based on the analytical modelling, the resonant voltage in the NDR region is reduced by increasing the parameter $n_1$ value and vice versa. The peak current decreased by reducing parameter C and B and with lower D value. The valley current is mainly controlled by parameter $n_2$ and saturation current. Parameter D has a direct correlation with the valley current and peak current.

Table 7.5 Fitting parameters for large area and submicron RTD on sample XMBE277

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Large Area RTD</th>
<th>Submicron RTD</th>
</tr>
</thead>
<tbody>
<tr>
<td>$A$</td>
<td>$1 \times 10^4$</td>
<td>$1 \times 10^4$</td>
</tr>
<tr>
<td>$B$ (eV)</td>
<td>0.0345</td>
<td>0.0345</td>
</tr>
<tr>
<td>$C$ (eV)</td>
<td>0.0222</td>
<td>0.0225</td>
</tr>
<tr>
<td>$D$ (eV)</td>
<td>0.0052</td>
<td>0.0051</td>
</tr>
<tr>
<td>$H$ (A)</td>
<td>$3 \times 10^{-4}$</td>
<td>$2 \times 10^{-2}$</td>
</tr>
<tr>
<td>$n_1$</td>
<td>0.130</td>
<td>0.122</td>
</tr>
<tr>
<td>$n_2$</td>
<td>0.442</td>
<td>0.475</td>
</tr>
</tbody>
</table>

7.6 Physical Modelling Approach for RTD

Continuing effort in the quantum transport modelling of RTD’s is motivated by the need to understand device operation and to provide a primary test for developing theoretical tools for nanoelectronic devices. High current density in the RTD device correlates to high device speed. To realize the full capability of RTD, it is necessary to determine the relationship between peak current density and peak voltage with respect to changes in the thickness of the epitaxial layers as discussed earlier in section 7.4. The following section discusses a full physical modelling which was developed to determine the relationship of changing the well and barrier thickness, doping concentration, and barrier height for the fabricated RTD devices.
7.6.1 Quantum Tunnelling Process Simulation

Figure 7.9 shows a simple quantum tunnelling process. Quantum mechanics permits a probability of the electron being on the other side of the barrier. If the barrier is thin enough, the propagating wave in the left side can penetrate in the barrier, continue attenuated through the barrier and excite a propagating wave beyond the barrier. In the quantum modelling, this transmission probability, $T$ through the barrier can be evaluated.

![Classical view](image1)
![Quantum mechanical view](image2)

Figure 7.9  Electron particle-wave duality (quantum tunnelling)[143]

In the modelling process, the RTD device is subdivided into three distinct regions (Figure 7.10). The left and right regions with emitter and collector contacts are quasi-equilibrium regions and a central device region with double barrier structure is treated to be in non-equilibrium using the Non-equilibrium Green Function (NEGF) solver. The NEGF solver will be further discussed in section 7.6.2. The central device region is considered to be the current limiting element in the device. The left/right reservoirs are assumed to be in local equilibrium with a flat Fermi level and conductive enough to provide current without depletion of the reservoir.

![Symmetrical double barrier regions in RTD](image3)

Figure 7.10  A Symmetrical double barrier regions in RTD
For a symmetrical barrier RTD device, the wave vector, $k$, is the same in the left, right side and in the well. Around a resonant energy level $E_n$, the transmission coefficient can be approximated by a Lorentzian function [139]. The transmission coefficient is a function of energy and depends on barriers characteristics, as mass, height, through the wave vectors calculated in each regions and thickness and distance between the barriers. These parameters are defined and optimised in DECKBUILD [80] to model the RTD device and reproduce the IV characteristics. For Sample XMBE308, the DECKBUILD file is given in APPENDIX F.

7.6.2 Non Equilibrium Green Function (NEGF)

The physical modelling for RTD device samples are developed in ATLAS SILVACO using one dimensional (1D) planar Non Equilibrium Green Function (NEGF) [80] which computes carrier density, I-V characteristics and energy dependent quantities such as transmission, DOS, and carrier density spectrum. NEGF takes into account the wave nature of electron in both transport and transverse directions, makes it different from the drift-diffusion or Boltzmann Transport equation, which treat electron classically. This fully quantum method treats such effects as source-to-drain tunnelling, ballistic transport, quantum confinement on equal footing [80]. A Schrödinger equation is first solved in each slice of the device to find eigen energies and eigen functions. Then, a transport equation of electrons moving in the sub-bands is solved with only a few lowest eigen sub-bands are occupied (the upper sub-bands can be safely neglected).

In the MODELS statement, N.NEGF_PL1D or P.NEGF_PL1D or both models is specified for electrons and holes respectively. This is defined to tell ATLAS to solve 1D NEGF equation in the first slice in transport direction and copy carrier and current density to all other slices. If the slices are not equivalent, use N.NEGF_PL or P.NEGF_PL or both instead to solve 1D NEGF equation for each slice separately. The EIG.YMIN and EIG.YMAX parameters on the models statement is activated to choose the states localized in this region [161]. The quasi-equilibrium regions are specified by employing the EQUIL.NEGF on the MODELS or the REGION statements. Specifying all regions in front of the first barrier and behind the last barrier as quasi-equilibrium is done to fill all possible quasi-bound states [75].
Quasi-equilibrium regions are characterized by a broadening, which can be set by ETA.NEGF parameter on the MODELS or the REGION statements with default value of 0.0066 eV [75]. Physically, the broadening corresponds to inelastic electron-phonon scattering [161], and is necessary to fill the emitter quasi-bound states. The output quantities of interest are the IV characteristics, spectrum of transmission, DOS, density and current and also spatial profiles of carrier density and conduction or valence band. The resonances can be seen as extremely narrow peaks in the transmission vs. energy plot. Use log scale in TONYPLOT to get a better understanding of the position of the transmission and DOS resonances. In case of poor convergence, energy grid size (ESIZE.NEGF on the MODELS statement) and magnitude of the broadening in quasi-equilibrium regions have to be increased.

7.6.3 Mass Approximation

For the sample XMBE277 structure, the AlAs barriers are 1.3nm wide layers separated by a 4.5nm In$_{0.5}$Ga$_{0.2}$As well. The two-band model is employed for the holes. The material parameters are set on the MATERIAL statement using parameters MHH, MLH for effective masses and DEV.HH and DEV.LH for band off-sets. The hole effective masses were taken with the following values: $m_c$(AlAs) = 0.268, $m_{lh}$(AlAs) = 0.1, and $m_{hh}$(AlAs) = 0.76 while $m_c$(InGaAs) = 0.041, $m_{lh}$(InGaAs ) = 0.05 and $m_{hh}$(InGaAs ) = 0.59. In addition to the lower mass, the light holes also have lower confinement barriers [162]. Both these factors make their confinement in the well less perfect.

7.7 Results and Discussion

The modelling is performed for various structure variation i.e spacer thicknesses, barrier thickness [144] and presented in [46] is the influence of doping concentration in RTD barriers and on IV-characteristics. The results and discussion for the modelled RTD sample XMBE277, XMBE308, XMBE302, and XMBE301 are presented in the following sections.
7.7.1 Modelling with Spacer Thickness (tₘ) variations

One of the reasons for the inclusion of the undoped spacer is to prevent diffusion of dopants to the subsequent layer during growth, i.e. from the n- InGaAs into the AlAs barrier. With the presence of undoped spacer, the electron mean free path is clear from ionised donors. By having undoped spacer layer (or even low-doped spacer) between the contact, say emitter (negative) and barrier, under large applied bias, a triangular well will be formed near the emitter barrier. Figure 7.11 depicted the spacer thickness variation in the sample XMBE277 RTD with 3µm x 3µm area. The excellent fitting at the lower bias voltage and thermionic current between measured and modelled is achieved using 20nm spacer width. However, the peak current density is very high (300mA) as compared to 200 mA for the measured data when the In₀.₅₃Ga₀.₄₇As spacer thickness is increased by 2nm (~7 ML). The model with various tₘ has a uniform Vₚ of about 0.17V (measured Vₚ=0.112 V) for the applied spacer thicknesses.

![Figure 7.11 I-V Characteristics (XMBE277 RTD) with various spacer thicknesses](image)

7.7.2 Doping Concentration

The peak current density can be modified by adjusting the doping concentration in the emitter and collector contact. A high doping concentration results in increasing of peak current density. However, it also decreases the peak to valley current ratio due to the Iᵥ increase [149]. Figure 7.12 shows the effects of varying the doping concentration in sample XMBE301. This low doping level result in a relatively wide
depletion region. Therefore, it is very difficult to match the forward current curve. However the lowest doping (in this case $3 \times 10^{18}$ cm$^3$) produces a very good tunnelling current. Increasing the doping concentration up to $8 \times 10^{18}$ cm$^3$ (plotted in dash line) and higher doping would fit the thermionic current curve. Unfortunately, this would change the epitaxial structure profile dramatically and the band energy diagram for the XMBE301 RTD. The modelling developed for XMBE301 RTD shows that a higher doping in the contact layer is needed to achieve higher peak current density as suggested by Cheng, P [163].

![Figure 7.12](image1.png)

Figure 7.12 Modelled and measured IV for XMBE301 RTD with doping variations

![Figure 7.13](image2.png)

Figure 7.13 Modelled and measured IV for XMBE301 RTD with doping variations
The same method was applied for the modelling of XMBE302 device (spacer=50Å). Increasing the doping from $4 \times 10^{18}$ cm$^3$ to $5 \times 10^{18}$ cm$^3$ increased the current from 3.8 mA to 4.86 mA. The thermionic current is in good agreement with the measured one. The current density of XMBE302 RTD with the doping variation is shown in Figure 7.13.

7.7.3 Modelling with Barrier Thickness ($t_b$) Variations

To understand the dependence of current density on barrier thickness, $t_b$, it is worthy to employ a quantum mechanical point of view. The resonant tunnelling current through a double barrier quantum well structure depends on the transmission probability, $T$ [142]:

$$T \propto e^{-2Kt_b} \quad \text{Equation 7.14}$$

where the wave vector inside the barrier is given by,

$$K = \sqrt{\frac{2m_bV}{\hbar^2}} \quad \text{Equation 7.15}$$

$m_b$ is the electron effective mass in the barrier at energies close to the conduction band edge of the emitter while $V$ is the potential barrier. By having thinner barrier, the transmission probability of the electron increases. This translates into higher current density of the RTD as can be observed from Figure 7.14. The peak voltage, $V_P$ increases with an increase in RTD current as a result of series resistance. However, the increase is not significant as the variation of peak voltage in the symmetrical barrier is thought to be more dominated by the parasitic resistance as suggested by Moise et.al [146]. From Figure 7.14, increasing of the barrier thickness by 1Å has significantly reduced the peak current density by about 20% (from 5 mA for $t_b = 9$ Å to 6.1 mA for $t_b = 8$ Å).
To validate that the barrier thickness plays a significant effect on RTD device, the modelling with \( t_b \) is also performed for other devices, i.e submicron RTD sample XMBE308. The barrier thickness for XMBE308 structure is also modified and optimised to achieve an excellent fit between modelled and measured current densities. This is shown in Figure 7.14. Reducing the barrier thickness from 9 Å to 8.5 Å in the submicron device gives a significant increase in peak current density from 4.8 mA to 5.7 mA. This also reduces the valley current which in turn gives a higher PVCR performance.

Figure 7.14  I-V Characteristics (XMBE302 RTD) with various barrier thicknesses

![I-V Characteristics (XMBE302 RTD) with various barrier thicknesses](image)

Figure 7.15  I-V Characteristics (XMBE308 RTD) with various barrier thicknesses

![I-V Characteristics (XMBE308 RTD) with various barrier thicknesses](image)
Further decreasing the barrier thickness layer has optimised the modelling for XMBE308 RTD device. The excellently fitted modelled and measured IV characteristics for this device are presented in Figure 7.16. The modelled characteristics has successfully reproduced the tunnelling and thermionic current which gives an excellent fit for the figure of merits i.e $I_p=6.4$ mA, $V_p=0.33$ V and $V_V=0.44V$.

![Figure 7.16](image)

Figure 7.16 Optimised model for XMBE308 with barrier thickness modification

### 7.7.4 Quantum Well Thickness ($t_{QW}$) effects in IV characteristics

The physical modelling for the RTD device is extended to study the correlation between quantum well thicknesses on the IV characteristics. The IV characteristics for a $2\mu m \times 0.35\mu m$ XMBE277 RTD with various $t_{QW}$ thicknesses is shown in Figure 7.17. Obviously from the plot, a thinner quantum well layer produces a higher peak current density due to more electrons being confined in the well. This however, results in the lowest thermionic current compared to the IV for the RTD with a thicker quantum well thickness. By increasing the $t_{QW}$ from the original $t_{QW}$ of 4.5 nm to 4.9 nm (~1ML), the peak current density decreases by about 35% from 0.28 mA to 0.18 mA. Decreasing the $t_{QW}$ from 4.5 nm to 4.3 nm has result in a dramatic increase in peak current density by about 50% from 0.28 mA to 0.42 mA. Hence, thinning the quantum well layer can be used to improve the peak current density of an RTD.

220
The optimisation of various samples of RTD device modelling by varying spacer thickness, barrier thickness, doping concentration and quantum well has contributes to the success of fitting the modelled and measured IV characteristics. These physical parameters which gives significant changes in the current ($I_p, I_V$) and voltage ($V_p, V_V$) have already been discussed in the previous sections and are summarised in Table 7.6. The excellent fitting of the modelled and measured IV curve can be observed in Figure 7.18.

Table 7.6 Optimised parameter value for various device structures

<table>
<thead>
<tr>
<th>Device</th>
<th>Doping concentration cm$^{-3}$</th>
<th>Spacer $t_s$ (Å)</th>
<th>Barrier $t_b$ (Å)</th>
<th>Broadening eta.negf (eV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>XMBE277</td>
<td>$3\times10^{18}$ $3\times10^{18}$</td>
<td>200</td>
<td>14</td>
<td>0.01</td>
</tr>
<tr>
<td>XMBE301</td>
<td>$4\times10^{18}$ $7\times10^{18}$</td>
<td>200</td>
<td>12</td>
<td>0.10</td>
</tr>
<tr>
<td>XMBE302</td>
<td>$3\times10^{18}$ $5\times10^{18}$</td>
<td>50</td>
<td>10</td>
<td>0.05</td>
</tr>
<tr>
<td>XMBE308</td>
<td>$5.5\times10^{18}$ $5.5\times10^{18}$</td>
<td>25</td>
<td>8.3</td>
<td>0.05</td>
</tr>
</tbody>
</table>
Figure 7.18 Optimised IV characteristics for RTD device sample:
(a) XMBE277, 1.5µm x 0.35µm, (b) XMBE301, 1.3µm x 0.7µm,
(c) XMBE302, 3.0µm x 0.4µm, (d) XMBE308, 1.5µm x 0.60µm
7.9 Summary

The parametric study for 1D physical modelling of large size and submicron In$_{0.8}$Ga$_{0.2}$As/AlAs RTD devices with variations in the spacer thickness, barrier thickness, quantum well thickness and doping concentration have been performed. The device model which was developed using the NEGF formalism was used to understand the relationship of these parameters towards DC performances. For every 1 monolayer increase in AlAs barrier thickness, the peak current density is reduced about 20 % which agrees with [142]. While for every 1 monolayer increase in spacer thickness, the peak current density is reduced by merely 2 % and peak voltage reduced by 1.5 %. By increasing the $t_{QW}$ from the original $t_{QW}$ of 4.5 nm to 4.9 nm (~1ML), the peak current density decreases by about 35% from 0.28 mA to 0.18 mA. Decreasing the $t_{QW}$ from 4.5 nm to 4.3 nm has result in a dramatic increase in peak current density by about 50% from 0.28 mA to 0.42 mA. For doping concentration variations, a higher doping translates into higher peak voltage and thermionic current. Therefore the peak current density and peak voltage in this study have a very strong dependence on barrier thickness. These DC characteristics are found to be less sensitive to variation in spacer thickness. The increase in spacer thickness, however improved the peak-to-valley current ratio (PVCR). This is attributed to low scattering as the spacer layer gets thicker.
8 CHAPTER 8

CONCLUSION AND FUTURE WORK

8.1 Conclusions

This chapter summarizes the research work in modelling and low noise amplifier (LNA) circuit design that have been discussed in details in the previous chapters. The fundamental of device physics, properties and physical models of an advanced III-V material systems are studied to establish an insightful understanding of the device physics. The device modelling for the in-house fabricated pHEMT devices with various sizes and gate lengths; namely VMBE2100, VMBE1998 and XMME131 device were successfully conducted: (1) physical modelling using ATLAS Silvaco and (2) empirical modelling performed in the ADS simulation tools. In both models, the DC and RF performances obtained from the simulations are compared with the experimental results. The deviations between the modelled and measured data are discussed and analysed.

The main goal of this research was to design and test a low noise amplifier (LNA) for high frequency microwave circuits, i.e in the C- and X-band applications. This work is an extension of the previous development of an LNA design for SKA radio telescope system operating over a frequency range of 0.4 - 1.4 GHz; which was based on a simple 1 μm gate pHEMT device. With the increasing demand for higher frequency and lower noise applications, the upper limit of 1μm gate device performance became obvious. The strained channel In_{0.7}Ga_{0.3}As/In_{0.52}Al_{0.48}As/InP pHEMT based on 0.25 μm gate length technology was chosen for use in this research due to its superior physical properties, resulting in an increased in cut-off frequency (f_T) and transconductance (g_m), which are the fundamental parameters for low noise characteristics.
The first step towards LNA design involved precise device and passive component modelling. Therefore, empirical device models were developed to accurately predict the behaviour of both active and passive devices over a wide range of frequencies under low noise condition. The precision of these models was ensured by validating them with the DC and RF results of respective devices, and further strengthened through the incorporation of the LNA S-parameters measurements into the simulation.

The empirical model for InGaAs/InAlAs/InP devices have been performed for small signal analysis (linear) and large signal analysis (nonlinear) parameters. The simulation model shows excellent agreement with the measured ICCAP data by fitting the simulation results with the DC and RF data at specified bias points over the 40 MHz to 20 GHz frequency range. The noise parameter modelling of these InP pHEMT devices is obtained through the empirical noise models given by Fukui and Pospieszalski. Comparable noise parameters have been achieved for modelled devices and these also agree with the built-in noise model of ADS. In this thesis, the optimised HEMT model for XMBE131 pHEMT device is used in the C-and X-band for single- and double-stage MMIC LNA circuit design. The passive MMIC components are designed and the most suitable biasing technique is considered to achieve the target specification of the LNA design. An inductive resistive bias mechanism was chosen which gave greater control over the device as well as the biasing components for achieving better match and stability. The simulation result shows excellent performance in the frequency range of 4 - 8 GHz and 8 - 12 GHz.

However, the underlying physical characteristics, i.e. carrier concentration, impact ionization and trapping parameters can hardly be understood and analysed in the empirical models. Hence, a two dimensional physical model of the device has been developed using ATLAS SILVACO. It provides the underlying physical simulations of the pHEMT devices. The physical model for the 2x50µm XMBE131 pHEMT device with 0.25 µm gate length employed current generation and recombination, mobility model, impact ionization and trapping mechanism to accurately model the device behaviour. An excellent agreement between the reproduced DC and RF characteristics from the simulations and the experimental results evidence that the 2-dimensional physical models are accurately developed for the pHEMT device.
Extensive physical and quantum modelling has also been performed for large size and submicron RTD devices (namely on sample XMBE277, XMBE301, XMBE302 and XMBE308). An excellent fit was achieved between experimental and physically modelled devices. A parametric study on the device structure, i.e. spacer layer, barrier layer and quantum well layer was also conducted to analyse the effects of these layer thickness effects toward the I-V characteristics of this two terminal device.

8.2 Future Work

A great deal of work has been done in both physical and empirical modelling area and also in the MMIC LNA circuit design for radio-astronomy applications. The work presented in this thesis offer the opportunities for further study in several areas. There are some suggestions of research directions and future improvements that are essential to make such a system feasible, which include:

1) A significant extension of this work would be the development of the fabrication process of the MMIC LNA circuit designs for the Single-stage (SSLNA) and Double-stage (DSLNA) in C- and X-band frequency range. This should be followed with the measurement of LNA performance characteristics, i.e. gain, noise figure and power dissipation.

2) The optimised DC and RF characterictics obtained from the physical modelling of pHEMT device in the ATLAS Silvaco could be used and integrated into an LNA circuit design. This would be possible with the MIXEDMODE; a mixed circuit and device simulator available in Silvaco [80]. The MIXEDMODE circuit simulator is very useful to simulate circuits that contain semiconductor devices with accurate physical models. This basically combines different levels of abstraction to simulate relatively small circuits where compact models for single devices are unavailable or sufficiently accurate. MIXEDMODE uses advanced numerical algorithms that are efficient and robust for DC, transient, small signal AC and small signal network analysis.
3) The physical modelling for the two terminal RTD devices has been successfully developed for DC analysis. Additionally, the quantum modelling might be extended to RF modelling and followed by RTD circuit design, eg. oscillator applications. This will lead to a better understanding of the quantum modelling of the device, as well as to ascertain the capabilities and limits of the RTD device in the Terahertz region. The RTD might well be the solution to this upcoming frequency region with its ability to provide a very high fundamental frequency well into the THz region. For example, when integrated with an optimised oscillator circuit, the RTD can potentially become a compact solid-state continuous-wave (CW) terahertz source. However, the viability of this system is beyond the scope of this study and therefore, requires further investigation.
APPENDIX A: TWO PORT NETWORK AND S-PARAMETER

The performance of a high frequency design is commonly described and represented by a two port network. It is considered as the most effective and well known approach to describe and analyse the performance of any high frequency design is through the use of a two-port network representation. A complex electrical network can be simplified by a mathematical model which represented by a two-port network. The device under test (DUT), i.e a transistor or any high frequency circuit design, is treated as a black box whereby the responses of the applied signal can be easily resolved without solving the complicated internal circuit elements. A simple diagram of the two-port network model is illustrated in Figure ---- where $V_1$ and $V_2$ is the input and output voltage at port 1 and port 2. $I_1$ and $I_2$ are the corresponding the input and output current. $Z_S$ and $Z_L$ are the source and load impedance.

![Image of two-port network model]

Figure A-1: A general representation of two-port network model

There are many different parameters available to describe the performance of the network, i.e. impedance (Z-parameters), admittance (Y-parameters), hybrid (H-parameters) and scattering (S-parameters), etc. At low frequencies, it is possible to characterise this two-port network by applying a test current or voltage at the input port whilst maintaining the output port as an open or short circuit. However, at RF and microwave frequencies, these characterisations become more difficult to determine since open and short circuits of ac signals are extremely difficult to implement [115]. Therefore, the S-parameters are preferred as they are relatively easier to measure at high frequency.
In the two-port network using S-parameters, the network is modelled as a set of incident \(a_n\) and reflected \(b_n\) signal waves travelling across the DUT, where \(n\) = port number. The relationship between \(a_n\), \(b_n\) and the corresponding port voltage \((V_n)\) and current \((I_n)\) is given by:

\[
a_n = \frac{V_n + Z_o I_n}{2\sqrt{Z_o}} = \text{Incident voltage wave on port } n
\]

Equation A-1

\[
b_n = \frac{V_n + Z_o I_n}{2\sqrt{Z_o}} = \text{Reflected voltage wave on port } n
\]

Equation A-2

Where \(Z_o\) denotes the reference impedance (normally 50Ω).

Figure A-2 shows a general representation of a two-port network. A two-port network describes the relationship between voltage, \(V_i\) and current, \(I_i\) at the input port and voltage, \(V_2\) and current, \(I_2\) at the output port.

Figure A-2: Schematic diagram of two-port network in S-parameter representation.

The relationship between the S-parameters and the travelling waves can be expressed in a matrix form (Equation A-3) and their relationship is illustrated in Figure A-2.

\[
\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix}
\]

Equation A-3
Where $S_{11}$ is the reflected signal at the input port, $S_{12}$ is reverse transmission gain, $S_{21}$ is forward transmission gain and $S_{22}$ is the reflected signal at the output port, at a matched condition as the following:

\[
\begin{align*}
\text{When } Z_L = Z_0, \ a_2 & = 0, \ S_{11} = \frac{b_1}{a_1} & \text{Equation A-4} \\
\text{When } Z_S = Z_0, \ a_1 & = 0, \ S_{12} = \frac{b_1}{a_2} & \text{Equation A-5} \\
\text{When } Z_L = Z_0, \ a_2 & = 0, \ S_{21} = \frac{b_2}{a_1} & \text{Equation A-6} \\
\text{When } Z_S = Z_0, \ a_2 & = 0, \ S_{22} = \frac{b_2}{a_2} & \text{Equation A-7}
\end{align*}
\]

In practice, a series of device microwave performance parameters, such as maximum available gain (MAG), stability factor ($K$) and short-circuited current gain ($h_{21}$) can be calculated from the S-parameters as shown below:

\[
\begin{align*}
MAG &= \frac{|S_{21}|}{|S_{12}|} K - \sqrt{K^2 - 1} & \text{Equation A-8} \\
K &= \frac{1 + |S_{11}S_{22} - S_{12}S_{21}|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{12}S_{21}|} & \text{Equation A-9} \\
|h_{21}| &= \left|\frac{-S_{21}}{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}\right| & \text{Equation A-10}
\end{align*}
\]

MAG defines the power gain obtained at input and output impedance matched condition, which is equal to the unilateral power gain ($U$) given that there is no feedback network used. $K$ defines the boundary of device’s stability, where a device with $K>1$ is regarded as unconditionally stable. This is why the power gain in Figure 2.30 shows two different rolling off profiles. Recalled the two FOMs $f_T$ and $f_{\text{max}}$, they are the corresponding cut-off frequency at the unity of MAG and $h_{21}$ respectively.
APPENDIX B: TRANSFORMATION OF Z → Y PARAMETER

The impedance matrix (Z matrix) for a two port network can be transformed to the admittance matrix (Y matrix) using the following equations and vice versa:

\[
Z = \begin{bmatrix}
\frac{Y_{22}}{\Delta Y} & -\frac{Y_{12}}{\Delta Y} \\
\frac{Y_{21}}{\Delta Y} & \frac{Y_{11}}{\Delta Y}
\end{bmatrix}
\]

Equation B-1

Where

\[\Delta Y = Y_{11}Y_{22} - Y_{12}Y_{21}\]

Equation B-1

And

\[
Y = \begin{bmatrix}
\frac{Z_{22}}{\Delta Y} & -\frac{Z_{12}}{\Delta Y} \\
\frac{Z_{21}}{\Delta Y} & \frac{Z_{11}}{\Delta Y}
\end{bmatrix}
\]

Equation B-2

\[\Delta Z = Z_{11}Z_{22} - Z_{12}Z_{21}\]

Equation B-3
APPENDIX C:
EE_HEMT1_Model (EEsof Scalable Nonlinear HEMT Model)

EE_HEMT1 is an empirical analytic model that was developed by Agilent EEsof for the express purpose of fitting measured electrical behaviour of HEMTs. The model equations were developed concurrently with parameter extraction techniques to ensure the model would contain only parameters that were extractable from measured data. Although the model is amenable to automated parameter extraction techniques, it was designed to consist of parameters that are easily estimated (visually) from measured data such as $g_m$-$V_{gs}$ plots. The EE_HEMT1 model can be extracted to fit either DC or AC characteristics. The parameters involve can be expressed as:

1. **DC** - Voltages, $G_{mmax}$, $V_{delt}$, $V_{to}$, Gamma, Kapa, $P_{eff}$, $V_{tso}$, $Deltgm$, $V_{go}$, $V_{ch}$, $V_{dso}$, $V_{sat}$ and
2. **AC** - Voltages, $G_{mmaxac}$, $V_{deltac}$, $V_{toac}$, Gammaac, Kapaac, $P_{effac}$, $V_{tsoac}$, $Deltmac$, $V_{go}$, $V_{ch}$, $V_{dso}$, $V_{sat}$

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Default (Units)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{to}$</td>
<td>Zero-bias threshold parameter.</td>
<td>-1.5 (V)</td>
</tr>
<tr>
<td>Gamma</td>
<td>Vds-dependent threshold parameter.</td>
<td>0.05 (1/V)</td>
</tr>
<tr>
<td>$V_{go}$</td>
<td>Gate-source voltage where transconductance is maximum.</td>
<td>-0.5 (V)</td>
</tr>
<tr>
<td>$V_{delt}$</td>
<td>Parameter that controls linearization point for $G_m$ characteristic.</td>
<td>0.0 (V)</td>
</tr>
<tr>
<td>$V_{ch}$</td>
<td>(Vchannel) Gate-source voltage where Gamma no longer affects the I-V curve.</td>
<td>1.0 (V)</td>
</tr>
<tr>
<td>$G_{mmax}$</td>
<td>Peak transconductance parameter.</td>
<td>70.0e-3 ($S$)</td>
</tr>
<tr>
<td>$V_{dso}$</td>
<td>Drain voltage where Vds dependency disappears from equations.</td>
<td>3.0 (V)</td>
</tr>
<tr>
<td>$V_{sat}$</td>
<td>Drain-source current saturation parameter.</td>
<td>1.0 (V)</td>
</tr>
<tr>
<td>Kappa</td>
<td>Output conductance parameter.</td>
<td>0.0 (1/V)</td>
</tr>
<tr>
<td>$P_{eff}$</td>
<td>Channel-to-backside self-heating parameter (effective power compression).</td>
<td>2.0 (W)</td>
</tr>
<tr>
<td>$V_{tso}$</td>
<td>Subthreshold onset voltage.</td>
<td>-10.0 (V)</td>
</tr>
</tbody>
</table>
### Table C-2 EEHEMT1 Charge Model Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Default (Units)</th>
</tr>
</thead>
<tbody>
<tr>
<td>C11o</td>
<td>Maximum input capacitance for $V_{ds}$=Vdso and $V_{ds}$&gt;$\Delta t_{ds}$.</td>
<td>0.3 (pF)</td>
</tr>
<tr>
<td>C11th</td>
<td>Minimum (threshold) input capacitance for $V_{ds}$=Vdso.</td>
<td>0.03 (pF)</td>
</tr>
<tr>
<td>Vinfl</td>
<td>Inflection point in C11-Vgs characteristic.</td>
<td>-1.0 (V)</td>
</tr>
<tr>
<td>Delq</td>
<td>C11th to C11o transition voltage.</td>
<td>0.5 (V)</td>
</tr>
<tr>
<td>Deltlds</td>
<td>Linear region to saturation region transition parameter.</td>
<td>1.0 (V)</td>
</tr>
<tr>
<td>Lambda</td>
<td>$C_{11}$-$V_{d}$ characteristic slope parameter.</td>
<td></td>
</tr>
<tr>
<td>C12sat</td>
<td>Input transcapacitance for $V_{gs}$=$V_{infl}$ and $V_{ds}$&gt;$\Delta t_{ds}$.</td>
<td>0.03 (1/V)</td>
</tr>
<tr>
<td>Cgdsat</td>
<td>Gate-drain capacitance for $V_{ds}$=$\Delta t_{ds}$.</td>
<td>0.05 (pF)</td>
</tr>
<tr>
<td>Riss</td>
<td>Source-end channel resistance.</td>
<td>2.0 (ohms)</td>
</tr>
<tr>
<td>Rids</td>
<td>Drain-end channel resistance.</td>
<td>0.0 (ohms)</td>
</tr>
<tr>
<td>Tau</td>
<td>Source-to-drain charging delay.</td>
<td>1.0 (ps)</td>
</tr>
<tr>
<td>Cdsso</td>
<td>Drain-source inter-electrode capacitance.</td>
<td>80.0 (fF)</td>
</tr>
</tbody>
</table>

### Table C-3 EEHEMT1 Dispersion Model Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Default (Units)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rdb</td>
<td>Dispersion source output impedance.</td>
<td>1.0e9 (ohms)</td>
</tr>
<tr>
<td>Cbs</td>
<td>Dispersion source capacitance.</td>
<td>1.6e-13 (F)</td>
</tr>
<tr>
<td>Gdbm</td>
<td>Additional d-b branch conductance at $V_{ds}$=Vdsm.</td>
<td>0.0 (S)</td>
</tr>
<tr>
<td>Kdb</td>
<td>Parameter that controls $V_{ds}$ dependence of additional d-b branch conductance.</td>
<td>0.0 (dimensionless)</td>
</tr>
<tr>
<td>Vdsm</td>
<td>Voltage where additional d-b branch conductance becomes constant (Gdbm).</td>
<td>1.0 (V)</td>
</tr>
<tr>
<td>Gmaxmac</td>
<td>Peak transconductance parameter (AC).</td>
<td>60.0e-3 (S)</td>
</tr>
<tr>
<td>Vdelac</td>
<td>Parameter that controls linearization point for Gm characteristic (AC).</td>
<td>0.0 (V)</td>
</tr>
<tr>
<td>Vtoac</td>
<td>Zero-bias threshold parameter (AC).</td>
<td>-1.5 (V)</td>
</tr>
<tr>
<td>Gammaac</td>
<td>$V_{ds}$-dependent threshold parameter (AC).</td>
<td>0.05 (1/V)</td>
</tr>
<tr>
<td>Kappaac</td>
<td>Output conductance parameter (AC).</td>
<td>0.0 (1/V)</td>
</tr>
<tr>
<td>Peffac</td>
<td>Channel-to-backside self-heating parameter (AC).</td>
<td>10.0 (W)</td>
</tr>
</tbody>
</table>
Figure C-1 EE_HEMT1 \( g_m^{-V_{gs}} \) Parameters

Table C-4 EEHEMT1 \( g_m \) Compression Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Default (Units)</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{Co} )</td>
<td>Voltage where transconductance compression begins.</td>
<td>10.0 (V)</td>
</tr>
<tr>
<td>( \mu )</td>
<td>Parameter that adds ( V_{at} ) dependence to transconductance compression onset.</td>
<td>0.0 (dimensionless)</td>
</tr>
<tr>
<td>( V_{ba} )</td>
<td>Transconductance compression &quot;tail-off&quot; parameter.</td>
<td>1.0 (V)</td>
</tr>
<tr>
<td>( V_{bc} )</td>
<td>Transconductance roll-off to tail-off transition voltage.</td>
<td>1.0 (V)</td>
</tr>
<tr>
<td>( \Delta g_m )</td>
<td>Slope of transconductance compression characteristic.</td>
<td>0.0 (S/V)</td>
</tr>
<tr>
<td>( \alpha )</td>
<td>Transconductance saturation-to-compression transition parameter.</td>
<td>1.0e-3 (V)</td>
</tr>
</tbody>
</table>
## APPENDIX D

### Material Parameters Used in XMBE131 pHEMT Device Physical Modelling

Table D-1 Models and parameters used in physical device simulation

<table>
<thead>
<tr>
<th>Material</th>
<th>In0.53Ga0.47As</th>
<th>In0.3Al0.7As</th>
<th>In0.3Al0.7As</th>
<th>In0.7Ga0.3As</th>
<th>In0.52Al0.48As</th>
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<td><strong>Regional and Band Parameters</strong></td>
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<td></td>
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<tr>
<td>Permittivity</td>
<td>13.88</td>
<td>12.01</td>
<td>12.01</td>
<td>12.01</td>
<td>14.2</td>
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<tr>
<td>Bandgap energy (eV)</td>
<td>0.76</td>
<td>1.981</td>
<td>1.981</td>
<td>1.981</td>
<td>0.602</td>
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<td>Electron affinity (χ)</td>
<td>4.57</td>
<td>4.02</td>
<td>4.02</td>
<td>4.02</td>
<td>4.67</td>
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<tr>
<td>Effective DOS (Nc)</td>
<td>2.2x10^17</td>
<td>9.38x10^17</td>
<td>9.38x10^17</td>
<td>9.38x10^17</td>
<td>2.1x10^17</td>
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<tr>
<td>Effective DOS (Nv)</td>
<td>8x10^18</td>
<td>1.44x10^19</td>
<td>1.44x10^19</td>
<td>1.44x10^19</td>
<td>7x10^18</td>
</tr>
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<td>Effective mass (me)</td>
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<td>0.085</td>
<td>0.085</td>
<td>0.085</td>
<td>0.036</td>
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<td><strong>Recombination Parameters and Models</strong></td>
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<tr>
<td>Auger coeff for e-</td>
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<td>1.4x10^−28</td>
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<td>Carrier lifetime e-</td>
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<td>0.34</td>
<td>0.34</td>
<td>-</td>
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<td>Density</td>
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<td>2x10^16</td>
<td>2x10^16</td>
<td>2x10^16</td>
<td>-</td>
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<tr>
<td>Cross Sec. Area (on)</td>
<td>-</td>
<td>1x10^−17</td>
<td>1x10^−17</td>
<td>1x10^−17</td>
<td>-</td>
</tr>
<tr>
<td>Cross Sec. Area (op)</td>
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<td>1x10^−17</td>
<td>1x10^−17</td>
<td>1x10^−17</td>
<td>-</td>
</tr>
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<td>Energy Level</td>
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<td>Density</td>
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<td>2x10^16</td>
<td>2x10^16</td>
<td>-</td>
</tr>
<tr>
<td>Cross Sec. Area (on)</td>
<td>-</td>
<td>8x10^−16</td>
<td>8x10^−16</td>
<td>8x10^−16</td>
<td>-</td>
</tr>
<tr>
<td>Cross Sec. Area (op)</td>
<td>-</td>
<td>1x10^−17</td>
<td>1x10^−17</td>
<td>1x10^−17</td>
<td>-</td>
</tr>
</tbody>
</table>
APPENDIX E:

DECKBUILD FILE FOR XMBE308 RTD DEVICE
(QUANTUM MODELLING)

go atlas
# n-type InGaAs-AlAs RTD example
# 0.85nm-4.5nm-0.85nm double barrier

mesh diag.flip space.mult=1.0 width=1.5

# This mesh is not important. Normally we'll use only one slice.
# Define device size here
x.mesh loc=0.00 spac=0.5
x.mesh loc=0.6 spac=0.5

# Non-uniform mesh in transport direction. Need higher resolution around the barriers.
y.mesh loc=0.0 spac=0.0005
y.mesh loc=0.045 spac=0.0002
y.mesh loc=0.070 spac=0.0002
y.mesh loc=0.0725 spac=0.0001
y.mesh loc=0.07335 spac=0.0001
y.mesh loc=0.07785 spac=0.0001
y.mesh loc=0.0787 spac=0.0001
y.mesh loc=0.0812 spac=0.0001
y.mesh loc=0.1062 spac=0.0001
y.mesh loc=0.1462 spac=0.0001

# Source and drain regions have to be specified as EQUIL.NEGF
# to impose quasi-equilibrium condition.
region num=1 material=InGaAs x.comp=0.47 y.max=0.0725 equil.negf
region num=2 material=AlAs y.min=0.0725 y.max=0.07335
region num=3 name=well material=InGaAs x.comp=0.2 y.min=0.07335
y.max=0.07785
region num=4 material=AlAs y.min=0.07785 y.max=0.0787
region num=5 material=InGaAs x.comp=0.47 y.min=0.0787 equil.negf

# Define electrode
elec num=1 name=emitter top
elec num=2 name=collector bottom

# Doping concentration
doping reg=1 y.max=0.045 uniform n.type conc=2e19
doping reg=1 y.min=0.045 y.max=0.070 uniform n.type conc=5.5e18
doping reg=5 y.min=0.0812 y.max=0.1062 uniform n.type conc=5.5e18
doping reg=5 y.min=0.1062 uniform n.type conc=1e19

# Mass approximation
material name=AlAs mc=0.268 mlh=0.16 mhh=0.76
material name=InGaAs mc=0.041 mlh=0.05 mhh=0.59

# Material material=InGaAs x.comp=0.47
# InGaAs x.comp=0.47
material name=InGaAs permittivity=13.88 eg300=0.74 affinity=4.57
nc300=2.06e17 nv300=7.81e18 mc=0.041 mv=0.46
ni.min=7.55e+11
material name=InGaAs taun0=3e-10 taup0=1e-8
NSRHN=9e17 NSRHP=8e17
material name=InGaAs vsatn=7.67e6 vsatp=6.01e6
material name=InGaAs augn=2e-27
mobility name=InGaAs mln.caug=2000 \nmu1p.caug=50\nmu2p.caug=400 ncritn.caug=6.4e17 ncritp.caug=7.4e17

#InGaAs x.comp=0.2

material name=well permittivity=14.15 \neg300=0.5 affinity=4.67 
c300=2.1e17 \nv300=7e+18 mc=0.03

material name=well taun0=1e-8 taup0=1e-8 NSRHN=1e17 NSRHP=5e17

material name=well vsatn=2.70e7 vsatp=5.47e6

material name=well augn=2e-26

mobility name=well mln=13400 mup=2000 betan=1.0

#trap donor e.level=0.4 density=5e15 degen.fac=2 sign=1e-13 sigp=1e-13

trap acceptor e.level=0.34 density=2e16 degen.fac=2 sign=1e-16 sigp=1e-17

models n.negf_plld eta.negf=0.03 esize.negf=2001 eig.ymin=0.070

method carr=0 trap impact selb

output con.band val.band eigen=5

log outf=xmbe308_spacer_25A_xmbe308_1.5umx0.6um_barr8.5A.log

solve init

save outf=xmbe308_spacer_25A_xmbe308_1.5umx0.6um_barr8.5A.str negf.log negf.eig

solve v2=0 name=collector vstep=0.012 vfinal=0.1

solve name=collector vstep=0.012 vfinal=0.2

solve name=collector vstep=0.012 vfinal=1.0

log off

tonyplot xmbe308_spacer_25A_xmbe308_1.5umx0.6um_barr8.5A.str

quit
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