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Real-Time Frequency Tracking for Induction Motor Drives using LabVIEW FPGA

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Abstract—This paper reports the implementation procedure of a real-time frequency tracking algorithm for induction motor drive velocity estimation on a commercial cRIO real-time/FPGA platform. The general software architecture required to establish a real-time frequency tracking routine is presented and its frequency tracking performance illustrated in practical tests on a 7.5 kW induction motor drive. The presented architecture is shown to provide a flexible and effective platform for real-time frequency estimation applications in electric motor drives.

Keywords—(induction motor drive; real-time frequency tracking; FPGA; velocity estimation)

I. INTRODUCTION

Computer-based real-time applications using field-programmable gate array (FPGA) based hardware present attractive possibilities for enhancing real-time performance of electric drive systems. Compared to microcontroller systems traditionally employed to enable real-time applications in electric drives [1-4], FPGAs generally provide the advantages of a significantly more flexible architecture with unconstrained input/output interfaces, high compatibility levels across different platforms and increased processing speed. While real-time FPGA based solutions have been researched for implementation of drive control algorithms [5-6] they received significantly less attention where drive parameter estimation techniques are concerned [1-4]. This work reports the implementation procedure of an FPGA based velocity estimation technique for an induction motor drive and illustrates its performance on a practical commercial system.

Sensorless velocity estimation techniques eliminate the requirement for high cost mechanical velocity sensors thus lowering the drive cost and increasing its robustness. These are largely based on real-time algorithms that estimate the rotor speed based on real-time analysis and estimation of a known speed-dependent spectral frequency contained in motor electrical signals. The available literature on sensorless velocity estimation mostly treats the development of real-time frequency tracking algorithms implemented on microcontrollers [1-4]. Real-time spectral search based velocity estimation is reported in [1-4] at estimation window durations ranging from ≈ 142.8 to ≈ 333.3 milliseconds, with some of the employed techniques using overlapping windows to increase the attainable estimation rate. FPGA application of real-time position and speed estimation techniques that are non-spectral search based has been examined recently [7-8] to evaluate the execution speed benefits provided by FPGA implementation.

Spectral search based techniques can however offer significant advantages in sensorless speed estimation schemes due to imposing no requirements for machine parameter data; their implementation on FPGA platforms could further improve their efficacy but has received little attention.

This work details the implementation procedure of a real-time frequency tracking algorithm for sensorless speed estimation in induction motor open-loop drives proposed in [9-10] using LabVIEW FPGA programming and the real-time embedded processor of a CompactRIO (cRIO) platform. The procedure required to establish the real-time frequency estimation algorithm on the cRIO platform is described and the experimental results obtained in its real-time performance tests on a commercial drive system reported.

II. EXPERIMENTAL SET-UP

Experimental work was performed on a 4-pole 7.5kW 50Hz induction machine connected to a speed controlled DC motor prime mover. Induction motor open-loop controlled operation was achieved by supplying its stator windings by a programmable supply unit (PSU), operated to provide a desired real-time V/f time profile. A simplified schematic of the test-rig system is presented in Fig. 1. The test rig allows open-loop operation of the considered motor design in a range of desired steady-state and transient regimes as further detailed in [9-11]. LEM LA305-S current and LV25-600 voltage transducers were used to acquire the test machine's stator currents and voltages. An NI-9205 C-series analogue input module was used to record the measured signals and an NI-9024 cRIO real-time platform employed for three-phase power signal acquisition and execution of the real-time frequency tracking algorithm.

Fig. 1: Schematic diagram of the test-rig system

III. REAL-TIME APPLICATION USING LABVIEW FPGA

A. Frequency Tracking Algorithm

The technique applied for real-time frequency tracking

uses the dichotomous search of the induction machine power signal; once the frequency of the known power signal harmonic, $f_{TRACKED}$, is estimated the velocity of the motor, n_r , can be calculated from $n_r = (10xf_{TRACKED})/(kxp)$, where k is the tracked harmonic order and p is the motor pole pair number, as proposed in [12]. Dichotomous search provides an inherent advantage in the attainable frequency estimation rate increase without compromising the estimation accuracy [9-12]. The search algorithm comprises a sequence of two main stages: the initial coarse search and the final, iterative, fine search [13].

The search algorithm executes frequency tracking of a known induction machine power signal harmonic within the searched narrowband window whose boundaries are determined from the machine operating speed range and the supply frequency, f_s [9-10]. The general steps comprising the algorithm are detailed in [9-13] and are briefly summarised here for the sake of completeness:

- Identify the boundaries of the searched power signal narrowband from the monitored value of the supply frequency, f_s , and perform a low resolution FFT.
- Extract the frequency maximising the low resolution narrowband to obtain a coarse estimate of the tracked harmonic's frequency. Execute dichotomous iterative fine search on the extracted coarse frequency estimate to obtain improved accuracy estimation of the tracked power harmonic frequency.

B. Real-Time Implementation on FPGA Platform

The proposed real-time frequency tracking algorithm is separated into two sections in this research: data collection, FFT processing and data transfer on the 40 MHz Virtex-5LX110 FPGA module housed in an 8-slot NI-9118 reconfigurable chassis, and the execution of the frequency tracking algorithm implemented on an NI-9024 cRIO controller. The NI-9024 cRIO is a real-time embedded controller with an 800 MHz processor, 512 MB of DRAM and 4 GB of memory in which data transfer can take place at a rate of up to 1000 Mbps [14]. An NI-9205 C-series analogue I/O module was mounted on an 8-slot NI-9118; this is a 32 channel 16-bit analogue module which uses successive approximation register of analogue to digital converter with a maximum sampling frequency of 250 kHz [15].

A LabVIEW FPGA VI code was developed to execute a FFT of the measured power signal in successive, constant size Hann windows. The obtained FFT values are stored in the controller's memory using the First In First Out (FIFO) method. Direct Memory Access – First In First Out (DMA - FIFO) was used to transfer the stored FFT values and the time domain power signal data to the cRIO controller for further processing. The power signal is processed in the FFT VI in a 2^8 point FFT routine. The calculated frequency and time domain power signal values are stored in the memory separately and transferred to the controller in the 2^8 data point packages by checking the DMA FIFOs status before writing

Fig. 2: FPGA VI's block diagram for FFT execution and data storage

Fig. 3: FPGA VI's block diagram for data transfer

the stored FFT values in the DMA-FIFOs, so that the FPGA DMA buffers do not overflow. The developed FPGA VI code writes the obtained FFT values to the DMA-FIFO one element at a particular time using the write method of the FPGAFIFO method node. Simplified block diagrams of the data collection/FFT execution and the data transfer practical implementation are shown in Figs. 2-3.

A LabVIEW VI code hosted on the cRIO controller was developed that uses the read method of the FPGA FIFO method node to collect the stored real-time FFT values and the power signal time domain data and perform the tracking of the target power harmonic frequency. In order to ensure a continuous execution of the main while loop with no data insufficiency the DMA-FIFOs on the controller were reconfigured so that the main while loop executes after the FIFOs obtain 2^9 data points from the FPGA VI, out of which 2^8 data points are processed at a time. Suitable sampling rate (≈ 2.56 kHz) of the FPGA VI code and the execution time (≈ 100 msec) of the main while loop hosted on cRIO were determined for the investigated application in practical tests. A simplified schematic describing the real-time data transfer from the FPGA to the cRIO controller is provided in Fig. 4.

The full structure of the developed real-time code executing frequency estimation is shown in the flowchart in Fig. 5. The dichotomous fine search summarised in section III.A and detailed in [9-13] is implemented as a text-based code using a MathScript RT module. This code is developed using if and else statements nested into the main while loop of the full algorithm along with the LabVIEW function blocks executed coarse search routine. The algorithm executed within the while loop first identifies the low resolution target frequency, $P_o(f_{max})$, within the defined narrowband by performing a coarse search of

the FPGA provided frequency domain data. Once $P_o(f_{max})$ is identified the coarse search routine also determines two adjacent frequency values and their magnitudes, $P_{-1}(f_{max})$ and $P_1(f_{max})$, as a precursor to the ensuing fine search executed in the MathScript RT module. In the fine search procedure, the frequency estimation is adjusted to extract a fine resolution estimate of the tracked frequency. This is achieved by executing the routine presented in [9-13] using if an else statements in MathScript code. The fine search procedure is repeated Q times to improve the obtained frequency estimation, $f_{TRACKED}$.

Fig. 4: cRIO VI's schematic for data transfer and frequency tracking

Fig. 5: Real-time frequency search algorithm implementation

Fig. 6: Measured power spectrum, ~478 rpm, $f_s = 16$ Hz

Fig. 7: Measured power spectrum, ~437 rpm, $f_s = 16$ Hz

IV. EXPERIMENTAL RESULTS

A. Spectral Analysis of the Power Signal

The order of the power signal harmonic whose frequency is tracked for velocity estimation on the examined motor design is $k=3$ [9-12, 16-17]. The searched spectral narrowbands maximised by the tracked harmonic have been measured in tests for drive system operation at the minimum (16 Hz) and maximum (50 Hz) attainable supply frequency on the test rig and are shown in Figs. 6-9 for illustration purposes; for each examined supply frequency the motor was run at no-load and full-load and the power narrowband acquired to illustrate the dependence of the tracked harmonic frequency on motor speed [16-17]. The presented narrowbands were obtained by processing the measured power signal data in the MATLAB FFT routine with frequency resolution of ≈ 0.15 Hz.

B. Real-time Frequency Tracking Performance

The frequency tracking performance of the FPGA platform executed real-time algorithm is illustrated in this section. This is done by first examining the motor operation at constant speed at no-load and full-load conditions with 16 Hz and 50 Hz supply frequencies. The obtained steady-state frequency estimation results are shown for a period of ≈ 10 secs in Figs. 10-11. These are seen to provide average frequencies of ≈ 284.9 and ≈ 896.7 Hz for the no-load conditions and are ≈ 261.1 and ≈ 874.4 Hz for full-load conditions, respectively. The estimated frequencies are seen to be in close agreement with the FFT measured tracked frequency spectra in Figs. 6-9.

Real-time frequency tracking performance was illustrated for motor transient operation comprising a transient ramp of ≈ 32 secs duration from minimum (16 Hz) to nominal (50 Hz) supply frequency under full-load conditions. The real-time tracked frequency results are shown in Fig. 12 and are seen to follow the expected transient variation profile. The comparison of the tracked frequency results in Fig. 12 with the Short-term FFT spectrum of the recorded searched power signal narrowband in Fig. 13 confirms close agreement between the estimated and measured tracked frequency, $f_{TRACKED}$, at an algorithm's execution time of ≈ 100 msec.

Fig. 8: Measured power spectrum, ~1498 rpm, $f_s = 50$ Hz

Fig. 9: Measured power spectrum, ~1465 rpm, $f_s = 50$ Hz

Fig. 10: Real-Time steady-state no-load and full-load, $f_s = 16$ Hz

Fig. 11: Real-time steady-state no-load and full-load, $f_s = 50$ Hz

Fig. 12: ~32 sec full-load, $f_s = 16$ to 50 Hz, $k = 3$

Fig. 13: ~32 sec Short-Term FFT, $f_s = 16$ to 50 Hz, $k = 3$

V. CONCLUSIONS

This paper presents the implementation procedure of a frequency tracking algorithm for velocity estimation in electric motor drives on a commercial cRIO FPGA/real-time platform. The general software architecture required to establish a real-time frequency estimation routine is described and its performance illustrated in tests on commercial equipment. The reported procedure provides a simple yet effective technique for real-time frequency tracking applications in electric drives.

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