ADVANCED InGaAs/InAlAs/InP pHEMTS

FOR

LOW NOISE AND ULTRA FAST ELECTRONICS

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School of Electrical and Electronic Engineering
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<tr>
<td>2DEG</td>
<td>2 Dimensional Electron Gas</td>
</tr>
<tr>
<td>ADS</td>
<td>Agilent Advanced Design System</td>
</tr>
<tr>
<td>Al</td>
<td>Aluminium</td>
</tr>
<tr>
<td>AlGaAs</td>
<td>Aluminium Gallium Arsenide</td>
</tr>
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<td>As</td>
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<td>Coat-Expose-Develop</td>
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<td>CMOS</td>
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<td>DC</td>
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<tr>
<td>DI water</td>
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<td>DUV</td>
<td>Deep Ultraviolet</td>
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<tr>
<td>G-S-G</td>
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<td>High Electron Mobility Transistor</td>
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<td>MIM</td>
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<tr>
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<td>NMP</td>
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<td>PA</td>
<td>Power Amplifier</td>
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<tr>
<td>PECVD</td>
<td>Plasma-Enhanced Chemical Vapor Deposition</td>
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<td>pseudomorphic High Electron Mobility Transistor</td>
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<td>Photoresist</td>
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<td>SoG</td>
<td>Spin-on-Glass</td>
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<tr>
<td>TE</td>
<td>Thermionic Emission</td>
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<td>TFE</td>
<td>Thermionic Field Emission</td>
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<td>Ti</td>
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<td>TLM</td>
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<td>U</td>
<td>Unilateral power gain</td>
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<td>UHV</td>
<td>Ultra-High Vacuum</td>
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<td>UV</td>
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<td>UWB</td>
<td>Ultra Wide Band</td>
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<td>V_BR</td>
<td>Breakdown Voltage</td>
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<td>VNA</td>
<td>Vector Network Analyser</td>
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Conventional pseudomorphic High Electron Mobility Transistor (pHEMTs) with lattice-matched InGaAs/InAlAs/InP structures exhibit high mobility and saturation velocity, and are hence attractive for the fabrication of three-terminal low noise and high frequency devices, which operate at room temperature. The major drawbacks of conventional pHEMT devices are the very low breakdown voltage (< 2 V) and the very high gate leakage current (~ 1 mA/mm), which degrade device performance especially in MMIC LNAs. These drawbacks are caused by the impact ionization in the low band gap, i.e. the In$_x$Ga$_{(1-x)}$As ($x = 0.53$ or $0.7$) channel material plus the contribution of other parts of the epitaxial structure.

The capability to achieve higher frequency operation is also hindered in conventional InGaAs/InAlAs/InP pHEMTs, due to the standard 1 μm flat gate length technology used. A key challenge in solving these issues is the optimization of the InGaAs/InAlAs epilayer structure through bandgap engineering, without affecting the device RF characteristics. A related challenge is the fabrication of submicron gate length devices using I-line optical lithography, which is more cost-effective, compared to the use of e-Beam lithography.

The main goal for this research involves a radical departure from the conventional InGaAs/InAlAs/InP pHEMT structures by designing new and advanced epilayer structures, which significantly improves the performance of conventional low-noise pHEMT devices, and at the same time preserves the RF characteristics. To achieve this, modified epilayer structures were fabricated and characterized, including solving the standard 1 μm gate length processing issue. DC and RF results are then carefully analysed, and compared with those of the conventional pHEMT. Optimization of the submicron T-gate length process is then performed, by introducing a new technique to further scale-down the bottom gate opening. A new material, SoG, is also explored to simplify the submicron process flow even further.

The results of this work show outstanding performance compared to the conventional pHEMT. The breakdown voltage and gate current leakage are significantly improved, by ≥ 70 % and ≥ 90 % respectively, with no detrimental effect on the RF characteristics, while the new technique of the submicron process shows a 58 % increase in $f_T$ and 33 % increase in $f_{max}$.

The SoG material shows suitability for use in a soft-reflow process, but due to some constraints, its development is left as future work; however, at present it could be used for passivation and production of capacitor dielectrics.

The success of the modification and optimisation of the InGaAs/InAlAs material system, coupled with the gate length reduction into sub-μm regime enable high breakdown and ultra-high speed low noise devices to be fabricated, especially for low-noise amplifiers (LNAs) and low-noise receivers operating in the microwave and millimetre wave regime.
DECLARATION

No portion of the work referred to in the dissertation has been submitted in support of an application for another degree or qualification of this or any other university or other institute of learning.

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DEDICATION

I would like to dedicate this thesis:

To my parents for making me be who I am...

To my wife, sons, siblings and in-laws for supporting

my PhD journey...
PUBLICATIONS

Journal:

F. Packeer, M. Mohamad Isa, W Mat Jubadi, K W Ian and M. Missous “Fabrication and Characterization of Tensile In$_{0.3}$Al$_{0.7}$As Barrier and Compressive In$_{0.7}$Ga$_{0.3}$As Channel pHEMTs Having Extremely Low Gate Leakage for Low Noise Applications” in IOP Journal of Physic D: Applied Physics, J.Phys. D: Appl. Phys. 46 (2013) 264002 (7pp).

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Conferences:


   (Best Overall Paper Award and the Best Paper Award in the category of Electronic and Electrical Engineering).

2. F. Packeer, Warsuzarina Mat Jubadi and M. Missous “New Submicron Low Gate Leakage In$_{0.52}$Al$_{0.48}$As-In$_{0.7}$Ga$_{0.3}$As pHEMT for Low Noise Applications” in UK Semiconductor 2014 Conference, Sheffield Hallam University, 9 July 2014.
3. W.M. Jubadi, **F. Packeer**, K.W.Ian and M.Missous “Optimization of Two Dimensional and Empirical Modelling of 0.25 µm In$_{0.7}$Ga$_{0.3}$As/In$_{0.3}$Al$_{0.7}$As pHEMT Device for X-band MMIC Low Noise Amplifier” in UK Semiconductor 2014 Conference, Sheffield Hallam University, 9 July 2014.


5. **F. Packeer**, M. Mohamad Isa and M. Missous “Fabrication and Characterization of Tensile In$_{0.3}$Al$_{0.7}$As Barrier and Compressive In$_{0.7}$Ga$_{0.3}$As Channel pHEMTs Having Extremely Low Gate Leakage for Low Noise Applications” in Postgraduate Poster Conference and Industrial Advisory Group Meeting, Manchester, 22 November 2012.

6. **F. Packeer**, M. Mohamad Isa and M. Missous “Fabrication and Characterization of Tensile In$_{0.3}$Al$_{0.7}$As Barrier and Compressive In$_{0.7}$Ga$_{0.3}$As Channel pHEMTs Having Extremely Low Gate Leakage for Low Noise Applications” in UK Semiconductor 2012 Conference, The University of Sheffield, 5 July 2012.
CHAPTER 1

INTRODUCTION

1.1 OVERVIEW

Modern consumer electronics generally use Silicon (Si) MOSFET technology. However, as the drive to fulfil Moore’s law continues, new device materials and architectures are being proposed - the High Electron Mobility Transistor (HEMT) being a case in point. The device has already been mapped onto the International Technology Roadmap for Semiconductor (ITRS), and will cater for more advanced communications and ultra-high speed, ultra-low noise electronics applications. The HEMT - also known as the heterostructure FET (HFET) - integrates a junction between two materials with different band gaps (a heterojunction) as the path for high electrons mobilities; this is different from MOSFET, which uses a doped region for the movement of electrons.

The formation of the channel in MOSFETs - particularly n-MOSFETs where the electrons are the charge carriers - can be explained by referring to Figure 1.1. When the bias at the gate has a positive potential with reference to the P-type substrate - i.e. a positive voltage is applied at the gate - a depletion region near to the gate oxide surface will be created, because the majority of the holes will be repelled by the positive charges at the gate terminal, while some minority electrons will be attracted to the surface; however, the gate potential it is still too low for the accumulation of electrons to cause current conduction. When the positive gate voltage is increased, it will form a dense inversion layer of electrons under the gate oxide surface; when this gate voltage reaches the threshold voltage (V_{th}), the electron-rich inversion layer will form a conduction channel; therefore this channel...
formation will conduct current between the MOSFET source and drain terminals. This behaviour is different from that of a High Electron Mobility Transistor (HEMT), which will be explained in detail in Chapter 2.

Figure 1.1 N-type Metal Oxide Semiconductor Field Effect Transistor (nMOSFET) [1]

HEMTs behave like FETs, except that they comprise materials which keep the electrons and holes less firmly bound, so that these carriers of electric current have greater mobility. This is due to the fact that the free charge carriers are “captured” in a potential well, and therefore these charge carriers are physically separated from their parent donor or acceptor atoms and thus will suffer less scattering leading to a higher mobility. If an undoped spacer layer is introduced, as is the case in all the devices studied in this work, then the physical separation of free electrons and their donor atoms is even greater improving the mobility even further.
Due to this “high electron mobility”, HEMT are able to switch much faster than FETs, therefore HEMTs offer higher performance when amplifying microwave signals.

Another variant, the pseudomorphic HEMT (pHEMT) is the fastest type of transistor, and is ideal for microwave and millimetre-wave applications. The device is made from compound materials which are not lattice-matched. The structure of the pHEMT is different from HEMT, in that one of the material layers is so thin that the crystal lattice stretches “pseudomorphically” to occupy the spacing of the nearby material. This structure allows the pHEMT to have better performance with larger bandgap differences than would otherwise be possible.

The pHEMT uses high-mobility materials for the channel; many new materials have been explored since early 2000’s, but the most recently studied materials are III-V compound semiconductors [2]. For this research, the materials used are Indium Gallium Arsenide (InGaAs) and Indium Aluminium Arsenide (InAlAs). InGaAs is a semiconductor material composed of Indium, Gallium and Arsenic, while InAlAs is a semiconductor material composed of Indium, Aluminium and Arsenic. In$_x$Al$_{(1-x)}$As has almost the same lattice constant as In$_x$Ga$_{(1-x)}$As for $x \approx 0.52$, but a larger bandgap. This material system has already become important for fabricating Monolithic Microwave Integrated Circuit (MMIC) devices including very low-noise amplifiers and receivers, mainly due to its outstanding combination of high frequency operation and low noise.

1.2 RESEARCH BACKGROUND

As the drive towards ever smaller and faster devices intensifies, a great deal of progress has been made in the research of non-silicon materials to substitute for silicon in the transistor channel. Among the materials studied are Ge [3], low band-
gap III-V compound semiconductors [4-7], carbon nanotubes [8] and graphene [9]. However, III-V compound semiconductors are the most studied materials in this group, and have the potential to enable the production of future high-speed transistors for commercial applications, with very low noise and high breakdown voltages.

Studies have also shown that pHEMTs using III-V compound semiconductors incorporating quantum wells show improvements in both energy efficiency and speed, compared with silicon channel devices; the enhanced electron channel mobility is the key performance boosting parameter [2, 6].

In general, pHEMT devices have the highest transconductance (for a given gate size) when incorporating InGaAs-InAlAs compound semiconductors, because of the high electron mobility, large conduction band discontinuity, and very good carrier confinement in the channel [10]. This unique property allows the design of fairly complex circuitry, and subsequent fabrication in relatively low-volume applications where the cost of using either CMOS or SiGe would be prohibitive.

The precise nanoscale-size growth of compound semiconductor materials for pHEMTs relies on a technique called Molecular Beam Epitaxy (MBE) [10, 11]. The most important aspect of MBE is the slow deposition rate (typically less than 1000 nm per hour), which allows the films to grow epitaxially. MBE dominates the practical approaches and techniques required to meet the stringent doping and thickness specifications, to sub-monolayer accuracy for the production of pHEMTs. This enables the production of a variety of advanced low-noise and ultra-fast electronic devices, such as next-generation high speed instrumentation, Ultra Wide Band communications (UWB) and electronic warfare.
1.3 PROBLEM STATEMENT

pHEMT devices using the InGaAs-InAlAs materials system, lattice-matched to InP, have a bright future not only for ultra-high speed and ultra-low noise devices such as Monolithic Microwave Integrated Circuit (MMIC) Low Noise Amplifiers (LNAs), but also for Power Amplifier (PAs).

Conversely, such devices that incorporate conventional InGaAs-InAlAs pHEMTs suffer from low breakdown voltage \( V_{BR} \) and poor linearity, regardless of the gate length used [12]. Over the years, researchers have made efforts to increase the off-state breakdown voltage [13-18], but as yet the \( V_{BR} \) issue has not been fully solved. In addition, the conventional material system also experiences a large DC gate current leakage, related to the low barrier height at the Schottky interface and to the forward conduction inherent in the Schottky gate.

1.4 RESEARCH OBJECTIVES

The focus of this research deals with optimization and improvement of a conventional 1 μm gate length, highly-strained channel, based on an InGaAs/InAlAs/InP pHEMT developed at The University of Manchester. The optimization and improvement is achieved either through bandgap engineering or lateral scaling, or both. The device fabrication is performed using I-line optical lithography, not only to produce low-noise devices that can be implemented in MMIC LNAs in S-band and X-band regimes, but also to maintain its cost effectiveness when producing sub-micron devices without the need to use e-Beam lithography, which is usually used in GaAs or InP technologies. The low noise devices investigated in this work are required to work in the region of 2 GHz to 8 GHz, operating at room temperature with a Minimum Noise Figure \( (NF_{\text{min}}) \) less than 1.5 dB [19, 20]. It is known from other researchers [21-23] that the gate leakage
current is one potential source of shot noise and thermal noise for operating frequencies lower than 10 GHz. Hence, by reducing the gate leakage currents, the reduction in noise figure is significant at the specified frequency range. Furthermore, improvements in device breakdown voltage are expected in this optimized material system, without compromising its low noise properties.

1.5 THESIS ORGANIZATION

i. **Chapter 2** starts with the theory and detailed description of the Hetero Junction Field Effect Transistor, and also of metal-semiconductor contacts which are important in HEMT fabrication. Near to the end of the chapter, and explanation is given of the basic HEMT structure, its operation and finally the advantages of the pHEMT which are used throughout this study.

ii. **Chapter 3** addresses the major issue with the current 1 μm pHEMT gate process, which is defined by optical I-line lithography; the gate length after metallization enlarges from its initial lithographic definition. The target is to solve the issue and optimize the gate length process. The performance of the optimized gate length process is then compared with the current process by device fabrication, where the DC and RF performances are compared.

iii. **Chapter 4** presents the fabrication and characterization of a very low leakage and high breakdown advanced InGaAs/InAlAs/InP pHEMT, through bandgap engineering for low-noise applications. A detailed DC and RF comparison is performed with the conventional InGaAs/InAlAs/InP pHEMT.

iv. **Chapter 5** presents a new technique, identified and investigated to further scale-down the bottom gate opening to less than 0.25 μm for the T-gate submicron InGaAs/InAlAs/InP pHEMT, although this finding is still under development. Similar to Chapter 4, fabrication and characterization of low-noise devices is
undertaken, and their performance compared with the conventional pHEMT. The fabrication of the improved pHEMT is performed with the new and improved soft-reflow process for lateral scaling, coupled with a new epilayer modification, resulting in excellent DC and RF performances.

v. Chapter 6 demonstrates the possible routes to improve the T-gate structure for submicron pHEMT development. The idea is to develop and explore a new material - Spin-on-Glass (SoG) - as a substitute for Silicon Nitride (Si₃N₄) hard mask deposition. The extensive study as well as the key challenges and issues are discussed in this chapter.

vi. Chapter 7 summarizes the work performed in this study and possible directions for future research are suggested.
CHAPTER 2

LITERATURE REVIEW

2.1 HETERO JUNCTION FIELD EFFECT TRANSISTOR

2.1.1 Introduction

Generally, the transistors in modern consumer electronics are made from Silicon (Si) MOSFETs. However, as the drive to fulfil Moore’s law remains, new device materials and architectures are being proposed - the High Electron Mobility Transistor (HEMT) being a case in point. It has already been mapped onto the International Technology Roadmap for Semiconductor (ITRS) and will cater for more advance communication and ultra-high speed, ultra-low power electronics applications. The HEMT, also known as the heterostructure FET (HFET), integrates a junction between two materials with different band gaps (a heterojunction) as the path for high electrons mobilities; this is different from MOSFET, which uses a doped region for the movement of electrons.

2.1.2 Lattice Matched Materials

Any two different semiconductor materials will have different lattice constants; if the two materials are brought into contact, one can observe that, at the atomic level, the atoms at the hetero-interface change their positions to maintain the geometry of the lattice. A strain will be induced at the hetero-interface, resulting from this atomic level change or adjustment. To form heterojunction interfaces, there is a need to ensure that the strain does not exceed a specific critical value which will
later cause crystal dislocation. The severity of such dislocation is such that the carriers will be concentrated in the defect area, and hence degrade the carrier mobility, which in turn will result in poor device function.

There are a number of materials that are available to form heterojunction interfaces, as shown in Figure 2.1.

![Figure 2.1 Energy band gap of direct (solid line) and indirect (dashed line) materials, and lattice constant for various III-V semiconductors at room temperature [24].](image)

As can be seen from the Figure 2.1, it is possible to combine the semiconductor materials in binary, ternary and quaternary systems, to form a variety of alloys with nearly lattice-matched hetero-junction interfaces. Examples of such semiconductor
alloys are $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{InP}$ and $\text{GaAs}/\text{Al}_{x}\text{Ga}_{1-x}\text{As}$; these material systems hetero-junction interfaces have close lattice constant values but abrupt variations in their band gaps.

### 2.1.3 Pseudomorphic Materials

Modern epitaxial growth techniques, for example the Molecular Beam Epitaxial (MBE) technique, have the ability to grow mismatched semiconductor epitaxial layers; the epitaxial layer grown will assume the lattice parameters of the layer it is deposited on. However, the mismatched layers must be kept within certain limits, and the deposited layer must be very thin to avoid formation of defects or dislocations. This new layer then is called “pseudomorphic”, as its original crystal structure and physical properties are altered - an example of this is $\text{In}_x\text{Ga}_{(1-x)}\text{As}$-$\text{In}_y\text{Al}_{(1-y)}\text{As}$ when $x \neq y$. As shown in Figure 2.2, the pseudomorphic material can be in compressive strain if the deposited layer has a larger lattice constant, or tensile strain if the deposited layer lattice constant is smaller.

![Figure 2.2 Formation of pseudomorphic layers with (a) compressive and (b) tensile strain](25).

Figure 2.2 Formation of pseudomorphic layers with (a) compressive and (b) tensile strain [25].
Note that a pseudomorphic layer can be grown to a certain critical thickness $h_c$. Taking Figure 2.2 as example, the strain between the substrate and the deposited epilayer is given by Equation 2.1.

$$\varepsilon = \frac{a_L - a_S}{a_S}$$  \hspace{1cm} \text{Equation 2-1}

Where $\varepsilon = \text{strain between the two layers}$, $a_L = \text{lattice constant of the deposited layer}$, $a_S = \text{lattice constant of the substrate layer}$, while the critical thickness $h_c$ is given by Equation 2.2 below:

$$h_c = \frac{a_S}{2\varepsilon}$$  \hspace{1cm} \text{Equation 2-2}

Furthermore, it is necessary to appreciate that, even though the crystal’s structures and their physical properties are changed, the total energy within the unit cell is maintained. This is possible because of the distortion of the deposited layer in the direction perpendicular to the growth direction, leading to lattice matching in the lateral plane.

### 2.1.4 Band Discontinuities

The most interesting and important part of the heterojunction is the band gap energy associated with each material in the structure. When two materials with different band gap energies are brought together, i.e. a high band gap material combined with a low band gap material, it will lead to energy band discontinuities as shown in Figure 2.3. This so called band-gap engineering is the main feature of heterojunction devices, especially HEMT-based devices.
Figure 2.3 Energy band diagrams before (left) and after (after) combination.

By referring to Figure 2.3, ‘A’ in blue is the high band gap material and ‘B’ in red is the low band gap material, while $E_v$, $E_c$ and $E_F$ are the valence band, conduction band and Fermi levels respectively. The two material’s band discontinuities are determined by $\Delta E_c$ for the conduction band, and $\Delta E_v$ for the valence band. Finally, $\chi$ and $E_g$ denote the electron affinity and band gap, respectively.

Once thermal equilibrium (i.e. Fermi levels aligned) is achieved between the two semiconductor materials, i.e. A and B, the band gap discontinuity $\Delta E_g$ of these two materials is given by Equation 2.3:

$$\Delta E_g = E_g^A - E_g^B$$

This band gap discontinuity can be further manipulated by using different types of materials in combination. For example, for the GaAs/Al$_{0.52}$Ga$_{0.48}$As and In$_{0.53}$Ga$_{0.47}$As/In$_{0.52}$Al$_{0.48}$As [26-28] HEMTs, the $\Delta E_g$ are 0.65 eV and 0.77 eV respectively. Hence, InGaAs-InAlAs pHEMTs have a larger energy band gap discontinuity with better control of the carriers at the heterostructure, compared to GaAs-AlGaAs devices.
2.1.5 Quantum Well and 2DEG

A basic Quantum Well (QW) can be formed if a thin layer (≈ 100 Å thickness) [29] of low band gap semiconductor material (e.g. GaAs) is sandwiched between two similar high band gap semiconductors (e.g. AlGaAs). As illustrated in Figure 2.4, such a heterojunction boundary will experience discontinuities at the edges of the conduction band and valence band, with a QW generated for the carriers (electrons and holes).

Figure 2.4 (a) Heterojunction structure, (b) Energy band diagram of an ideal un-doped square shape quantum well and (c) Conduction band diagram if AlGaAs is n-doped [29].
Note that the dopants in high band gap layers can supply the carriers to the quantum well; when the bottom of the quantum well is below the Fermi level, the high energy donors will fall down to the low lying energy levels in the well, hence creating a Two Dimensional Electron Gas (2DEG) - this is shown in Figure 2.4(c). An interesting fact about the 2DEG is that the electrons are only able to move in the direction along the heterojunctions interface, not in the direction perpendicular to the interface i.e. the crystal growth direction [29].

2.1.6 Delta (δ)–Doped Layers

Traditionally, the doped layers are referred to as bulk doped, where the impurities are homogeneously doped throughout the supply layer. However, a better type of doping is found to be delta doping or simply δ-doping, where a semiconductor layer is doped in a single-atomic plane. Figure 2.5 show the difference between δ-doped and bulk-doped structures in terms of the energy band diagram and quantum wells.

![Delta (δ)–Doped Layers](image)

Figure 2.5 Energy band diagram (a) δ-doped AlGaAs/GaAs heterostructure. (b) Bulk-doped AlGaAs/GaAs heterostructure [30].
Referring to Figure 2.5, the 1\textsuperscript{st} quantization energy level is denoted as $E_0^\delta$, and is similar to $E_0$ in the quantum well. Further observations from the figure also show that all of the carriers are in $E_0^\delta$ of the $\delta$-doped material, whereas they are widely spread over the supply layer of bulk-doped material. As $E_0^\delta$ is below the Fermi level, this gives the advantage of being able to increase the carrier concentration in the 2DEG region, with a high probability of carriers being transferred from the $\delta$-doped are to the quantum well. This phenomenon gives great benefits to HEMT-based devices.

### 2.2 METAL-SEMICONDUCTOR CONTACTS

#### 2.2.1 Introduction

There are two essential contacts in any semiconductor device, especially in heterostructures like HEMT-based devices. These two contacts are known as the Ohmic contact and the Schottky contact, the creation of which depends on the characteristics of the interface with the semiconductor. These contacts are mainly used to connect the semiconductor device to external circuits or probes.

#### 2.2.2 Schottky Contact

This type of contact is basically a metal contact to the gate, in order to enter the channel region in the HEMT. Figure 2.6 illustrates a metal-to-semiconductor interface before and after forming of the Schottky contact; this is the energy band diagram of an n-type semiconductor and metal contact. The notation shown in the figures is as follows: $\Phi_m$ is the metal work function, $\Phi_s$ is the semiconductor work function, $\Phi_B$ is the contact barrier height, $\chi$ is the semiconductor electron affinity,
$E_g$ is the band gap, $E_c$ is the bottom of the covalence band, $E_v$ is the top of the valence band, $E_F$ is the Fermi level, $V_n$ is the potential difference between minimum of the conduction band and the Fermi level, $E_g$ is the energy band gap, and $V_{bi}$ and $X_{dep}$ are the built-in-voltage and depletion region, respectively.

![Schematic band diagram of a metal and semiconductor](image)

**Figure 2.6** Schematic band diagram of a metal and semiconductor (a) in isolated n-type semiconductor adjacent to metal, and (b) in contact after thermal equilibrium [31].

As can be seen from Figure 2.6(b), there will be a flow of electrons from the semiconductor conduction band into the metal, when both the metal and semiconductor make contact due to the Fermi levels of both materials reaching equilibrium. The flow of free electrons will then leave a positive charge of ionised donors in the semiconductor, which creates a depletion region of thickness $X_{dep}$, and consequent band bending at the interface.
Note that there is also a small region of electron build-up at the boundary of the metal and semiconductor. These equal and opposite charges at the contact boundary will then create an electric field from the semiconductor to the metal, and subsequently establish a potential barrier $\Phi_B$ at the interface, and $V_{bi}$ - the built-in-potential - at the semiconductor side. The function of these $\Phi_B$ and $V_{bi}$ is to restrict the electron flow from semiconductor to metal side, subsequently forming a rectifying contact. Equation 2.4 below shows the relationship between $V_{bi}$ with $\Phi_B$ and $V_n$:

$$qV_{bi} = q\Phi_B - qV_n$$  \hspace{1cm} \text{Equation 2-4}$$

On the other hand, the barrier height $\Phi_B$ is ideally related to the work function $\Phi_m$, and the semiconductor electron affinity $\chi$, as shown below in Equation 2.5:

$$q\Phi_B = q\Phi_m - q\chi$$  \hspace{1cm} \text{Equation 2-5}$$

The built-in-potential can also be written as Equation 2.6, to show its relationship with the work functions $\Phi_m$ and $\Phi_s$.

$$qV_{bi} = q(\Phi_m - \Phi_s)$$  \hspace{1cm} \text{Equation 2-6}$$

Furthermore, the Schottky contact will be formed under the two key conditions below:

1. Large barrier height i.e. when $\Phi_B >> kT$
2. Low doping concentration $N_D << N_C$
The Schottky barrier described in Figure 2.6(b) is at zero-bias where the Fermi level $E_F$ between semiconductor and metal are equal (or aligned). Under this zero-bias condition, the net current flow between semiconductor and metal is zero, because the same amount of current flows from semiconductor to metal and vice-versa. However, under forward and reverse bias conditions, the built-in-potential changes, and hence changes the flow of current transport. These conditions are illustrated in Figure 2.7 below, in which $\Phi_B$ remains constant [31] in both figures.

![Figure 2.7](image.png)

**Figure 2.7 Current transport by thermionic emission. (a) forward bias, and (b) reverse bias [31].**

Figure 2.7(a) shows that, when a positive bias $V_F$ is applied to the metal, it will undergo a forward bias condition. Under this condition, the Fermi level of semiconductor ($E_{FS}$) will be shifted up relative to the Fermi level of metal ($E_{FM}$) and the built-in-potential will be reduced by the applied voltage $V_F$. On the other hand
Figure 2.7(b) shows that, if a negative bias $-V_R$ is applied to the metal, a reverse-bias condition is achieved. In this case, the Fermi level of semiconductor ($E_{FS}$) will be shifted down relative to the Fermi level of metal ($E_{FM}$), and the built-in-potential will increase by the applied voltage $V_R$. The quantity of electron flow from metal to semiconductor under the reverse-bias mode is also known as the leakage current in pHEMTs.

### 2.2.3 Ohmic Contact

An Ohmic contact different from a Schottky contact, because it is essentially a non-rectifying contact, and does not control the flow of current, which means the current flows equally in both directions (reverse and forward) with a linear I-V characteristic. An Ohmic contact should have insignificant contact resistance relative to the series resistance of the semiconductor, so that little or no current loss occurs across the device.

The current conduction mechanism is usually either tunnelling or thermionic emission. In the case where thermionic emission is dominant, the contact resistance of the metal to semiconductor is given by Equation 2.7 below:

$$R_C = \frac{k}{qA^*T} \exp\left(\frac{q\phi_B}{kT}\right)$$  \hspace{1cm} \text{Equation 2-7}

Where $A^*$ is the effective Richardson constant, and $T$ is the temperature in K. Equation 2.7 also shows that a low barrier height is needed to allow the Ohmic contact to achieve a small $R_C$ irrespective of doping.

In the case of high semiconductor doping ($N_D \geq 10^{19}$ cm$^{-3}$), the barrier height and depletion width becomes very thin, for which the $R_C$ is then controlled by the
tunnelling current. Alternatively, for semiconductor doping $N_D \leq 10^{17}$ cm$^{-3}$, thermionic emission will once again be dominant [31]

2.3 HIGH ELECTRON MOBILITY TRANSISTOR (HEMT)

2.3.1 Introduction

HEMT devices are an improvement on the Metal-Semiconductor Field Effect Transistor (MESFET) and preferred for high speed, high frequency and low noise applications. The high and low band gap heterojunction in the HEMT, made from group III-V materials, enables high electron mobility.

Furthermore, the existence of quantum well and 2DEG in un-doped channel layer enhances the carriers mobility where electrons can move freely and quickly without collision with any impurities.

2.3.2 HEMT Structure

As discussed previously, a sandwich of an un-doped low band gap and a doped high band gap material establishes a 2DEG structure, and therefore enables high electron mobility. Generally, a depletion-mode HEMT structure is as shown in Figure 2.8 below:
The source and drain metal contacts are on top of the cap layer, where the cap layer could be either un-doped or doped. In the above figure, an alloyed Ohmic contact is diffused down to the 2DEG, and provides a low resistance path between the 2DEG and metal contacts (Source and Drain in this case).

Under the cap layer are the supply layer, δ-doping and spacer layer. The supply layer could be either δ-doped or bulk doped - the difference is illustrated in Figure 2.9 below.
In Figure 2.9 above, energy quantization occurs at the discontinuity formed between the high and low band gap materials. Electrons in the supply layer (bulk doping case) or δ-doping (δ-doping case) can then tunnel through the thin potential barrier and be trapped in the triangular QW. The electrons in the QW form a high electron mobility plane called a 2DEG [33].

The Coulomb scattering between electrons and the fixed ionized atoms separated by the spacer layer leads to high mobility. This separation helps to improve the low
temperature (<100 K) carrier mobility [32]. However, there is always a trade-off between carrier density and mobility with the spacer layer thickness.

Lastly, the purpose of the buffer layer is to isolate any unwanted defects in the substrate surface, and also to de-couple it from the 2DEG.

Note that, in Figure 2.8, the gate metal contact is between the etched cap layers (gate recess process). The depletion region exists under the gate. When a negative gate electric field is applied, this region will broaden from the bottom of the gate towards the 2DEG, and the channel formed in the same location as the 2DEG region will be depleted - this is called a depletion mode device [32].

### 2.3.3 Principles of Operation

In a depletion mode HEMT, and referring to Figure 2.8, a depletion region will extend to the 2DEG region when a bias voltage is applied to the gate metal. The developed depletion region is actually due to the induced electric field when the bias voltage is applied. Hence, by adjusting the gate bias voltage, $V_{GS}$, the 2DEG concentration can be altered and therefore controls the channel current, $I_{DS}$.

Figure 2.10 below shows the relationship between two important terms in HEMT operation, which are the pinch-off voltage ($V_p$) and threshold voltage ($V_{th}$).
Figure 2.10 General $V_{GS}$ vs $I_{DS}$ graph (Depletion mode device) [31].

The condition when the channel current is at zero is called pinch-off voltage ($V_p$) as shown in Figure 2.10. This is because the 2DEG is completely depleted by the depletion region under the gate electric field. An increase in negative gate bias voltage ($-V_{GS}$) will push out some electrons from the already-formed quantum well (at $V_{GS} = 0$ for a depletion-mode HEMT), hence a decrease in the concentration of electrons in the channel, at an adequately-large negative $V_{GS}$ (i.e. at $V_p$), all electrons are driven out of the well, causing the sheet carrier density ($n_s$) in channel to become zero [34, 35]. Equation 2.8 and Equation 2.9 show the expressions for $V_p$ for bulk doping and δ-doping supply layer, respectively.

$$V_{p,bulk-doping} = \frac{qN_d d_1^2}{2\varepsilon_0 \varepsilon_s} \quad \text{Equation 2-8 [31, 36]}$$
Equation 2-9 [31]

\[ V_{p,\delta-doping} = \frac{q n_{\delta}^s d^*}{\varepsilon_0 \varepsilon_s} \]

Where \( q \) is the electron charge, \( N_D \) is the bulk carrier density, \( d_1 \) (as shown in Figure 2.9) is the distance between the gate metal (Schottky barrier) and the top of the spacer layer, \( \varepsilon_0 \) is the dielectric constant of vacuum, \( \varepsilon_s \) is the dielectric constant of the supply region (large-band gap region), \( n_{\delta}^s \) is the sheet carrier density in the \( \delta \)-doping region, and \( d^* \) (as shown in Figure 2.9) is the distance between the gate metal and the \( \delta \)-doping. Equations 2-8 and 2-9 show that, at a given fixed value of \( N_D \) and \( n_{\delta}^s \), the distances \( d_1 \) and \( d^* \), measured from the gate, determine the device \( V_{th} \) and hence the mode of operation of the device, as explained below.

The threshold voltage (\( V_{th} \)) is the starting point of current conduction between the source and drain in the channel at a predetermined particular value of current (as shown in Figure 2.10), or simply the point that determines whether the device is ON or OFF. Equation 2.10 below determines the value of \( V_{th} \).

\[ V_{th} = \frac{\Phi_b \Delta E_c}{q} - V_p \]  

Equation 2-10 shows that \( V_{th} \) is largely-influenced by the value of the barrier height \( \Phi_b \) and pinch-off voltage \( V_p \) (assuming a fixed \( \Delta E_c \) for a specific semiconductor heterojunction) i.e. \( V_{th} \) can be varied between negative and positive values, which later determine the operational modes of the HEMT, i.e. Depletion or Enhancement [31]. As previously discussed, a depletion-mode HEMT already has a channel at \( V_{GS} = 0 \) \( V \), and hence is known as a normally “ON” device, and has a negative value \( V_{th} \) (\( V_{th} < 0 \)). Conversely, a normally “OFF” device with a positive \( V_{th} \) value (\( V_{th} > 0 \)) is known as an enhancement-mode HEMT.
Furthermore, when $V_{GS}$ is made higher than $V_{th}$, the carrier density in the channel can be changed if the gate bias voltage is applied to the HEMT without changing the channel thickness. The sheet carrier density ($n_s$) can be calculated using Equation 2.11 below:

$$n_s(x) = \frac{C_i[V_{GS} - V_{th} - V_{DS}(x)]}{q}$$  \hspace{1cm} \text{Equation 2-11 [31, 32]}

Where $x$, is the direction of the drain-source electric field, $V_{DS}(x)$, is the applied drain-source electric field ($V_{DS} = 0$ at source side $V_{DS} = $ applied electric field at drain side), and $C_i$ is the gate channel capacitance, given by Equation 2.12:

$$C_i = \frac{\varepsilon_0 \varepsilon_s}{d_1 + d_2 + d_3}$$  \hspace{1cm} \text{Equation 2-12 [31, 32]}

Where $d_1$, is the supply layer thickness, $d_2$, is the spacer thickness, and $d_3$ is the channel thickness (as shown in figure 2.9). The most important characteristic of the HEMT operation is the channel current behaviour, where the two regions are usually the main areas of concern. Depending on the $V_{DS}$ magnitude, the channel current falls into two regions, called linear and saturation. The current behaviour in this channel is given by Equation 2.13 below:

$$I_{DS} = \frac{W}{L_g} \mu_n C_i [(V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}]$$  \hspace{1cm} \text{Equation 2-13 [31, 32]}

Where $L_g =$ gate length, $\mu_n =$ Carrier mobility in 2DEG.
Considering the condition when $V_{DS} \ll (V_{GS} - V_{th})$, the channel current will be in the linear region, and Equation 2.13 can be re-written as:

$$I_{DS} = \frac{W}{L_g} \mu_n C_i (V_{GS} - V_{th}) V_{DS}$$  \hspace{1cm} \text{Equation 2-14 [31, 32]}

Here $I_{DS}$ is shown to be linear with $V_{DS}$, and the corresponding channel resistance is given by:

$$R = \frac{L_g}{W \mu_n C_i} \times \frac{1}{V_{GS} - V_{th}} \frac{\Delta V_{DS}}{\Delta I_{DS}}$$  \hspace{1cm} \text{Equation 2-15 [31, 32]}

The relationship between $I_{DS}$ and $V_{DS}$ is shown in Figure 2.11:
As can be seen from Figure 2.11, when $V_{DS}$ increases to a positive value, the electric field at the drain side will rise rapidly, therefore the depletion region at the drain side increases. Hence, the average cross-sectional area for the $I_{DS}$ flow is reduced, which causes the channel resistance to increase; consequently $I_{DS}$ increases at a slow rate, and eventually saturates when $V_{DS} = V_{GS} - V_{th}$ (pinch-off point). This is the point where the source and drain are completely separated by the reversed-biased depletion region, but the large saturation $I_{DS}$ could flow across this depletion region [37]. Furthermore, as the $V_{DS}$ increases beyond this pinch-off point, the depletion...
region will extend from the drain side to the source side, and the pinch-off point will also move toward the source side [37]. Hence increasing the $V_{DS}$ will not increase the $I_{DS}$, which remains at the saturated value and does not depend on $V_{DS}$. This happens because the $V_{DS}$ value at the pinch-off point remains the same as it moves toward the source, which means that the potential drop in the channel from source to pinch-off point does not change [37]. This regime is known as the saturation region, where the $I_{DS}$ is not controlled by $V_{DS}$, but is influenced by $V_{GS}$. The corresponding equation for $I_{DS}$ in the saturation region is:

$$I_{DS} = \frac{W}{L} \mu_n C_i (V_{GS} - V_{th})^2$$  

Equation 2-16 [31, 32]

Another equally important parameter in the operation of the HEMT is the Transconductance ($g_m$), defined as the change in $I_{DS}$ in response to the change in $V_{GS}$ for a given $V_{DS}$. In Figure 2.11, it can be represented by the following Equations 2.17, 2.18 and 2.19:

$$g_m = \frac{\Delta I_{DS}}{\Delta V_{GS}}$$  

Equation 2-17 [31, 32]

$$g_{m, linear \ region} = \frac{W \mu_n C_i V_{DS}}{L_g}$$  

Equation 2-18 [31, 32]

$$g_{m, saturation \ region} = \frac{W \mu_n C_i (V_{GS} - V_{th})}{L_g}$$  

Equation 2-19 [31, 32]

Transconductance ($g_m$) is a measure of how much current gain a device can provide in response to a change in voltage input $V_{GS}$. The $g_m$ is also important in determining two very important frequency limit parameters, cut-off frequency ($f_T$) and maximum frequency of oscillation ($f_{max}$). The cut-off frequency, also called the unity gain frequency, is defined as the speed at which an electron can travel within a
distance \((L_g)\). In another words, it is the maximum frequency at which the device can operate with a current gain factor of “1”. Equation 2.20 describes the relationship between \(f_T\), \(g_m\) and parasitics [31]:

\[
f_T = \frac{g_m}{2\pi(C_{GD} + C_{GS})} = \frac{V_{sat}}{2\pi L_g}
\]

Equation 2-20 [31, 32]

Where \(C_{GD}\) is the gate-drain capacitance, \(C_{GS}\) is the gate-source capacitance, \(V_{sat}\) is the saturation velocity, and \(L_g\) is the gate length. However, when a device operates in saturation mode, \(C_{GS} \gg C_{GD}\) and the value \(C_{GD}\) may be neglected with respect to \(C_{GS}\) [32]. There is also a study that demonstrates that \(C_{GS}\) has a strong relationship to \(V_{DS}\), compared to the \(C_{GD}\) which is less-dependent on \(V_{DS}\) [38]. Note that \(f_T\) is proportional to \(g_m\), and inversely proportional to \(C_{GD}\) and \(C_{GS}\). Hence in practice, \(g_m\) is maximised when the parasitics are minimised.

The maximum frequency of oscillation - also known as the power gain frequency - is defined as the point in the frequency when power gain = 0 dB [31]. It is given by Equation 2.21:

\[
f_{max} = \frac{f_T}{2\sqrt{\frac{R_G + R_{ch} + R_S}{R_{DS}}} + f_T(2\pi R_G C_{GD})}
\]

Equation 2-21 [31, 32]

Where \(R_G\) = gate resistance, \(R_{ch}\) = channel resistance, \(R_S\) = source resistance, \(R_{DS}\) = drain-source resistance.
2.3.4 Pseudomorphic HEMT (pHEMT)

The pHEMT is an improvement over the HEMT; a pHEMT is basically engineered by growing a very thin and pseudomorphic material like In$_x$Ga$_{1-x}$As on top of the GaAs or InP substrates.

The GaAs channel in the GaAs-AlGaAs HEMT is changed to In$_{0.2}$Ga$_{0.8}$As in the pHEMT, and this leads to a double heterojunction structure and creates a rectangular QW rather than the triangular shape in the HEMT. Below are the benefits of the GaAs pHEMT compared to the GaAs/AlGaAs HEMT [32]:

1. More efficient carrier transport as higher conduction band discontinuity which then increases the 2DEG carrier density.
2. Extra heterojunction contributes to less carrier injection towards the buffer and substrate.
3. Higher low-field mobility in 2DEG due to the addition of Indium (In) component.
4. Reduced DX centres density because of lower Al content in the pseudomorphic structure supply layer.

2.4 MECHANISM OF REVERSE SCHOTTKY GATE LEAKAGE CURRENT

2.4.1 Introduction

The reverse Schottky gate leakage current consists mainly of the Off-state leakage current ($V_{GS} < V_{th}$ and channel-off mode) and On-state leakage current ($V_{GS} \geq V_{th}$ and channel-on mode). These two types of gate leakage currents are determined by gate-drain breakdown at high applied voltages. Figure 2.11 shows a HEMT’s I-V
characteristics; in the Off-state, the gate leakage current is dominated by the
tunnelling mechanism of gate electrons, while in the On-state, the gate leakage
current is dominated by the impact ionization mechanism of channel electrons. The
focus of this thesis is to minimize these types of leakage currents, and consequently
increase the breakdown voltage. The subsequent sections explain the physics of
leakage currents in HEMTs.

2.4.2 Current Transport Mechanism in Schottky Barrier

As mentioned in Section 2.2.2 (Schottky Contact), a Schottky barrier exists between
the gate metal and the semiconductor beneath it. The majority carrier (electrons in
this study) must overcome this barrier to travel from the semiconductor to the gate
metal, and vice-versa [25, 31]. There are three electron transport mechanisms which
are dominant through the Schottky barrier under forward and reverse bias
conditions, which are explained below [31, 39, 40]:

1. Thermionic Emission (TE): Electrons with sufficient energy to travel over
the top of the Schottky barrier with potential $\Phi_B$. This is the preferable
transport mechanism, and gives a near-ideal Schottky diode interface [40].
2. Thermionic Field Emission (TFE): Electrons with energy below the TE but higher than FE tunnel through the thinner top layer of the Schottky barrier.

Figure 2.12 Thermionic Emission (TE) transport mechanism under forward and reserve bias [31].

Figure 2.13 Thermionic Field Emission (TFE) transport mechanism under forward and reserve bias [31].
3. Field emission (FE): A pure tunnelling transport of electrons through the entire Schottky barrier, very near to the Fermi level.

Figure 2.14 Field Emission (FE) transport mechanism under forward and reserve bias [31].

2.4.2.1 Thermionic Emission in Schottky Barrier

Consider the case where the barrier height is much larger than the \( kT \) required for a Schottky contact to be formed, as mentioned in Section 2.2.2. Under the Thermionic Emission (TE) theory, Rhoderick [40] and Sze [31] state that when the net flow of current does not affect the thermal equilibrium at the interface where the emission occurs - i.e. near the metal-semiconductor interface - the current flow from the semiconductor to metal and vice-versa depends mainly on the barrier height.

However, under forward bias, the electrons need to travel from the semiconductor to the metal side; they must transit the depletion region through diffusion and drift
processes, and then be emitted over the Schottky barrier to get to the metal side. On the other hand, as the barrier height does not change under reverse bias for the electrons crossing over from metal to semiconductor, the general relationship of total current density \( J \) and the voltage \( V \) applied for this TE process is given by Equation 2.22.

\[
J = A^* T^2 \exp \left( \frac{-q \Phi_B}{kT} \right) \left\{ \exp \left( \frac{qV}{kT} \right) - 1 \right\}
\]

**Equation 2-22 [40]**

Where \( T \) is the absolute temperature in Kelvin, \( \Phi_B \) is the barrier height, \( q \) is the electron charge and \( k \) is the Boltzmann’s constant. While \( A^* \) is the effective Richardson constant for TE and given by below Equation 2.23.

\[
A^* = \frac{4\pi m^* q k^2}{h^3}
\]

**Equation 2-23 [40]**

Where \( m^* \) is the effective electron mass, \( h \) is Planck’s constant, \( q \) is the electron charge and \( k \) is Boltzmann’s constant. However, when taking into consideration the scattering and quantum mechanical interference, \( A^* \) could be reduced and termed as \( A^{**} \) [41].

### 2.4.2.2 Tunnelling in Schottky Barrier

Tunnelling through the Schottky barrier consists of two mechanisms: Thermionic Field Emission (TFE) and Field Emission (FE), as illustrated in Figure 2.13 and 2.14 in Section 2.4.2. These tunnelling mechanisms are deviations from the ideal
Thermionic Emission, where the electrons' energy is below that of the Schottky barrier height $\Phi_B$, yet they still penetrate through the barrier [40]. Both of these tunnelling mechanisms can be seen in both forward and reverse-biased conduction mechanisms. However, if these tunnelling effects are dominant in the forward bias condition, compared to Thermionic Emission (TE), they will also dominate in the reversed-biased region [42]. These tunnelling mechanisms are due to the heavily-doped nature of the semiconductor ($N_D > 1 \times 10^{17} \text{ cm}^{-3}$), which causes the depletion region to become sufficiently thin to enable the electrons to tunnel through the barrier. Basically, TFE dominates the reverse leakage current, as shown in a few studies [43-46], compared to the FE which is the pure tunnelling and ideal mode for metal-semiconductor Ohmic contacts. The thickness of the depletion region and the barrier height also depends on the supply/donor layer thickness, and the applied gate bias [43]. The increase in gate bias will also increase the electric field strength at the edge of the gate metal contact, and hence reduce the barrier height. As mentioned previously, the main tunnelling mechanism affecting reverse-biased gate leakage is determined by the TFE, which is given by Equation 2.24 below.

$$J = J_s \exp \left( \frac{V}{E_0} \right) \left\{ 1 - \exp \left( -\frac{-qV}{kT} \right) \right\}$$  \hspace{1cm} \text{Equation 2-24} [40]

Where $J_s$ is the saturation current, derived from a complicated function consisting of Schottky barrier height, temperature and other semiconductor parameters, as shown by Padovani and Straton [42], while $E_0$ is given by Equation 2.25:

$$E_0 = E_{00} \coth \left( \frac{qE_{00}}{kT} \right)$$  \hspace{1cm} \text{Equation 2-25} [40]
E₀₀ is an important tunnelling parameter which depends on material properties, as shown in Equation 2.26.

\[ E_{00} = \frac{q\hbar}{4\pi} \sqrt{\frac{N_D}{m^*\varepsilon_0\varepsilon_s}} \quad \text{Equation 2-26 [39, 40]} \]

Where \( q \) is the electron charge, \( \hbar \) is Planck’s constant, \( N_D \) is the donor concentration, \( \varepsilon_0 \) is the permittivity of the free space, \( \varepsilon_s \) is the specific permittivity of the semiconductor material, and finally \( m^* \) is the electron effective mass.

However, a better way to measure the relative deviation of TFE in the reverse-biased characteristic, compared to TE, is based on Equation 2.27 below:

\[ J = J_r \left\{ \exp \left( \frac{qV}{nkT} \right) - \exp \left[ \left( \frac{1}{n} - 1 \right) \frac{qV}{kT} \right] \right\} \quad \text{Equation 2-27 [39]} \]

Where \( J_r \) is the reverse current density, given by Equation 2.28 below:

\[ J_r = A^* T^2 \exp \left( \frac{-q \Phi_B}{kT} \right) \quad \text{Equation 2-28 [39]} \]

Equation 2.27 consists of both TE and TFE. The \( n \)-value is known as the ideality factor of the diode behaviour of a Schottky contact; when \( n = 1 \), the ideal mechanism is TE i.e. no tunnelling, leading to a TE equation as in Equation 2.22. The greater the value of \( n \), the greater the tunnelling compared to ideal TE, hence the greater the reverse gate leakage current.
2.4.3 Impact Ionization Mechanism

In the semiconductor channel, the impact ionization or Avalanche Multiplication occurs due to electron multiplication. This mechanism exists when the depletion region of the semiconductor experiences a large electric field with a large reverse bias voltage applied to the Schottky contact [47], and at certain point it gives the electron in the conduction band sufficient kinetic energy to knock an electron from the valance band to the conduction band via Coulombic interaction, and hence creates an electron-hole pair. The new electron-hole pair is then accelerated by the electric field, and creates more pairs by the same process. Furthermore, apart from the high electric field, the electron in the conduction band must have a minimum energy, slightly greater than the band gap energy, to excite the electron from the valence band to the conduction band under this impact ionization mechanism [31, 48]. Hence, it can be said that the impact ionization is inversely proportional to the energy band gap, i.e. the lower the band gap energy between the conduction band and valence band, the higher the impact ionization [31, 46]. Figure 2.15 illustrates the impact ionization process which generates an electron-hole pair.
Figure 2.15 Illustration of energetic electron generating electron-hole pair during impact ionization mechanism [48].

For the case of the reverse Schottky gate leakage current, the impact ionization dominates in the On-state, i.e. when $V_{GS} \geq V_{th}$ (the channel-on and conducting condition); this differs from the Off-state i.e. the Channel-off and non-conducting condition, where TFE dominate [49]. As the device is turned on, the electrons are first injected from the reverse-biased gate to the channel by Thermionic Emission (TE). These electrons flow through the high electric field region near to the gate-drain area, and through the conduction energy band gap between barrier and channel; these electrons are also known as “hot-electrons” when entering the channel as they releasing their energy by starting the impact ionization process, creating electron-hole pairs [46, 50]. The generated electrons will be swept into the drain and cause increase in drain current, while some holes will flow to the source and combine with electrons, and some other holes will be collected by the negatively-biased gate and increase the reverse gate leakage current in the form of a bell shape [46, 50, 51]. As the impact ionization rate increases with the increase in
the electric field, the reverse gate leakage current will increase dramatically. Equation 2.29 shows the gate leakage current or impact-ionization-induced current, while Equation 2.30 is the elaboration of impact ionization rate from Equation 2.29, where the definition of impact ionization rate comes from the number of electron-hole pairs generated by an electron per unit distance travelled [31]. Figure 2.16 illustrates the impact ionization process.

\[ I_{imp} = \alpha \Delta LI_{DS} \quad \text{Equation 2-29 [52, 53]} \]

\[ \alpha = A \exp \left( \frac{-TE_i}{V_{DG} - V_{th}} \right) \quad \text{Equation 2-30 [52, 53]} \]

Where, \( I_{imp} \) is the impact-ionization-induced current, \( \alpha \) is the impact ionization rate, \( \Delta L \) is the effective length of the high-field region at the gate-end, and the drain \( I_{DS} \) is the drain current, \( A \) is a constant which depends on the device design, \( T \) is the temperature, \( E_i \) is the ionization energy, \( V_{DG} \) is the drain-gate voltage and \( V_{th} \) is the device threshold voltage.

As can be seen from Equation 2.30, \( \alpha \) will increase exponentially with the increase in \( V_{DG} \), whereby an increase in \( V_{DG} \) will lead to an increase in the electric field near to the gate end nearest the drain [52]. Hence, \( \alpha \) is strongly-dependent on the electric field in the gate-drain region; the higher the electric field, the higher the impact ionization in the channel [31], as has been mentioned previously.
2.4.4 Other Mechanisms

Apart from the main reverse gate leakage current mechanisms described above, under normal bias conditions, not only do undesired electrons flow from the source to the drain through the substrate, but injection of hot electrons also occurs beyond the 2DEG into the buffer [36, 48, 54]. As these electrons are far from the gate, the modulation of the gate is not efficient, leading to both excess reverse gate leakage current and eventually a low gate-drain breakdown voltage [55]. Furthermore, the holes from the impact ionization in the channel also create a leakage path to the buffer; the holes accumulated in the buffer will act as a fixed positive charge, and enhance hot electron injection to the channel and buffer [56]. Hence the buffer improvement also plays a significant role to counter these leakage mechanisms.
2.4.5 Material Design Impact on Reverse Gate Current Leakage

As mentioned previously, the main contributors of the reverse Schottky gate current leakage in the Off-state are the TFE and Impact ionization, in addition to some other leakage mechanisms. There are many ways to address these problems, as will be discussed in the later chapters of this thesis, but the main improvements are as follows (taking InP-based In$_x$Ga$_{1-x}$As-In$_x$Al$_{1-x}$As HEMT material as a reference):

1. An In$_x$Al$_{1-x}$As wide band gap barrier layer material with low Indium content $\approx 30\%$ will increase the barrier height $\Phi_B$, and hence reduce the TFE and holes collection at the gate.

2. The increased thickness of In$_x$Al$_{1-x}$As wide band gap spacer layer helps to reduce the number of holes generated from impact ionization due to tunnelling to the gate. It also degrades the efficiency of electron transfer from the donor to the channel and hence minimize the rate of impact ionization.

3. The high Indium content of 70% in the low-band-gap In$_x$Ga$_{1-x}$As channel, plus the double-delta doping above and beneath the channel, gives a deeper and more-confined quantum well, which help to reduce TFE.

4. The improvement of the In$_x$Al$_{1-x}$As buffer layer by growth at low temperature increases this layer’s resistivity, and improves the Off-state and On-state gate current leakages.
CHAPTER 3

OPTIMIZATION OF 1 µm GATE LENGTH InGaAs-InAlAs pHEMT

3.1 INTRODUCTION

The gate length plays an important role in the device’s maximum unity current gain cut-off frequency ($f_T$) and maximum oscillation frequency ($f_{\text{max}}$). Theoretically, to obtain a gate length of 1µm, the resist opening must be a 1 µm wide (using negative resist in this case). After the coat-expose-develop process, a high magnification image of the device shows an opening that became 13% larger after metal evaporation, as shown in Figure 3.1. This enlargement is due to both the resist thickness and profile [57], the thicker the resist, the larger the gate length feature as illustrated in Figure 3.2.

Figure 3.1 Gate opening dimensions after coat-expose-develop process, and after metallization.
The bottom footprint of the gate length determines the $f_T$, hence - after metallization - the gate length is not 1 μm as initial opening of the resist. The so called flat gate length is actually a trapezium shape, hence to achieve a 1 μm gate length, it is necessary to reduce the size of the opening by 13%. It was therefore also necessary to reduce the AZ®nLOF™ 2070 negative resist film thickness by at least 13%. As will be demonstrated later, the reduced resist film thickness can help to obtain a smaller opening, with exposure optimization.
3.2 NEW RESIST MIX DEVELOPMENT

As mentioned in the Introduction, the resist used to define the pHEMT gate length is AZ®nLOFTM 2070, which is negative resist. As the current resist thickness is 1 μm, achieving a 1 μm gate length would require a sub-μm range capability resist such as AZ®nLOFTM 2020, which is more expensive. One alternative is to dilute the AZ®nLOFTM 2070 resist with AZ® EBR solvent; dilution theoretically allows the changing of a resist thickness to different film thickness using the same coating parameters.

3.2.1 Resist Preparation Technique

The dilution ratio of AZ®nLOFTM 2070 negative resist with AZ EBR is based on Figure 3.3. The dilution of AZ®nLOFTM to EBR solvent must be done carefully to preserve a high resolution and reproducible undercut profile for the later lift-off process.
The graph in Figure 3.3 shows the film thickness of AZ®nLOF™ 2070 achieved with standard in-house coating parameters i.e. 3000 rpm spin speed and then soft-bake at 110 °C on a hotplate for 1 minute. As can be seen from the graph, without any dilution, the film thickness of AZ®nLOF™ 2070 is 7 μm and the minimum film thickness which can be achieved for this type of resist after dilution is 0.5 μm, with a 1:1 ratio of the AZ®nLOF™ 2070 to AZ EBR solvent. Note that the supplier only provides the 7 μm and 2 μm grade of AZ®nLOF™ resist; to achieve 1 μm and below, diluted grades are produced in-house. Table 3.1 gives clearer information to describe the graph in Figure 3.3, where 20 grams of AZ®nLOF™ 2070 used for each added gram of AZ EBR solvent.
Table 3-1 Amount of AZ EBR solvent added to 20 grams of AZ®nLOF™ 2070.

<table>
<thead>
<tr>
<th>AZ®nLOF™ 2070 (g)</th>
<th>AZ EBR Solvent (g)</th>
<th>Total Weight (g)</th>
<th>AZ 2070 : EBR Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>20</td>
<td>0</td>
<td>20</td>
<td>0.00</td>
</tr>
<tr>
<td>20</td>
<td>8</td>
<td>28</td>
<td>1.00 : 0.40</td>
</tr>
<tr>
<td>20</td>
<td>15</td>
<td>35</td>
<td>1.00 : 0.75</td>
</tr>
<tr>
<td>20</td>
<td>20</td>
<td>40</td>
<td>1.00 : 1.00</td>
</tr>
</tbody>
</table>

Only AZ®nLOF™ 2070 2 μm grade resist is available in-house, therefore to get a sub-μm range film thickness from this resist requires manipulation of the total weight from Table 3.1 as shown below.

Total Weight of AZ®nLOF™ 2070 2 μm = 28 g

Total Weight of AZ®nLOF™ 2070 0.5 μm = 40 g

Total Weight difference of above 0.5 μm and 2 μm grades = 12 g

Hence to get a 0.5 μm film thickness from AZ®nLOF™ 2070 2 μm grade instead of using AZ®nLOF™ 2070 itself, 12 g of AZ EBR solvent is added to 28 g of AZ®nLOF™ 2 μm resist.

The next step is to follow the mixing procedure for the 2 μm grade AZ®nLOF™ 2070 resist and the calculated amount of AZ EBR solvent. The procedure is done using the in-house clean room, and need a bottle which has been cleaned with Acetone and IPA. The mixing method is straightforward but needs to be done carefully to avoid over-dilution. The empty bottle is placed on the Adventurer analytical balance with precision of 0.1 mg, then 28 g of AZ®nLOF™ 2070 2 μm grade resist is added to the bottle. Then 12 g of AZ EBR is carefully added, possibly
drop by drop using plastic Pasteur pipettes to dilute it. After a total weight of 40 g is achieved from the newly mixed resist, it undergoes an hour of degassing in an ultrasonic bath. Finally, the new resist is allowed to stabilize for about 3 days to ensure it is properly mixed and has no bubbles in it. This new resist is simply called AZ 0.5 μm.

### 3.2.2 Exposure Experiment

After a 3 day degassing and stabilization period of the newly mixed AZ 0.5 μm, it is ready to be used to define the pHEMT gate length. For later comparison purposes, the coating parameters remained similar to those for the standard 1 μm gate length process i.e. coater’s spin speed of 3000 rpm and soft bake at 110 °C for 1 min. However the exposure time and development time need to be optimized to achieve the desired sub-μm range opening - Table 3.2 show the detailed parameters used in this experiment. The experiment was performed using silicon samples and a standard 1 μm mask, as shown in Figure 3.4. After development, these samples were inspected under a microscope to check for quality i.e. yield of the opening, then measured under a high-power microscope – the results are shown in Table 3.3

<table>
<thead>
<tr>
<th>Parameters</th>
<th>New AZ 0.5 μm</th>
<th>Standard AZ 1 μm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Coating Spin Speed (rpm)</td>
<td>3000</td>
<td>3000</td>
</tr>
<tr>
<td>Soft-bake (°C) for 1 min on Hot-plate</td>
<td>110</td>
<td>110</td>
</tr>
<tr>
<td>Exposure (s) @ intensity 0.9 mW / cm²</td>
<td>12</td>
<td>X (3 to 12)</td>
</tr>
<tr>
<td>Post-bake (°C) for 1 min on Hot-plate</td>
<td>110</td>
<td>110</td>
</tr>
<tr>
<td>Development time (min)</td>
<td>5</td>
<td>1</td>
</tr>
</tbody>
</table>
Figure 3.4 Mask for 1 µm gate length opening for exposure experiment.

Table 3-3 Results and yields for exposure experiment with AZ 0.5 µm resist.

<table>
<thead>
<tr>
<th>Exposure time (s)</th>
<th>Development time (s)</th>
<th>Opening 1 µm feature (µm)</th>
<th>Yield (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>60</td>
<td>1.51</td>
<td>100</td>
</tr>
<tr>
<td>4</td>
<td>60</td>
<td>1.51</td>
<td>100</td>
</tr>
<tr>
<td>5</td>
<td>60</td>
<td>1.45</td>
<td>100</td>
</tr>
<tr>
<td>6</td>
<td>60</td>
<td>1.25</td>
<td>100</td>
</tr>
<tr>
<td>7</td>
<td>60</td>
<td>1.15</td>
<td>100</td>
</tr>
<tr>
<td>8</td>
<td>60</td>
<td>0.97</td>
<td>100</td>
</tr>
<tr>
<td>9</td>
<td>60</td>
<td>0.82</td>
<td>100</td>
</tr>
<tr>
<td>11</td>
<td>60</td>
<td>0.85</td>
<td>&lt; 40</td>
</tr>
<tr>
<td>12</td>
<td>60</td>
<td>0.55</td>
<td>&lt; 30</td>
</tr>
</tbody>
</table>
As can be seen from Table 3.3, the smallest opening achieved with 100 % yield is roughly 0.8 μm. The exposure time was stopped at 12 s, mainly because the standard 1 μm process exposure time is 12 s, and the yield became very low as shown in the table. The poor yield with the newly mixed resist may be due to the preparation method and the clean room humidity. In addition, during dilution there may be a possibility that the mixing speed was not quick enough as mentioned in the AZ®nLOFT™ application note [58], since slow mixing can lead to particle formation. Furthermore, the low yield may also be due to the limitations of this type of resist. To go further into the sub-μm range, a much higher resolution resist is required, i.e. AZ®nLOFT™ 2020 as mentioned earlier in this chapter.

The 9 s exposure time samples were checked again for repeatability, and the gate length metallization was performed. Figure 3.5 show the comparison of gate length metallization using AZ 1 μm using standard process and AZ 0.5 μm using an optimized process.
Referring to Figure 3.5, the 1 μm opening with AZ 0.5 μm resist has been reduced by 19.6 % after development, compared with the standard AZ 1 μm resist. Furthermore, after metallization, it is possible to achieve nearly 1 μm gate length, and with almost the same reduction factor, 19.1 %. Observe also that the gate length feature increased by about 13 % after metallization for both resist runs, which explains the AZ negative resist profile as shown in Figure 3.2. As the smooth and reproducible lift-off process depends strongly on the undercut profile, the newly-mixed AZ 0.5 μm has demonstrated this quality. This optimization has concluded that it is possible to get a nearly sub-μm range gate opening using a diluted resist, and at the same time retaining a high resolution and undercut profile. However, due to the metal thermal evaporation limitation, the final gate length dimension increased, but still contributed to improvement of the $f_T$, which will be demonstrated in a later section of this chapter.
3.3 DEVICE MATERIAL GROWTH AND FABRICATION

To further study the performance of the newly mixed AZ 0.5 μm negative resist, it was necessary to fabricate a device and to analyze its DC and RF performance, and to compare them with a standard AZ 1 μm negative resist. The chosen device is VMBE#1998, for which the epitaxial layer are grown in-house at the University of Manchester. The prefix VMBE is used to indicate that it is grown using a solid-source MBE V90H system.

3.3.1 Epitaxial Layer Growth Introduction and Technique

The growth of two dissimilar semiconductors on adjoining surfaces causes abruptness of the heterojunction interface. The discontinuities at the heterointerface are fundamental to the production of quantum wells for electronic devices. However, the growth of such heterojunctions would not be possible without the evolution and major advances in material technology; in this study, the term ‘advanced materials’ refers to group III-V compound semiconductors. There are a number of common growth techniques used to produce epitaxial layers [59], but only two techniques are generally used to grow HEMT and pHEMT layers: Molecular Beam Epitaxy (MBE) and Metal-Organic Chemical Vapour Deposition (also known as Metal-Organic Vapour Phase Epitaxy-MOVPE). Below are some of the key features for each of these techniques.

**Molecular Beam Epitaxy (MBE):**

The epitaxial layers are grown on a heated substrate, with reactants which are introduced by elemental or molecular beams; the beams are created by the heating of source elements in an effusion (e.g. a Knudsen cell for solid-source MBE). The chamber environment is always under ultra-high vacuum (UHV) conditions, to
ensure not only the purity of the starting materials but also the grown epitaxial layers. Moreover, under UHV, the molecular or elemental beam travels in a straight path directly to the heated substrate. As multiple material layers are involved, several beams from several different material sources (such as Si, In, Ga, As, Be) can be aimed at the heated substrate [60].

**Figure 3.6 Schematic diagram of basic MBE system [61]**

To achieve variation in layer thickness, doping and composition, there is a mechanical shutter in front of each source, to interrupt the evaporated beam in periods of less than one second. Together with a defined and low growth rate (1um h$^{-1}$ or roughly one atomic layer per second or less) for MBE, and by controlling the source temperature and rapid on/off control of the shutters, the growth of ultra-thin layers and excellent abruptness of the interfaces can be achieved.
As the chamber environment is kept at UHV, it is possible to monitor in-situ growth thickness. The most commonly-used technique to monitor the thickness is Reflection High-Energy Electron Diffraction (RHEED).

**Metal Organic Chemical Vapour Deposition (MOCVD):**

This type of epitaxial growth technique also has the capability to grow thin layers and monolayers, creating abrupt interfaces between heterojunctions. Similar to MBE, the epitaxial layers are grown on a heated substrate, but the major difference is that the sources are complex compound i.e. metal-organic sources (e.g. Ga, In, Al etc), hydrides (e.g. AsH$_3$ etc.) and other gas sources like Silane (SiH$_4$).

The epitaxial layer growth depends on the reactant’s chemical reaction at the surface of the heated substrate, where it is transported to the heated substrate by a carrier gas (usually H$_2$). Unlike MBE, an MOCVD chamber environment is highly pressurized, and the layer structures of the epi-layer are controlled by the flow of the gases.

![Schematic diagram of basic MOCVD system](Image)

**Figure 3.7 Schematic diagram of basic MOCVD system [62].**
One advantage of MOCVD over MBE is its high growth rate, typically 5 μm h\(^{-1}\) to 25 μm h\(^{-1}\) [60]. The major drawback of the MOCVD technique is that it requires not only high-purity gas sources, but also the use of highly-toxic and flammable gases such as Silane (SiH\(_4\)) and Arsine (AsH\(_3\)), which makes the safety precautions for handling and waste management more complex.

**Why MBE for pHEMT?**

Practically, the production of HEMT and pHEMT epitaxial layers is dominated by MBE growth techniques, whereas MOCVD is less commonly used. The reason for this is that MBE can produce very smooth interfaces between the grown layers, and also the doping and composition in the layers can be abruptly changed. Furthermore, solid-source MBE is favourable to grow pHEMT epitaxial layers, because the source elements such as Indium, Aluminium, Arsenic, Silicon and Gallium required can easily be obtained as very high purity ingots and solids, at or near room temperature. Hence the pHEMT layers described in this chapter and subsequent chapters were produced using solid-source MBE. The method allows the growth of the high-purity layers needed for pHEMT structure fabrication, especially for the large and small band-gap layers, since it is possible to minimize impurity scattering, which can impede the performance of the 2DEG [63].

Furthermore, the epitaxial structures grown by MBE show excellent uniformity compared to MOCVD [64]: excellent layer thickness uniformity of the alloys composition, as well as the tight control of dopant concentration, are crucial to pHEMT device fabrication. For instance, one of the important parameters for the pHEMT is the threshold voltage (\(V_{th}\)), as discussed in Chapter 2, which is related to the distance from the gate (after gate recess and metallization) to the In\(_x\)Ga\(_{1-x}\)As channel. Hence, variations in layers thickness and alloy composition will alter the device threshold voltage.
3.3.2 Material Epitaxial Growth

The material growth of VMBE#1998 is basically a lattice matched to InP pHEMT with highly tensile channel, with a double Silicon delta-doped (δ-doped) and a highly doped cap. Figure 3.8 illustrates the epi-layer with a detailed explanation of the layers from bottom to top (substrate to cap layer).

![Epitaxial layer structure for VMBE#1998 grown in-house using a V90H MBE machine (thickness not to scale).](image)

VMBE#1998 uses a semi-insulating InP substrate doped with Iron (Fe). On top of this is a 4500 Å thick InAlAs buffer layer, which is lattice-matched to the InP; this buffer layer is grown relatively thick compared to the other layers on top of it, to avoid any unwanted impurities originating from the substrate diffusing upwards,
especially into the channel. As this structure incorporate a double silicon δ-doping, there are 2 lattice matched 100 Å-thick InAlAs Spacer layers protecting the non-lattice matched - but highly strained - pseudomorphic In$_{0.7}$Ga$_{0.3}$As channel from coulomb scattering. On top of the second spacer layer is the barrier layer which also lattice-matched to InP. This layer is grown 150 Å thick, and later used to form the Schottky contact to the gate metal. Finally the upper-most layer grown is also a lattice-matched InGaAs cap layer of thickness 200 Å. This cap layer is highly doped, with doping concentration (n) of 2x10$^{19}$cm$^{-3}$, allowing the formation of a low-resistivity Ohmic contact through Source and Drain metallization.

### 3.3.2.1 Hall Effects Measurements and Band Diagrams

The quality of the VMBE#1998 epilayer is determined by Hall Effect measurement; this measures the epilayer 2DEG electron mobility and its sheet carrier concentration - shown in Table 3.4.

| Table 3-4 VMBE#1998 epilayer Hall Effect measurement data. |
|-----------------------------------|-----------------|
| Measurement                        | Data            |
| Sheet Carrier Concentration (n$_H$) at 300 K / 77 K (x10$^{12}$ cm$^{-2}$) | 2.40 / 2.50     |
| Hall Mobility (μ$_H$)               |                 |
| at 300 K / 77 K (cm$^2$/V.s)        | 13896 / 47829   |

Table 3.4 show that at 300 K, i.e. room temperature, the Hall mobility in the 2DEG was 13896 cm$^2$/V.s – this is a better figure than that reported for other InP [65, 66] and GaAs [67, 68] pHEMTs.
Figure 3.9 Energy band diagram of VMBE#1998 structure ($V_{GS} = 0, V_{DS} = 0$).

The energy band diagram of this epilayer shown in Figure 3.9 was simulated using the WinGreen® program [69]. The double-sided δ-doped structures gives good carrier confinement in the 2DEG quantum-well, which reflects the excellent mobility shown in Table 3.4. Correspondingly, the double-sided doping gives not only high current handling capability, but also better linearity in high-power applications.

### 3.3.3 Device Fabrication (AZ 0.5 μm Vs AZ 1 μm)

To further study the outcome of the use of both resists, the DC and RF results will be analyzed and compared. Here, two samples of VMBE#1998 are fabricated side-by-side to minimize uncertainty where possible.
The standard fabrication process flow is shown in Figure 3.10 for the two samples; the fabrication steps were the same throughout the process except during coat-expose-develop gate length step. At this gate length step, AZ 0.5 μm and AZ 1 μm negative resists were used on each sample respectively, using the process parameters are recorded in Table 3.2.

### 3.3.4 Direct Current (DC) Characteristics

The DC performance of the 2 samples was measured after the Ohmic metallization step and after bond pad metallization. After Ohmic metallization, the measurement
of particular interest is the quality of the contact resistance ($R_c$) of the Ohmic contact, as well as the sheet resistance ($R_{sh}$), measured via the Transfer Length Method (TLM) which had been explained in detail elsewhere [70]. Prior to TLM measurement, both of the samples were annealed in an N$_2$ environment, in a furnace at 280 °C for 90 s. The TLM measurement was then performed using 4 point-probes on a test pad structure of size 50 μm length x 100 μm width; the pads were structured in an array of different spacing from 5 μm to 45 μm on the cap layer – the results are shown in Table 3.5, Figure 3.11 for AZ 0.5 μm and Figure 3.12 for AZ 1 μm.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Sample 1 (AZ 0.5 μm)</th>
<th>Sample 2 (AZ 1 μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{sh}$ (Ω/□)</td>
<td>77</td>
<td>78</td>
</tr>
<tr>
<td>$R_c$ (Ω.mm)</td>
<td>0.052</td>
<td>0.046</td>
</tr>
</tbody>
</table>

Figure 3.11 Plot of total resistance vs TLM pad spacing including error bars for AZ 0.5 μm.
Figure 3.12 Plot of total resistance vs TLM pad spacing including error bars for AZ 1 μm.

Both samples were metalized at the same time under the same thermally evaporated metallization scheme i.e. 50 nm AuGe followed by 100 nm Au, therefore as expected, the sheet resistance ($R_{sh}$) and the contact resistance ($R_c$) for both samples were very similar. The very low $R_{sh}$ value is a result of both the high carrier concentration and the high mobility of electrons, as shown in the Hall Effect measurement data in Table 3.4, and hence demonstrates that the 2DEG is very well confined in the channel. Meanwhile, the very low $R_c (< 0.2 \, \Omega/mm)$ indicates a very good Ohmic contact, which also reflects that the AuGe is diffused deeply into the 2DEG channel. A low $R_c$ is very important for MMIC devices, as a large $R_c$ will limit the drain current and increase the source resistance ($R_s$), and therefore degrade the device performance.
As mentioned previously, the DC measurements were performed after bond pad metallization. Unlike TLM measurement, the DC measurements are more complex and produce more data to analyse. The measurements were performed using a Cascade Ground-Signal-Ground (G-S-G) 3-pin probe station, as shown in Figure 3.13, which was connected to an HP-Agilent 4142B Modular DC Source. The metallization for the bond pads was 50 nm Ti followed by 450 nm Au - the same as for the gate. Comparatively, the Au is thicker than that in the Ohmic contacts, to reduce the gate resistance during microwave or RF measurement later on. The pHEMT devices were measured at room temperature on devices with two gate fingers, with gate width of 2 x 200 μm (400 μm) and with 5 μm Source-to-Drain spacing.

![Figure 3.13 DC and RF measurements on VMBE#1998’s pHEMT samples.](image)

Note that all of the DC results shown hereafter are the average value across several measured devices, furthermore, the values are normalized to the device gate width. In addition, as mentioned previously, all of the DC results presented are to compare
the performance between two VMBE #1998 pHEMT samples, with the gates masked using both the newly mixed AZ 0.5 μm and standard AZ 1 μm resist respectively, while the rest of the fabrication processes were similar. To begin with, Figure 3.14 shows the output characteristic or the current-voltage (I-V) curves, biased at $V_{GS} = 0$ V to -1.2 V with 0.12 V step size, top-down. Both devices demonstrate well-behaved curves with excellent pinch-off characteristic. At biasing $V_{DS} = 1$ V, the measured drain saturation current $I_{dss}$ at $V_{GS} = 0$ V for this depletion mode pHEMT shows that the new AZ 0.5 μm resist gives a higher current density than the standard AZ 1 μm - 337 mA/mm (± 1 mA/mm) and 309 mA/mm (± 1 mA/mm) respectively; this improvement of about 10% is due to the shorter gate length as shown in Figure 3.5.

The improvement in current density is not statistically significant, since it may include errors in the measurement; to be statistically significant, the improvement target should be more than 20% [71]. However, it shows that reduction of the gate length leads to an increasing in $I_{DS}$, based on the $I_{DS}$ Equation 2-16 in the saturation region, where $I_{DS}$ is inversely proportional to the gate length $L_g$. The 10% increase was also expected as the gate length reduction is just 20% i.e. from 1.15 μm to 0.93 μm (Figure 3.5), based on the $I_{DS}$ Equation 2-16, while the rest of the parameters remain the same because of the similar epilayer structures, gate width and fabrication process used for both samples. The only parameter that has an impact on $I_{DS}$ is $L_g$, hence if the gate reduction is 50% or more, then the $I_{DS}$ improvement or increment is significant, provided that a similar epilayer and fabrication process is used. Furthermore, in the linear region of the curves, the inverse of the I-V slope determines the ON resistance ($R_{on}$), which is very similar for both devices, due to the similar epilayers and gate widths. Both curves show very minimal ‘kink effect’ when the devices were biased in the low $V_{DS}$ region i.e. from $V_{DS} = 0.5$ V to 1 V. Furthermore, the kink effect is better than that exhibited by a similar structure reported in [72], due to better electron confinement in the 2DEG from the double δ-doped structure in the VMBE#1998 epilayer design. Even though the kink effect is
minimal in both of the samples, the new AZ 0.5 μm sample shows more of this effect due to the shorter gate length [73], hence it has a higher output conductance, where the output conductance $g_o$ taken at $V_{DS} = 1$ V to 2 V gives 47.7 mS/mm for AZ 0.5 μm and 35.4 mS/mm for AZ 1 μm. The typical value of $g_o$ for an InP HEMT is about 50 mS/mm for a highly-doped cap and short gate length [74].

![Figure 3.14 Output characteristics of pHEMTs with new and standard resist with 2 x 200 μm gate width.](image)

The next DC characteristics to be considered are the Threshold Voltages ($V_{th}$), as shown in Figure 3.15. The linear extrapolation from the square root of $I_{DS}$ vs. $V_{GS}$ at $V_{DS} = 1$ V gives values of -0.90 V and -0.88 V for the new AZ 0.5 μm and standard AZ 1 μm respectively. The threshold voltage of the AZ 0.5 μm device is 2.3% lower than the AZ 1 μm device, but this is considered as comparable. This conclusion is supported by the fact that both devices have the same pinch off characteristic, as

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shown in Figure 3.14, due to the same epilayer structure and gate recess conditions used.

Figure 3.15 Threshold voltage ($V_{th}$) at $V_{DS} = 1$ V of pHEMTs with New and Standard resist with 2 x 200 µm gate width.

Figure 3.16 shows the Extrinsic Transconductance ($g_m$), which is derived from the I-V curve in Figure 3.14. This parameter is important in order to show how the gate controls the drain current; this parameter can be improved (increased) when the gate length becomes shorter [34]. The Extrinsic Transconductance ($g_m$) vs. $V_{GS}$ biased at $V_{DS} = 1$ V shows two maximum $g_m$ ($g_{m_{max}}$) points, one at $V_{GS} = -0.4$ V ($g_{m_{max}} = 512$ mS/mm) and the other one at $V_{GS} = -0.22$ V ($g_{m_{max}} = 501$ mS/mm) for the new AZ 0.5 µm and standard AZ 1 µm respectively. The slight increase is expected for AZ 0.5 µm, because of the higher saturation current ($I_{DSS}$) as shown in Figure 3.14. Another key point to note is the shift in the curve of AZ 0.5 µm with a reduced gate length, which is consistent with the drop in $V_{th}$ and increase in $g_o$ - mentioned previously. The intrinsic transconductance ($g_{mi}$) is inversely proportional
to the gate length ($L_g$), and also to the gate-to-channel distance; these are the important physical parameters that control the intrinsic $g_{mi}$ [75, 76]. Equations 3.1 and 3.2 show the relationship of the intrinsic transconductance to the physical and geometrical parameters.

$$g_{mi} = \frac{\varepsilon}{d} V_{sat} = \frac{C_g}{L_g} V_{sat} \quad \text{Equation 3-1 [75, 76]}$$

$$\frac{C_g}{L_g} = \frac{\varepsilon}{d} \quad \text{Equation 3-2 [75, 76]}$$

Where $\varepsilon$ is the dielectric constant, $d$ is the gate-to-channel distance, $V_{sat}$ is the saturated or peak electron velocity, and $C_g$ is the intrinsic gate capacitance.

Figure 3.16 Extrinsic transconductance ($g_m$) at $V_{DS} = 1V$ of pHEMTs with new and standard resist with 2 x 200 µm gate width.
The final DC characteristic to consider in this analysis is the gate current leakage, which is illustrated in Figure 3.17, when the device is in the pinched-off condition. The plot shows the gate current (I_{GS}) on a logarithmic scale, vs. gate voltage (V_{GS}). Such a graph is also called the off-state Schottky gate leakage current, which consist of two significant curves: forward-biased (V_{GS} = 0 to 1 V) and reverse-biased (V_{GS} = 0 to -4 V). The forward-biased curve from the I_{GS} vs. V_{GS} shows no dissimilarity between the new AZ 0.5 μm and standard AZ 1 μm, hence the Ideality Factor (η) and Barrier Height (Φ_B) extracted from this curve are similar at 1.58 and 0.36 eV. The reason for this similarity is that both devices have the same epilayer design, and have undergone the same gate recess step and gate metallization scheme.

Conversely, the reverse-biased curve is significantly different between the two devices. The reversed-biased curve is actually the Schottky gate reverse current, which importantly determines the gate current leakage and gate-drain breakdown voltage (BV_{DG}), with the gate current reaching a maximum value of 1 mA/mm during the off-state condition [51]. It is important to note that, for this case, the gate-drain breakdown voltage is the same as the gate-source breakdown voltage, as the fabricated devices have symmetrical geometry i.e. 2x200 μm gate width with 5 μm source-drain separation, hence the off-state breakdown will only be referred as breakdown voltage (V_{BR}). As can be seen clearly from the graph in Figure 3.17, a very low breakdown voltage was observed for the fabricated devices, as well as high gate current leakages. This will impede the device performance for low noise millimetre-wave MMIC (Monolithic Microwave Integrated Circuit) and high power millimetre-wave application devices. This poor performance is due to the low barrier height, which is expected to be ~ 0.5 eV for In_{0.52}Al_{0.48}As with Ti as the bottom metal [77], causing tunnelling or thermionic-field-emission (TFE) across the Schottky barrier [44, 52]. Furthermore, the AZ 0.5 μm device shows a higher gate leakage and low breakdown voltage compared to standard AZ 1 μm, due to the shorter gate length [78, 79] however the increased leakage is still low and even at -5 V it is only a factor of 2 higher.
The higher gate leakage for shorter gate lengths is due to the increase in electric field strength in the gate-drain region, considering the same applied bias or supply voltage [1]. Note that the critical-electric field $E_c$ is defined for the electrons to reach their saturation velocity [80], hence for the shorter gate length, the magnitude of the electric field in the channel is greater than $E_c$. For that reason, the electrons in this high-field region will be accelerating at a higher velocity, and become very “hot”, or highly-kinetic. These hot electrons can then be injected into the barrier, and cause gate current leakage [1].

![Figure 3.17 Off-state Schottky gate leakage current of pHEMTs with New and Standard resist with 2 x 200 µm gate width.](image)
3.3.5 Radio Frequency (RF) Characteristics

The final step in assessing the performance of the optimized resist compared to the standard is to perform microwave measurements. The measurement is performed as shown in Figure 3.13, with a 3-pin Cascade G-S-G probe station, with the measurements taken using the Vector Network Analyzer (Anritsu VNA HP-Agilent 8510C). The Radio Frequency (RF) figure of merit from this measurement is the cut-off frequency ($f_T$). For the devices concerned, the VNA sweep frequency was from 45 MHz to 20 GHz, and the small signal properties were extracted when biased at their maximum $g_m$, $V_{DS} = 1$ V and at $V_{GS} =$ device’s $g_{mm}$max. The details of the biasing and results for the two devices are shown in Table 3.6.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>New AZ 0.5 μm</th>
<th>Standard AZ 1 μm</th>
</tr>
</thead>
<tbody>
<tr>
<td>$g_{mm}$max (mS/mm)</td>
<td>512 ± 5</td>
<td>501 ± 5</td>
</tr>
<tr>
<td>$V_{GS}$ (V)</td>
<td>-0.40 ± 5</td>
<td>-0.22 ± 5</td>
</tr>
<tr>
<td>$I_{DS}$ (mA/mm)</td>
<td>161.6 ± 1</td>
<td>214.7 ± 1</td>
</tr>
<tr>
<td>$f_T$ (GHz)</td>
<td>26 ± 1</td>
<td>20 ± 1</td>
</tr>
</tbody>
</table>

Graphically, Figure 3.18 illustrate the $f_T$, showing the $f_T$ with the -20 dB / decade slopes crossing the 0 dB line on a graph of current gain vs frequency (on a logarithmic scale).
Observations from Figure 3.18 show a significant improvement from using the new AZ 0.5 μm negative resist, as the $f_T$ was improved by 30% compared with the standard AZ 1 μm negative resist, where the improvement correlates with the reduction in gate length after metallization, as shown in Figure 3.5.

### 3.3.6 Gate Recess Experiments

In addition to assessing the new resist performance, the high off-state Schottky gate leakage and low breakdown voltage shown in Figure 3.17 for VMBE#1998 also need to be investigated. The high gate current leakage and low breakdown voltage
will impede the performance for future low-noise and high-power applications. Hence, apart from the tunnelling and TFE mechanisms mentioned previously, the gate recess may contribute to the performance issues. The footprint of the gate length is defined by the gate recess, while the gate recess width is theoretically defined by the opening of the resist (AZ 0.5 μm in this case). The gate recess is required to remove the highly doped In$_{0.53}$Ga$_{0.47}$As cap so that the Ti/Au metal gate metallization can form a Schottky contact with the exposed In$_{0.52}$Al$_{0.48}$As Schottky barrier layer. The cap is removed by an in-house developed selective succinic acid [70], but this has been optimized for a thin un-doped cap layer of 50 Å thickness. The study also discovered that longer etching time was needed for thicker cap layers or smaller gate length openings after resist development - this is necessary to avoid residue in the recess area, as illustrated in Figure 3.19.

![InGaAs cap residue after gate recess!](image)

Figure 3.19 InGaAs cap residue after gate recess. (Picture just for illustration)
For the purpose for this study, a new VMBE#1998 epilayer sample was used. The fabrication process exactly followed the process steps in previous runs, as depicted in Figure 3.10, but using only AZ 0.5 µm negative resist. For the gate recess study, the sample was cleaved to 4 pieces of identical size, etched with a different recess etch time for each piece, then gate metalized through standard thermal evaporation. The results are shown in Figure 3.20.

Figure 3.20 Off-state Schottky gate leakage current of pHEMTs with new AZ 0.5 µm negative resist for various gate recess etch times.

From Figure 3.20, it can be deduced that at $V_{GS} = -5$ V, the standard 5 minutes gate recess time gives a reverse gate current leakage of about 1.5 mA/mm, which is consistent with the value in Figure 3.17 for the new AZ 0.5 µm negative resist. The samples produced with longer gate recess extra times show very minimal
improvement, as their current leakage values are still high - around 0.34 mA/mm to 0.82 mA/mm. In addition, the $V_{BR}$ values shown in Figure 3.20 still low - about -4 V to -5 V for all runs. Meanwhile, the forward biased region from $V_{GS} = 0$ to 1 V gives a similar Ideality Factor ($\eta$) and Barrier Height ($\Phi_B$) for all runs - 1.58 and 0.36 eV respectively - this is still a consistently low barrier height as discussed previously.

It can be seen that longer gate recess etch times show slightly improved gate current leakage and increased $V_{BR}$, and consequently the threshold voltage is increased i.e. shifted towards a positive direction as shown in Figure 3.21 – this is confirmed by other researchers [81, 82]. This type of shift is due to the deeper gate recess to the $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ Schottky barrier layer, which is detrimental to the pHEMT device characteristics.

![Figure 3.21 Threshold voltage ($V_{th}$) at $V_{DS} = 1$ V of pHEMTs with New AZ 0.5 $\mu$m negative resist under various gate recess etch time.](image)

Figure 3.21 Threshold voltage ($V_{th}$) at $V_{DS} = 1$ V of pHEMTs with New AZ 0.5 $\mu$m negative resist under various gate recess etch time.
3.4 CONCLUSION

In this chapter, improvements are made to the gate mask step for the optically defined 1 μm gate length process. Although the current AZ 1 μm negative resist opening is measured at about 1 μm after C-E-D (coat-expose-develop) steps, metallization by thermal evaporation increases the dimension of the self-aligned gate length - this is caused by the undercut shape of the negative resist.

To solve this issue, a new resist mix was prepared in-house based on the spin curve for the AZ®nLOF™ 2070 negative resist and availability of AZ®nLOF™ 2 μm grade resist. By a careful calculation and dilution process, a newly mix AZ negative with 0.5 μm negative was successfully developed.

However, after exposure experiments for the newly mix resist, the smallest feature opening with high yield is after C-E-D is 0.8 μm, in spite of an ideally targeted goal of 0.5 μm. This issue may be due cleanroom conditions such as humidity and lack of special tools for resist mix and dilution. However, a gate length close to 1 μm was achieved after metallization, which is sufficient for the 1 μm gate length pHEMT process.

The performance of the newly mixed AZ 0.5 μm negative resist is compared with the standard AZ 1 μm negative resist. This is done by fabricating pHEMTs which incorporating the two resists at the gate step, the DC and RF performance is assessed. An optimised pHEMT epitaxial layer structure, VMBE#1998 is chosen, which not only tests the new resist mix presentation, but also the epilayer structure performance.

The DC and RF figures of merit, discussed thoroughly in this chapter, demonstrate a significant improvement by using this newly mixed AZ 0.5 μm resist, compared to the standard AZ 1 μm resist; of particular note is the approximately 30 % increase
in this paper. These improvements not only save the cost of purchasing high resolution resist, but are also excellent for low-cost research purposes. However, to reduce further the gate length to sub-micron dimensions, this newly-developed resist mix has limitations – this will be discussed in detail in Chapters 4 and 5.

For the VMBE#1998 device, the high mobility and good carrier confinement make it suitable for low cost optically-defined 1 μm gate length applications, such as high speed and logic devices. However, the device is not suitable for low-noise and high-power applications, as a consequence of its high Schottky gate leakage current and low breakdown voltage. As the gate recess experiments do not show promising improvements to the gate leakage current and breakdown voltage, a different type of material needs to be characterized. Hence, the next chapter will focus on improving the epilayer structures to achieve low noise and high breakdown voltage results. Part of these improvements involve a thinner and un-doped cap layer, as supported by other researchers [74, 83].
CHAPTER 4

FABRICATION AND CHARACTERIZATION OF TENSILE BARRIER AND COMPRRESSIVE CHANNEL 1 µm GATE LENGTH InGaAs-InAlAs pHEMT

4.1 INTRODUCTION

The lowest possible noise figure for any transistor technology in the 2-1000 GHz frequency range is delivered by the InP-based High Electron Mobility Transistor (HEMT) [84]; this has been shown to have the best performance of all three-terminal devices [85]. However, InP-based HEMT performance can be further improved through the use of strained high mobility InGaAs; using this material, the best noise figures and high-frequency operation can be produced.

An excellent material for the production of high-frequency, low-noise devices is the conventional lattice-matched In$_{0.53}$Ga$_{0.47}$As-In$_{0.52}$Al$_{0.48}$As pseudomorphic HEMT (pHEMT), using an InP substrate, with an In$_{0.7}$Ga$_{0.3}$As compressively-strained channel. This is due to the high mobility and high saturation velocity of the device, stemming from the high level of Indium in the InGaAs channel [86].

A conventional low-noise pHEMT using the above material system exhibits a breakdown voltage of about 2 - 4 V, and a high gate leakage of around 1 mA/mm at -5V [87, 88] - these are significant limitations for the device. The lattice-matched In$_{0.52}$Al$_{0.48}$As supply layer used as the barrier, and the low band-gap material employed in the channel are the principal causes of this limitation. The small Schottky barrier in the supply layer and high impact ionization in the channel are the causes of the low breakdown voltage and high gate leakage, respectively. The
problems described have restricted the usefulness of these pHEMT materials in low-noise designs.

A number of researchers have suggested options to address the problems previously described, although the proposed solutions significantly reduce the unity current gain cut-off frequency $f_T$, and therefore increase the noise. The methods proposed include: using platinum gate metal [89] as the Schottky barrier, a far larger InGaP and AlAs spacer layer [14, 16, 90], a composite channel design [17], and double recessed structures [18, 91].

Over the past few years, a novel high-breakdown, low-leakage InGaAs-InAlAs pHEMT has been developed by the author and colleagues at the University of Manchester [92]. A device with a 1 µm gate length has been optimised, but it is based on lattice-matched In$_{0.52}$Al$_{0.48}$As barriers. However the ability to change the Indium and Aluminium compositions of the $\text{In}_x \text{Ga}_{(1-x)} \text{As-In}_{(x)} \text{Al}_{(1-x)} \text{As}$ system alters its material characteristics. InAlAs acts as the barrier layer in pHEMT structures; it is possible to increase the band gap of In$_{0.3}$Al$_{0.7}$As up to 2 eV, and that of InGaAs to ~0.6 eV, beginning from the lattice-matched composition ($x \approx 0.52$) - this results in high mobility and high saturation velocity. The highly-strained materials have key thicknesses that are compatible with pHEMT aspect ratios, ranging from gates of deep submicron size (25 nm), up to more than 1 µm.

Recently, a significant increase in the breakdown voltage and decrease in gate leakage has been produced. This was achieved only through bandgap engineering, which generated a narrow band gap channel and a barrier with a wide band gap, in an advanced highly-strained InGaAs-InAlAs pHEMT. Two double delta-doped structures are included in the epitaxial layers, giving improved confinement of the quantum well charge, and a high 2DEG carrier density.

The successful fabrication and characterization of the above structure exhibits breakdown voltage and gate leakage improvements of over **89 % and 99 %**
respectively, compared to a conventional InGaAs-InAlAs pHEMT device. These significant improvements are likely to make these devices useful in low-noise and high-power applications. The cut-off frequency of a device with a 1 µm gate length and 800 µm gate-width was measured, and found to be practically identical to the value for conventional structures, which shows that the higher tensile strain caused no adverse effects on the device cut-off frequency.

4.2 DEVICE MATERIAL GROWTH AND FABRICATION

4.2.1 Epitaxial Growth

Two alternative samples with an InGaAs/InAlAs/InP epitaxial layer design were produced: a conventional pHEMT, XMBE171 - the baseline for the study - and an advanced pHEMT, XMBE210. The devices were grown in-house using Molecular Beam Epitaxy (MBE) on a RIBER V100 System.

The XMBE171 sample is a single Si-δ doped epitaxial layer device. A lattice matched (to InP) un-doped 4500 Å InAlAs buffer was grown, then a highly-compressive un-doped 140 Å pseudomorphic In$_{0.7}$Ga$_{0.3}$As channel was added, followed by a lattice-matched un-doped 50 Å InAlAs spacer, and a Si-δ doping layer. The un-doped 300 Å InAlAs barrier was also lattice-matched to InP, which is used as a Schottky contact layer. In addition, an un-doped lattice-matched 50 Å InGaAs cap layer was grown, allowing for the later addition of low resistivity Ohmic contacts.

The XMBE210 device employs an advanced pHEMT epilayer design with double Si-δ doping - this is the key difference to the conventional pHEMT XMBE171. The device has two barrier and supply layers formed from InAlAs, resulting from the double Si-δ doping. It consists of a lattice-matched, un-doped 100Å-thick InAlAs
barrier, and 100Å-thick supply layers, which was grown after a lattice matched 4500 Å un-doped buffer layer - the first Si-δ delta-doped layer was positioned between these layers. The channel is designed to be similar to that of XMBE171; it is produced from 160 Å thick, highly-compressive, un-doped pseudomorphic In$_{0.7}$Ga$_{0.3}$As. An un-doped, highly tensile, 130 Å thick, In$_{0.5}$Al$_{0.7}$As spacer was then grown, after which the second Si-δ delta-doped layer was formed. An un-doped, highly-tensile In$_{0.3}$Al$_{0.7}$As barrier was then grown, to a thickness of 190 Å - this forms a Schottky contact layer. Low-resistivity Ohmic contacts were then formed as the final cap layer, from lattice-matched un-doped 50 Å InGaAs.

Cross-sections of the two epitaxial layer structures are shown in Figures 4.1 and 4.2, and Table 4.1 shows calculations [93] of the approximate band energies ($E_g$) and band gap differences ($\Delta E_g$), of XMBE171 and XMBE210.

![Cross-section of the two epitaxial layer structures](image)

**Figure 4.1** XMBE171 (Conventional pHEMT) epitaxial layer grown in-house on RIBER V100 MBE (Thickness not to scale).
Figure 4.2 XMBE210 (Advanced pHEMT) epitaxial layer grown in-house on RIBER V100 MBE (Thickness not to scale).

Table 4-1 XMBE171 and 210 band energies ($E_g$) and band gap difference ($\Delta E_g$).

<table>
<thead>
<tr>
<th>Device</th>
<th>Wide Band Gap 1</th>
<th>Narrow Band Gap 2</th>
<th>$E_{g1}$ (eV)</th>
<th>$E_{g2}$ (eV)</th>
<th>$\Delta E_g$ (eV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>XMBE#171</td>
<td>In$<em>{0.52}$Al$</em>{0.48}$As</td>
<td>In$<em>{0.7}$Ga$</em>{0.3}$As</td>
<td>1.4</td>
<td>0.579</td>
<td>0.821</td>
</tr>
<tr>
<td>XMBE#210</td>
<td>In$<em>{0.3}$Al$</em>{0.7}$As</td>
<td>In$<em>{0.7}$Ga$</em>{0.3}$As</td>
<td>2.2</td>
<td>0.579</td>
<td>1.621</td>
</tr>
</tbody>
</table>

4.2.1.1 Hall Effects Measurements and Band Diagrams

Two important Hall measurement parameters for assessing the quality of the conventional pHEMT XMBE171 and advanced pHEMT XMBE210 epilayers are the 2DEG electron mobility and its sheet carrier concentration. Measurements at
room temperature of XMBE171 showed an electron mobility value of 10653 cm$^2$/V.s, while the sheet carrier concentration was 3.16 x10$^{12}$ cm$^{-2}$. The advanced pHEMT exhibited an electron mobility of 11008 cm$^2$/V.s and a sheet carrier concentration of 2.70 x10$^{12}$ cm$^{-2}$ at room temperature. The reduced spacer thickness in the conventional pHEMT device - as shown in Figure 4.1 - is the main cause of the increased 2DEG sheet carrier concentration observed, relative to the advanced pHEMT.

The baseline for this study is the conventional pHEMT epilayer structure of XMBE171. Compared with this, the XMBE210 advanced pHEMT epilayer structure has a wider band gap, consisting of Al-rich In$_{0.3}$Al$_{0.7}$As; it produces higher Schottky barriers, as seen by the carriers within the 2DEG channel. Consequently, the leakage current of the Schottky gate will be reduced, through limitation of the number of carriers produced from tunnelling through the Schottky barrier in the off-state ($V_{GS} \approx V_T$) mode [13], or from thermionic field emission. The higher Schottky barrier, in conjunction with the Al-rich In$_{0.3}$Al$_{0.7}$As spacer, produces a lower impact ionization in the channel in the on-state ($V_{GS} > V_T$) mode, thereby reducing the on-state Schottky gate leakage.

The highly-strained barrier which increases the Schottky barrier height reduces the hot electrons injection from the gate, where these electrons enter the channel gate-drain zone with high energy, due to the high electric field between gate and drain. These electrons will then relax this energy, and will be high enough to initiate the impact ionization process in the channel, and to generate electron-hole pairs [50, 80, 94]. The highly-strained spacer increases the valence band discontinuity at the spacer-channel interface, and hence reduces the number of holes generated from impact ionization in the channel due to tunnelling to the negatively biased gate [13, 14, 95]. The thicker spacer also degrades the transport properties, due to lower electron transfer efficiency from the donor layer to 2DEG channel, hence a low $I_{DS}$ which then gives low electron-hole pair generation in the channel during impact.
The addition of double Si-δ doping results in improved 2DEG confinement in the quantum well; combining this with the wider band gap of Al-rich In$_{0.3}$Al$_{0.7}$As results in a higher Schottky breakdown voltage [96]. A band diagram for the structures of the two devices discussed is shown in Figures 4.3 and 4.4.

**Figure 4.3** XMBE171 (Conventional pHEMT) conduction band diagram and electron distribution.
4.2.2 Device Fabrication

To avoid problems of inconsistency in processing, all of the devices mentioned up to this point were produced simultaneously, using a standard process with the same mask. The fabrication was done using conventional optical lithography and metal lift-off. Consequently the active layer or MESA isolation was initially created by wet-etching the epilayers as far into the InAlAs buffer layer. The etching was done with Orthophosphoric acid (H₃PO₄:H₂O:H₂O₂), a non-selective rapid etchant, with a ratio of 3:1:50. The MESA sidewall was wet-etched using a succinic acid solution at the same step, but after the Ortho etch, to achieve better gate metal isolation from the In₀.₇₂Ga₀.₂₈As channel when gate metallization is performed later in the fabrication process [97]. In the last step, Ohmic connections for Source and Drain
were deposited using thermal evaporation of 50 nm of AuGe, followed by 100 nm of Au; these were then alloyed at 280 °C in a furnace. The resultant resistances (R_C) of the contacts were < 0.16 Ω.mm.

A highly-selective solution of succinic acid was used to pattern the gate recess, to remove the InGaAs cap layer; this defines the gate footprint. Following this, 50 nm of Ti and then 450 nm of Au metals were thermally evaporated, to produce a 1 µm-long flat gate contact. Finally, a thermal evaporation technique was used to produce the bond pads required for microwave measurement probing.

4.3 RESULTS AND DISCUSSIONS

4.3.1 Direct Current (DC) Characteristics

Figures 4.5 and 4.6 show typical voltage-current curves for the baseline XMBE171 and the advanced XMBE210 pHEMT devices - normalised I_DS current values are shown for ease of comparison. The conventional pHEMT device had a gate width of 200 µm, and the advanced device gate width was 800 µm. The very large leakage currents in an 800 µm gate-width device baseline pHEMT meant that the device could not be sustained.
Figure 4.5 XMBE171 (Conventional pHEMT) DC characteristic with 1 µm length multi-gate of 2x100 µm width. $I_{DS}$ vs. $V_{DS}$ when $V_{GS}$ is swept from 0 V to -1.2 V.

Figure 4.6 XMBE210 (Advanced pHEMT) DC characteristic with 1 µm length multi-gate of 4x200 µm width. $I_{DS}$ vs. $V_{DS}$ when $V_{GS}$ is swept from 0 V to -1.6 V.
Figure 4.6 shows the output characteristics of an XMBE210 device with a maximum drain current density of 230 mA/mm at $V_{GS} = 0$ V and $V_{DS} = 1$ V, while the XMBE171 device shows 370 mA/mm. The maximum extrinsic transconductance at $V_{DS} = 1$ V for XMBE210 is 300 mS/mm – this is low compared to the 470 mS/mm for XMBE171. This is as expected, since the 2DEG sheet carrier concentration in the channel is lower, due to the fact that the spacer is 62% thicker (see Figures 4.3 and 4.4, and the Hall Effect measurement data).

Figure 4.7 shows the off-state Schottky gate leakage current for both devices; the improved performance of the advanced XMBE210 pHEMT compared with XMBE171 is clear.

![Figure 4.7 XMBE171 (Conventional pHEMT) and XMBE210 (Advanced pHEMT) off-state Schottky gate leakage current at $V_{GS} = -8$ V.](image)
The data in Figure 4.7 shows that the Schottky gate current leakage of XMBE210 in the off-state is over four orders of magnitude lower, compared to -1000 µA/mm at $V_{GS} = -1.6$ V for XMBE171 - it is anticipated that this will result in excellent noise performance. The design of the double delta structure and the wide-band materials used in the supply result in exceptionally low gate leakage current. The leakage for XMBE210 is -9 µA/mm at $V_{GS} = -8$ V, a remarkable figure placing the actual breakdown (defined as 1mA/mm) probably well into the 10s of volts.

The features of the Schottky diode in XMBE210 exhibit a barrier height of 0.9 eV, and an Ideality factor of 1.15; this demonstrates the presence of excellent Schottky contacts. The baseline XMBE171 has an Ideality factor and barrier height of 1.60 and 0.5 eV, respectively.

The near-unity Ideality factor implies that a good Schottky diode interface exists, which shows that thermionic emission is the sole transport mechanism, because any deviation from unity shows that current flow is due to other transport mechanisms such as Thermionic-Field Emission (TFE) current [98] - this is the case for the baseline transistor. As previously mentioned, the main cause for the Off-state reverse Schottky gate leakage current is tunnelling through the barrier. Hence, the Schottky barrier height ($\Phi_B$) plays an important role in reducing this tunnelling or TFE [51, 99]. From the simulated band diagrams in Figure 4.3 and Figure 4.4, and also from Figure 4.8 (which show Conduction band of XMBE210 and XMBE171 only), the Schottky barrier heights for XMBE210 and XMBE171 are 0.9 eV and 0.5 eV respectively. This is about a 44 % increase in barrier height compared to the XMBE171 Conventional pHEMT. This enhanced Schottky barrier height is due to the tensile In$_{0.3}$Al$_{0.7}$As barrier and spacer of the XMBE210, compared to the lattice matched In$_{0.52}$Al$_{0.48}$As barrier in XMBE171. In addition, the high Al content in the XMBE210 wide band gap material enhanced the barrier height [100]. There is therefore an increase in the tunnelling barrier height between the Schottky gate and
narrow band gap strained In_{0.7}Ga_{0.3}As channel, which suppresses the Off-state gate leakage appreciably.

Figure 4.8 Conduction band ($E_c$) diagram of XMBE210 and XMBE171.

To explain further, and by referring to Figure 4.8, the mechanism of reverse Schottky gate leakage current is suppressed due to the gate electrons in XMBE210 experiencing a greater barrier height compared to the gate electrons in XMBE171. When the barrier is high, there is minimal gate leakage current or Thermionic Field Emission (TFE) or tunnelling which occurs, only Thermionic Emission (TE) of electrons from source to drain [99]. Equation 2.28 in Chapter 2 also shows that the reverse Schottky gate leakage current depends on the $\Phi_B$, while Equation 2.27 shows that when the Ideality factor is near unity, only the TE mechanism occurs,
which is supported by the Ideality factor value for XMBE210, which is 1.15 compared to XMBE171 which is 1.60. Furthermore, due to the double-delta-doped structure, and the wide band gap $\text{In}_{0.3}\text{Al}_{0.7}\text{As}$ which increases the conduction band discontinuity with the narrow band gap $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$, the quantum well is deeper, and electrons are more confined in the channel, which helps to effectively increase the barrier for TFE to occur. This reduces the gate leakage [101] in XMBE210, compared to the single-delta-doped and low band gap $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ in XMBE171, as mentioned in Table 4.1, where the energy band gap discontinuity or $\Delta E_g$ of XMBE210 is 1.621 eV ($\Delta E_c$ is approximately 70% of $\Delta E_g$ or 1.13 eV) while $\Delta E_g$ for XMBE171 is only 0.821 eV ($\Delta E_c$ is approximately 70% of $\Delta E_g$ or 0.57 eV).

Another factor that contributes to the reverse Schottky gate leakage current is the carrier concentration in the channel [102], or the Donor concentration ($N_D$) in the supply layer [43], which is also shown in Equation 2.26 in Chapter 2, where $E_{00}$ i.e. the tunnelling parameter is directly proportional to $N_D$. The effect of higher carrier concentration is that the depletion region or the effective tunnelling barrier becomes thin, which will lead to electrons tunnelling through the barrier under the TFE mechanism, as shown in Figure 2.13 in Chapter 2. This is the case for XMBE171, where the carrier concentration is $3.16 \times 10^{12}$ cm$^{-3}$ which is higher than $2.70 \times 10^{12}$ cm$^{-3}$ in XMBE210.

Under similar bias conditions, the reverse Schottky gate leakage current of XMBE210 is 4 orders of magnitude lower than XMBE171; this improvement is mainly due to the increase in Schottky barrier height, as well as the lower carrier concentration in the channel. These improvements are mainly in the material epilayer design, with a tensile barrier, spacer thickness and the double delta doping compared to the XMBE171 epilayer, while Table 4.2 show a comparison of the gate leakage current of this Advanced pHEMT (XMBE210), with other research mentioned earlier in the Introduction section of this chapter.
Table 4-2 Comparison between XMBE210 gate leakage current with literature.

<table>
<thead>
<tr>
<th>Improvement</th>
<th>Reference</th>
<th>Gate Leakage (µA/mm) @ $V_{GS} = -1.5$ V</th>
<th>Cut-off Frequency ($f_T$) Reduction After Improvement</th>
</tr>
</thead>
<tbody>
<tr>
<td>Platinum (Pt) gate metal</td>
<td>[88]</td>
<td>-1</td>
<td>Parameter not available</td>
</tr>
<tr>
<td>AlAs spacer</td>
<td>[16]</td>
<td>-20</td>
<td>Parameter not available</td>
</tr>
<tr>
<td>InGaP spacer</td>
<td>[18];[89]</td>
<td>-55</td>
<td>23 %</td>
</tr>
<tr>
<td>Composite Channel</td>
<td>[19]</td>
<td>-1</td>
<td>Parameter not available</td>
</tr>
<tr>
<td>Double gate recess structure</td>
<td>[20];[90]</td>
<td>-20</td>
<td>54 %</td>
</tr>
<tr>
<td>Tensile InAlAs Barrier (XMBE210)</td>
<td>This work</td>
<td>-0.2</td>
<td>0 %</td>
</tr>
</tbody>
</table>

The measured gate-drain or gate-source breakdown voltage is defined as the reverse gate voltage, as both the XMBE171 and XMBE210 devices have symmetrical geometry when the gate current rises to 1 mA/mm. Therefore, Figure 4.7 shows that XMBE210 exhibits a high breakdown voltage; extrapolating this suggests that breakdown occurs at $V_{GS} = -15$ V at $I_{GS} = 1$ mA/mm, compared to only $\sim -1.6$ V for the conventional device.

The high breakdown voltage in XMBE210 is a result of the large band gap of the supply layer, which leads to a high Schottky barrier, as previously discussed. The high Schottky barrier reduces the TFE effect, and consequently increases the breakdown voltage; this is because the off-state leakage current is principally caused by TFE in the Schottky barrier. This feature is ideal for producing low-noise amplifiers which require minimal protection circuits.
An additional key improvement of the advanced pHEMT device compared with the conventional design is shown in Figure 4.9, which gives the on-state Schottky gate leakage current. The gate leakage described differs from the off-state Schottky gate leakage depicted in Figure 4.7, because of the existence of an applied drain-source voltage, $V_{DS}$. Figure 4.9 shows that a very small reverse Schottky gate leakage current caused by electron tunnelling of -0.2 µA/mm at $V_{GS} = -3$ V is present in XMBE210 - this is over three orders of magnitude smaller than the -6 mA/mm to -8 mA/mm in XMBE171.

![Figure 4.9 XMBE171 (Conventional pHEMT) and XMBE210 (Advanced pHEMT) on-state Schottky gate leakage current at $V_{GS} = -3$ V, in mA-range.](image)

For small values of $V_{DS}$, the gate leakage current is generally caused principally by electrons tunnelling through the Schottky barrier. The magnified section of Figure 4.10 shows a gate leakage current of a few µA; this is due to the fact that when $V_{DS}$ is increased beyond 1 V, impact ionization begins in the channel [50]. The collection of holes generated by impact ionization results in the leakage current...
taking the form of bell-shaped curves, therefore the advanced XMBE210 pHEMT device in Figure 4.10 demonstrates a maximum on-state Schottky gate leakage, due to impact ionization at $V_{DS} = 2\, V$, of only about $-16\, \mu A/mm$. This is over two orders of magnitude lower than the -3.3 mA/mm in XMBE171, and much lower than that reported in [103]. A further physical mechanism of the on-state Schottky gate leakage current and the peak and position of the bell shape can be explained as follows. Referring to Figure 4.10, at a large negative $V_{GS}$ less than $V_{th}$ (between $V_{GS} = -3\, V$ to $\approx -1.6\, V$), the device is OFF, which means $I_{DS} = 0$ and no holes are generated as no impact ionization occurs in the channel - gate leakage currents are mainly due to the electrons tunnelling through the Schottky barrier [50, 52, 103]. When $V_{GS}$ is greater than $V_{th}$ ($V_{th} = -1.6\, V$ for XMBE210 as in Figure 4.10), the device is turned ON, and impact ionization occurs starting from $V_{DS} = 1\, V$, which then deforms the gate leakage current plot into a bell shape at a particular constant $V_{DS}$ value. As mentioned previously, the bell shape is due to the collection of holes which are created from the impact ionization process, due to the negatively-biased gate (refer Figure 2.16 in Chapter 2) which increases the gate current leakage. The peak of the bell shape increases, since the impact ionization rate increases as $V_{DS}$ increases; this phenomenon is due to the electric field becoming stronger and more significant at the gate-drain area [52, 103], where the maximum impact ionization occurs at $V_{DS} = 2\, V$ i.e. the max $V_{DS}$ applied for the device run. The position of the impact ionization, according to Figure 4.10 of XMBE210, occurs in the vicinity of $V_{GS} = -1.2\, V$, because this is where the critical electric field ($E_c$) occurs; the value of $E_c$ could not be determined in this device run, except through modelling, which is beyond the scope of this research. Based on other research, the position of the starting point of the impact ionization depends on the thickness of the gate-to-channel distance and the carrier sheet density of the device, which then influences the $E_c$ [52]. After this position of $V_{GS}$, the gate leakage current declines from the peak value as the impact ionization becomes lower, since the electric field at the gate-drain region reduces as $V_{GS}$ increases toward 0 V [52, 103].
XMBE210 shows extremely low on-state Schottky leakage current, solely because of the band gap engineering employed in the pHEMT epitaxial layer design. Holes are prevented from being collected by the gate due to the large Aluminium (Al) content, which increases the $\Delta E_g$ discontinuity; this reduces the gate current leakage in the on-state. The device is therefore ideal for both high power and low noise applications.

4.3.2 Radio Frequency (RF) Characteristics

A Vector Network Analyzer (VNA) was used to quantify the small-signal S-parameters across a span of 40 MHz to 40 GHz. An on-wafer RF measurement tool,
Cascade Microtech WINCAL XE, was used to calibrate the measurements over the span, using the 2 Port LLRM method on the substrate, as follows:

i) Raw open-circuit measurements are made multiple times to ensure repeatability.

ii) Calibration of standard thru, separate, short and load structures are performed.

iii) Calibration is calculated and transmitted to VNA.

iv) Validation is conducted using calibrated VNA.

Results below the red upper limit line are designated as ACCEPTABLE. If the validation results are UNACCEPTABLE, no RF measurement will be performed.

The cut-off frequency (\(f_T\)) was extracted for a bias at \(V_{DS} = 1\) V and 60% \(g_{m\text{max}}\), for devices with a 1 \(\mu\)m gate length (normalized gate width). Figure 4.11 can be used to derive the \(f_T\) - the crossing point at 0 dB and shows similar result for both devices, with the slopes of the lines at -20 dB / decade. The virtually identical \(f_T\) of the advanced device compared with the result for the conventional structures shows that the high-tensile strained supply layer in the advanced pHEMT epitaxial design does not degrade the device performance.
4.4 CONCLUSION

The purpose of this study was to improve the performance of the conventional 1µm-gate-length InGaAs/InAlAs/InP pHEMT. The aim was to reduce the high gate leakage current, and to increase the low breakdown voltage, as these limit the devices’ usefulness in low-noise applications. It has been possible to address these issues through the design of a new epitaxial layer structure, involving a heavily-compressively-strained (In-rich) channel and a highly tensile strained (Al-rich) Schottky contact barrier.

A significant improvement in the breakdown voltage was observed in the new advanced pHEMT design, combined with much lower off-state and on-state
Schottky gate current leakages. In addition, a thicker spacer and double delta-doped structure was developed.

The cut-off frequency ($f_T$) for both 1 µm-gate-length conventional and advanced pHEMT devices was measured to be almost identical; this shows that the new high-tensile strain structure causes no degradation to performance. An improvement in noise figure over the conventional pHEMT was also achieved[19]. The combination of these improvements makes the advanced pHEMT device useful in low-noise designs such as low noise amplifiers requiring minimal protection circuitry. Work is continuing to reduce the gate length to sub-micron levels, as will be discussed in the following chapters.
CHAPTER 5

NEW OPTICALLY-DEFINED SUBMICRON GATE LENGTH

pHEMT

5.1 INTRODUCTION

To achieve high speed, low noise, and high power-added efficiency at high frequencies, pHEMTs require a very small gate length. The cut-off frequency of operation, $f_T$, which is the figure of merit used to evaluate pHEMTs performance, is given by Equation 5-1.

$$f_T = \frac{\nu_{sat}}{2\pi L_g}$$  \hspace{1cm} \text{Equation 5-1}

Where $\nu_{sat}$ is the electron saturation velocity and $L_g$ is the gate length. Fabricating a very small gate is a challenge that requires well-developed lithography and pattern transfer techniques.

In most research projects, masks for the lithography of pHEMTs are fabricated using a combination of electron beam lithography (EBL) [104] and photolithography. Although direct-write EBL is a low throughput exposure process, it facilitates an accurate definition and alignment of sub-micron geometries, while providing flexibility and fast turnaround for design iterations. EBL is widely and routinely used to produce gate dimensions of less than 0.25 μm [105-107]. To improve the wafer or sample exposure throughput, optical lithography is used for the coarse features (>1 μm or 1000 nm), and the direct EBL is used only for the very small gates. This hybrid lithography technique has the combined advantages of the
high throughput of optical lithography, and the high resolution and accuracy of EBL. The hybrid lithography scheme is also used for pHEMT-based MMICs requiring sub-micron gates.

As an alternative to the EBL, there exists a simple technique called thermal reflow patterning, which had been use in some studies [108-111]. This technique involves transforming an initial photoresist pattern by baking it above its glass transition temperature (\(T_g\)). Since the photoresist pattern reflows at high temperatures (150 °C to 200 °C), the technique is sometimes known as hard reflow; however it cannot be used shrink dimensions further, even when reflowing at higher temperatures.

In Pseudomorphic HEMTs (pHEMTs), to achieve high operating speeds of up to 100 GHz, and low noise figures, the device gate length must be short – i.e. below 0.25 μm [112]. Conversely, as the gate length reduces, its resistance increases, but this can be compensated for by the introduction of a mushroom-shaped or T-shaped gate structure. Moreover, fabricating a very short gate needs a well-developed lithography and pattern transfer technique, commonly based on electron beam lithography (EBL) with multiple resist layers. However, there are also several reported studies which have used optical lithography with thermal reflow [108-111].

Techniques such as EBL have the disadvantage of low throughput, while thermal-reflow has its own limitations such as the high temperatures involved. In this chapter, a conventional I-line optical lithography technique combined with a soft-reflow technique invented at the University of Manchester [70] will be discussed. This method is simple, repeatable and very cost-effective for achieving nm-scale features.
5.2 SUBMICRON T-GATE PROCESS

5.2.1 Soft Reflow Technique

The soft reflow technique is also known as the bi-layer soft reflow process. It uses a low-cost optical lithography method with a starting gate opening of roughly 1 µm width. The sample is then subjected to a reflow process using a solvent which vaporises close to room temperature. The major advantage of this technique is that the deep submicron T-shaped gate structure can be realized using only optical lithography, giving high throughput compared to e-Beam lithography.

5.2.1.1 Principle of Soft Reflow

Soft reflow is performed in a conventional closed chamber, as shown in Figure 5.1 - the principle of this process is explained below:

![Figure 5.1 Conventional Manchester soft reflow chamber setup](image_url)

A) The reflow process is based on the concept of steaming the solvent in a closed chamber containing the solvent and a metal sample holder.
B) The chamber is half-filled with a special solvent that evaporates slowly near room temperature (< 50 °C) at atmospheric pressure (~ 1 bar). The solvent used depends on its evaporation rate and also the type of photoresist.

C) During reflow, the sample is placed on a metal holder hanging above the solvent.

5.2.1.2 Soft Reflow Patterning Flow on Hard Mask

Figure 5.2 shows the process flow to define the bottom gate using the soft reflow technique. A hard mask (usually Silicon Nitride) is formed on the substrate which is not soluble in the solvent, and the photoresist on top of this is the soft top layer that determines the final opening after reflow.

![Figure 5.2 Process flow of the soft reflow](image)

The first step is to pattern the photoresist with an opening of length (L) on the hard mask using optical lithography. Step two is to reflow the sample in the reflow chamber, where the vapour from the solvent, close to room temperature, will condense on the photoresist. In step three, the condensate is absorbed by the photoresist, and expands or reflows from length L to L’.

The amount of reflow
produced ($\Delta L$) is closely dependent on the reflow time. In the final step, the reflowed pattern is transferred from the soft layer to the hard mask.

The key advantage of this soft reflow process compared to hard reflow in the literature [109] is that the reflow temperature is $< 50 \, ^\circ C$, and is more controllable, while hard reflow is applied at $150 \, ^\circ C$ and above, and the hard baked resist become difficult to etch or develop. Furthermore, this reflow technique can be further applied to other organic or polymer-based materials, such as spin-on-glass as will discussed in the

5.2.2 Soft Reflow Optimization

Currently, the soft reflow technique developed at the University of Manchester [114] can only achieve features of 250 nm, and the maximum reflow time with a conventional closed chamber set up is 90 s. Beyond this reflow time, the initial 1 $\mu$m opening is fully closed, and hence it is not possible to define the bottom gate (see Figure 5.3).

![Figure 5.3 Gate opening versus reflow time [114].](image)

Figure 5.3 Gate opening versus reflow time [114].
In the optimization process discussed here, the technique used for the improved chamber is still valid, as illustrated in Figure 5.1, but major modifications are performed to the chamber setup. Notably, the reflow is no longer performed in a closed chamber, but with an aperture or shutter to control the vapour flux from the reflow solvent. Figure 5.4 illustrates the improved soft reflow chamber setup, compared to the conventional one shown in Figure 5.1.

As mentioned previously, the conventional reflow chamber setup only yields bottom gate definitions of 250 nm for a maximum time of 90 s; further reflow of more than 90 s will cause the feature size to fully close. However the advantage of the conventional chamber design is its simple setup with repeatable results; its main drawback is the condensation and the reflow solvent pressure increase over time, which also increases the reflow rate.

![Diagram of reflow chamber setup](image)

**Figure 5.4 Side and top views of improved version of reflow chamber setup.**

The improved soft reflow chamber setup is also easy to set up, and has a number of advantages compared to the previous design. Apart from being simple and easy to set up, the results are also repeatable. Due to constant reflow of solvent pressure, the
flux can be varied by removing the aperture or shutter for fine tuning, hence the reflow time is extendable well beyond 90 s. The top view in Figure 5.4 shows that the shutter can be opened to maintain a constant flux, hence reducing the solvent vapour pressure.

5.2.3 T-Gate Fabrication Process Through Soft-Reflow Technique

5.2.3.1 Fabrication using conventional chamber set up

A trial run was conducted to examine the performance of the conventional soft reflow process. The hard mask was formed by a 200 nm-thick silicon nitride (Si₃N₄) layer, which is deposited by PECVD at a temperature of 200 °C on a sample. The surface of the hard mask was then patterned using Shipley S1805 resist, and then reflowed for 90 s using the conventional chamber setup shown in Figure 5.1. The reflowed pattern was then transferred to the hard mask by performing plasma etching using Tetrafluoromethane (CF₄) gas at a low power (20 W) and low pressure (21 mTorr to 23 mTorr) in order to define the bottom gate or gate footprint. The remaining processes - formation of Ohmic to Top gate - are the same as for the conventional process flow to fabricate 1 μm flat gates.
Figure 5.5 T-gate device fabrication by conventional soft reflow chamber setup.

Picture A in Figure 5.5 shows the measurement of the bottom gate opening after coating, exposure and developing using S1805 Shipley resist - the initial gate opening is roughly 1µm. In picture B of Figure 5.5, the measurement is taken after CF$_4$ plasma etching and cleaning, where it is clear that the bottom gate is about 250 nm, and consistent with that developed earlier at the University of Manchester [114]. Further measurement was taken after the bond pad, for which the measurement is also about 250 nm on the groove pattern found in the middle of the gate, where the footprint is located underneath the top gate head. The cross sectional or side view of this fabricated T-shape gate is illustrated also in Figure 5.5 above.
5.2.3.2 Fabrication using improved chamber set up (stage under development)

In this study, only the bottom gate is defined in order to study its shrinkage properties. The hard mask layer thickness, resist type, reflow solvent and pattern transfer process are similar to those described in section 5.2.3.1. The only different is that the reflow process was performed in the new soft reflow chamber setup, as illustrated in Figure 5.4. The results were captured for different reflow times and number of shutter openings, to determine whether it is possible to achieve a bottom gate size of less than 250 nm.

Figure 5.6 Bottom gate opening after 150 s reflow (both one shutter and two shutter open).

Figure 5.7 Bottom gate opening after CF₄ etch and cleaning (One shutter open).
Figure 5.8 Bottom gate opening after CF$_4$ etch and cleaning (Two shutters open).

Figure 5.6 shows the image for both one and two shutters open for a reflow time of 150 s. It can be clearly seen from Figure 5.6 that the photoresist changed its profile, moving inwards and hence reducing the opening size to 0.19 µm or 190 nm. The rainbow pattern observed is due to the expansion of the resist in both the horizontal and vertical directions, as explained in Figure 5.2, due to absorption of the solvent vapour. After plasma etching using CF$_4$ gas at a low power and low pressure, and then cleaning (to remove residual resist), Figures 5.7 and 5.8 show that the submicron bottom gate footprint became more visible, as the reflowed pattern transferred to the Si$_3$N$_4$ hard mask layer. Figures 5.7 and 5.8 also show that the final bottom gate definition is the same whether one or two shutters are opened during the reflow process. The results of the experiment in this study is given in Table 5.1, which also summarizes the runs of the experiment, for comparison purposes; the 3 µm and 2 µm initial opening features size are also included.
Table 5-1 Summary of study of reflow time vs bottom gate opening for number of shutters open during reflow.

<table>
<thead>
<tr>
<th>Reflow time (s)</th>
<th>One shutter open</th>
<th>Two shutters open</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>3 μm</td>
<td>2 μm</td>
</tr>
<tr>
<td>0</td>
<td>3.00</td>
<td>2.00</td>
</tr>
<tr>
<td>30</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>60</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>90</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>120</td>
<td>2.00</td>
<td>1.10</td>
</tr>
<tr>
<td>150</td>
<td>1.90</td>
<td>1.10</td>
</tr>
<tr>
<td>180</td>
<td>1.90</td>
<td>0.90</td>
</tr>
</tbody>
</table>

The data in Table 5.1 shows that there is no significant difference whether one or two shutters are opened during the reflow process. This implies that the constant flux evaporation of the solvent vapour, as shown in Figure 5.4, does not significantly affect the reflow rate. Table 5.1 also demonstrates that, with the new and improved chamber setup, the bottom gate opening can be further reduced, and the reflow time is now extendable to 150 s before the 1 μm opening is fully closed at 180s. This is a marked improvement compared with the previous studies [114], and other work that has used EBL or hard reflow techniques. Further observation of the behaviour of the reflow is shown in Figure 5.9, whereby this graph is a plot of the runs in Table 5.1.

135
According to the graph in Figure 5.9, there is a clear resist expansion during the reflow process. As can be seen, the data for the one shutter opening only starts at 90 s reflow, while the two shutters opening run starts from 30 s reflow time. By comparing this data to the previous study with a conventional-closed chamber setup [114], the rate of reflow is obviously not as rapid, but there are still 3 distinct regions: the active, saturation and termination regions for all the 6 curves in the plot. In the active region, the slopes of the curves show that the reflow rate is faster compared to the saturation region, where little resist expansion is observed. As the active region curve is not very steep, the region is wider and hence pushes the saturation region towards starting at 90 s. The termination region in this run occurs at 180 s for 1µm opening, but not for the 2 µm and 3 µm initial gate openings which - by extrapolation - starts at about 240 s. In short, the improved open chamber setup with controllable solvent vapour flux evaporation greatly helps with defining much
smaller feature sizes than the 250 nm that was reported, mainly thanks to the extended reflow time.

5.2.4 Discussion

This soft reflow study had been initiated at the University of Manchester, but operating limitations due to the conventional chamber design at the time restricted shrinkage of the 1 µm initial bottom gate opening to 250 nm. The maximum reflow time is also relatively short – only 90 s before the gate opening is fully closed. Major parameters that affect this soft reflow are the ability of the resist to absorb the solvent vapour, reflow solvent evaporation rate, and - most importantly - the reflow time, as well as other etching parameters such as gas choice, power, pressure and time.

The Shipley resist S1805 so far represents the best candidate for use in the soft reflow process, due to its ability to absorb solvent vapour. It is capable of expanding both horizontally and vertically when subjected to soft reflow. Different types of resists had been tried for soft reflow, such as Shipley S1813 which is thicker but the initial opening could not be reduced to 1 µm. In addition, a positive AZ 3 µm resist could not be reflowed with the chosen reflow solvent.

The previous conventional closed-chamber design (as shown in Figure 5.1) could not control the chamber pressure due to the build-up of solvent vapour. This was the major obstacle in achieving less steep active region, which in turn limited the reflow time in the saturation region, required to shrink the opening further. Conversely, the new open chamber design has the ability to control the rate of evaporation flux simply by opening and closing the shutters (refer to Figure 5.4). This constant flux evaporation rate enables a wider margin for the saturation region, making it possible to prolong the reflow time. Figure 5.9 describes and explains the operating
principles and improvement on the previously-developed method [114]. Hence, the optimization of the soft reflow using the newly-designed open chamber has been proven to reduce the bottom gate opening from 1 µm to 0.19 µm (190 nm), compared to 250 nm in the conventional closed-chamber design. It is estimated that the shrinkage could go down to 100 nm by further optimization, as more shutters could be opened to manipulate the saturation region. Although this may be true, due to time constraints, this is left as for future development.

5.3 NEW-SUBMICRON DEVICE FABRICATION AND CHARACTERIZATION

This section is an extension of the studies using the novel soft-reflow technique with the improved chamber setup shown in Figure 5.4, and also of the work done in Chapter 4. The focus of this study is on the area of epitaxial design, fabrication, characterization and final device performance of new optical sub-µm gate length InP-based pseudomorphic High Electron Mobility Transistors (pHEMT) using InGaAs-InAlAs material systems. The modification of the epitaxial layer design by incorporating a low temperature (LT) In$_{0.52}$Al$_{0.48}$As buffer (grown at $<$ 200 °C) significantly improves upon the conventional low noise pHEMT [92], which suffers from high gate current leakage and low breakdown voltage.

In addition, a new submicron T-gate process technique using conventional I-line optical lithography is capable of shrinking the gate length from 1 µm to 0.5 µm by solvent reflow at low temperature ($<$ 50 °C) with a high throughput compared to e-Beam lithography. Note that, despite the fact the soft-reflow process using the new chamber setup is able to shrink the 1 µm initial opening to 0.19 µm, for the purpose of this study, work start at 0.5 µm for application to actual device fabrication.
5.3.1 Device Material Epitaxial Growth

As in chapter 4, there are two structures of epilayer that are studied and compared, which were grown from an InGaAs/InAlAs/InP family. These two epitaxial layer structures are full-grown using in-house Molecular Beam Epitaxy (MBE) on a RIBER V100 System, and carry the prefix XMBE. One of these epitaxial structures, known as XMBE171, is set as the baseline for this study, and is identical to the conventional pHEMT in chapter 4. The other epitaxial structure is identified as XMBE56, and will be known as the Improved pHEMT throughout the discussion. Detailed overviews of both lattice matched InGaAs/InAlAs/InP pHEMTs are shown in Figures 5.10 and 5.11, while Table 5.2 shows calculations [93] of the approximate band energies ($E_g$) and band gap differences ($\Delta E_g$) of XMBE171 and XMBE56.

![Figure 5.10 XMBE171 (Conventional pHEMT) epitaxial layer grown on in-house RIBER V100 MBE (thickness not to scale).](image)

<table>
<thead>
<tr>
<th>Cap</th>
<th>InGaAs 50 (\text{Å} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Barrier</td>
<td>InAlAs 300 (\text{Å} )</td>
</tr>
<tr>
<td>Spacer</td>
<td>InAlAs (\delta) 50 (\text{Å} )</td>
</tr>
<tr>
<td>Channel</td>
<td>In(<em>{0.7})Ga(</em>{0.3})As 140 (\text{Å} )</td>
</tr>
<tr>
<td>Buffer</td>
<td>InAlAs 4500 (\text{Å} )</td>
</tr>
<tr>
<td>Substrate</td>
<td>InP (Fe)</td>
</tr>
</tbody>
</table>

Lattice matched to InP:
- \(\text{In}_{0.52}\text{Ga}_{0.47}\)As
- \(\text{In}_{0.57}\text{Al}_{0.43}\)As
Figure 5.11 XMBE56 (Improved pHEMT incorporating LT-In_{0.52}Al_{0.48}As buffer) epitaxial layer grown on in-house RIBER V100 MBE (thickness not to scale).

Table 5-2 XMBE171 and 56 band energies ($E_g$) and band gap difference ($\Delta E_g$).

<table>
<thead>
<tr>
<th>Device</th>
<th>Wide Band Gap</th>
<th>Narrow Band Gap</th>
<th>$E_g1$ (eV)</th>
<th>$E_g2$ (eV)</th>
<th>$\Delta E_g$ (eV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>XMBE171</td>
<td>In_{0.52}Al_{0.48}As</td>
<td>In_{0.7}Ga_{0.3}As</td>
<td>1.4</td>
<td>0.579</td>
<td>0.821</td>
</tr>
<tr>
<td>XMBE56</td>
<td>In_{0.52}Al_{0.48}As</td>
<td>In_{0.7}Ga_{0.3}As</td>
<td>1.4</td>
<td>0.579</td>
<td>0.821</td>
</tr>
</tbody>
</table>

As can be seen in Table 5.2, the conduction band gap differences or discontinuities are similar for both devices, since both have a lattice-matched In_{0.52}Al_{0.48}As spacer layer to an In_{0.7}Ga_{0.3}As channel.
5.3.1.1 Hall Effects Measurements and Band Diagrams

The epilayer structures for both XMBE171 and XMBE56 were characterized through Hall Effect measurement, and the results for both are recorded in Table 5.3. Furthermore, the 2DEG performance - i.e. the carrier mobility and sheet carrier concentration - are compared both at room temperature (300 K) and at 77 K. Further data in Table 5.3 again demonstrates that the sheet carrier concentration of XMBE56 of the Improved pHEMT is lower than the XMBE171 conventional pHEMT. This same trend, as shown in Chapter 4, is due to the spacer layer thickness of the Improved device being half of that of the Conventional epilayer structure, which can clearly be seen by referring to Figure 5.10. On the other hand, the carrier mobility for the Improved pHEMT is higher than the Conventional pHEMT epilayer structure. Hence the thinner spacer enhances more electrons to be trapped in the 2DEG channel, giving higher carrier concentration, at the same time achieving a stronger coulomb scattering effect between the δ-doped donor at the barrier layer with the channel, which causes degradation in carrier mobility in the 2DEG channel [115].

Significantly, the excellent carrier transport properties shown for the Improved pHEMT at room temperature i.e. with channel carrier concentration = $2.47 \times 10^{12}$ cm$^{-2}$ and mobility = 13169 (cm$^2$/Vs), is important for realizing high speed device fabrication.

<table>
<thead>
<tr>
<th>Measurement</th>
<th>XMBE171 (Conventional)</th>
<th>XMBE56 (Improved)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sheet Carrier Concentration ($n_H$) at 300 K / 77 K (x$10^{12}$ cm$^{-2}$)</td>
<td>3.16 / 3.56</td>
<td>2.47 / 2.61</td>
</tr>
<tr>
<td>Hall Mobility ($\mu_H$) at 300 K / 77 K (cm$^2$/V.s)</td>
<td>10653 / 24649</td>
<td>13169 / 42906</td>
</tr>
</tbody>
</table>
To complete the comparisons, the benefits of using the Improved epitaxial layer can be seen in the WinGreen® band diagram simulation. The illustrations of the energy band diagram for both structures are shown in Figure 5.12 and Figure 5.13.

Figure 5.12 XMBE171 (Conventional pHEMT) conduction band diagram and electron distribution.
Figure 5.13 XMBE56 (Improved pHEMT) conduction band diagram and electron distribution.

5.3.2 Device Fabrication

The fabrication process flow and steps of the device using XMBE171 (conventional epitaxial structure) are similar to those described in section 4.2.2 of Chapter 4, where a standard 1 μm process flow is incorporated. Generally, the flow starts with MESA isolation followed by the selective succinic acid etching of the MESA’s side walls. Then thermal evaporation of 50 nm AuGe and 100 nm Au is performed to form Source and Drain connections on the In$_{0.53}$Ga$_{0.47}$As cap layer. To achieve excellent Ohmic contact, the device is then alloyed at 280 °C for 90 s in the N$_2$ environment furnace to allow adequate metal diffusion deep into the 2-DEG. The following steps are succinic acid gate recess etching and then definition of the Schottky gate contact on the In$_{0.52}$Al$_{0.48}$As barrier layer using a flat gate length...
process as shown in Figure 3.2 in Chapter 3. Finally, thermal evaporation of 50 nm of Ti and 450 nm Au bond pad metals is performed.

The Improved epitaxial structure in this study, XMBE56, is made for a submicron T-gate device. The process starts with the deposition of 200 nm PECVD Si$_3$N$_4$ as a hard mask on the cap layer, then a 1 μm gate opening as for XMBE171, optically defined by I-line lithography and patterned on the hard layer. Next, a soft reflow technique as describe in Section 5.2.3 is employed, but using the improved chamber setup (see Section 5.2.3.2), to reduce the 1 μm gate opening to roughly 0.4 μm. The soft reflowed photoresist is then etched with CF$_4$ plasma for pattern transfer, defining the submicron bottom gate footprint. Upon successful definition of the bottom gate footprint, the MESA and Ohmic steps are similar to the fabrication of XMBE171. The last step for this submicron fabrication is to metalize the top gate and bond pads; this is different from XMBE171, in this process the top gate and bond pads are fabricated together in one mask step. Here again the 1 μm gate plus the bond pads opening are produced through an optical I-line process. Prior to metallization, the gate recess is produced in a similar way to XMBE171. The completed submicron T-gate device is then ready for DC and RF characterization after thermal evaporation of 50 nm Ti then 450 nm Au. Figure 5.14 shows the XMBE56 device after soft reflow and the T-gate structure.
5.3.3 Results and Discussion

5.3.3.1 Direct Current (DC) Characteristics

The TLM measurement was taken at room temperature directly after the Ohmic step and alloying. The data for both devices are recorded in Table 5.4.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>XMBE171 (Conventional pHEMT)</th>
<th>XMBE56 (Improved pHEMT)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{sh}$ ($\Omega/\square$)</td>
<td>182</td>
<td>155</td>
</tr>
<tr>
<td>$R_{c}$ ($\Omega$.mm)</td>
<td>0.19</td>
<td>0.13</td>
</tr>
</tbody>
</table>

In observing the data in the above table, one could appreciate that the $R_{sh}$ of the Improved pHEMT is lower by 14.8% compared to the Conventional pHEMT, due
to the higher mobility of electrons, by referring to the room temperature Hall Effect measurement data in Table 5.3 i.e. 13169 cm²/V.s and 10653 cm²/V.s for Improved and Conventional pHEMTs, respectively. Both devices have a low $R_c$ i.e. < 0.2 Ω/mm, demonstrating good Ohmic contact and reflecting deep diffusion of AuGe/Au metals into the 2DEG channel.

Hereafter, the DC characteristics for the devices studied have been measured with a Cascade Ground-Signal-Ground (G-S-G) 3 pin probe station, shown in Figure 3.13 of Chapter 3. The HP-Agilent 4142B Modular DC parameter analyser and an Agilent Vector Network Analyser (VNA) connected to the probes were used to measure the devices via their bond pads for data extraction. Furthermore, these two types of pHEMT devices are measured at room temperature, with data averaged over two devices of each type, while the values are normalized to the device gate width for fair comparison. Moreover, data for both the Improved and Conventional pHEMTs are compared on only 2 gate fingers of 2 x 100 μm (200 μm) gate width with 5 μm Source-Drain separation.

The DC output characteristics or I-V curves at various $V_{GS}$ points from $V_{GS} = 0$ V to $V_{GS} = -1.2$ V, for both Conventional XMBE171 and Improved XMBE56 epilayer structures, are shown in Figure 5.15 and Figure 5.16. Both figures show well-behaved curves with sharply defined pinch-off characteristics at room temperature, demonstrating excellent device operation. Analysis from both the curves shows that the normalized $I_{DS}$ current of the XMBE56 is lower than the XMBE171 at the same $V_{GS}$ biasing, resulting from the lower carrier concentration in the 2DEG channel in the Improved epilayer structure (refer to Hall Effect measurement data in Table 5.3) and hence less electron contribution to current conduction, and thus decreased the $I_{DS}$ output current. Correspondingly, the maximum drain current density ($I_{DSS}$) at $V_{GS} = 0$ V and $V_{DS} = 1$ V is 350 mA/mm and 370 mA/mm for XMBE56 and XMBE171 respectively.
Figure 5.15 XMBE171 (Conventional pHEMT) DC output characteristic with 1 µm length multi-gate of 2x100 µm width. $I_{DS}$ vs. $V_{DS}$ when $V_{GS}$ swept from 0 V to -1.2 V.

Figure 5.16 XMBE56 (Improved pHEMT) DC output characteristic with 0.5 µm length multi-gate of 2x100 µm width. $I_{DS}$ vs. $V_{DS}$ when $V_{GS}$ swept from 0 V to -1.2 V.
More insight into XMBE56 I-V curve shows a significant Kink effect and high output conductance compared to the Conventional XMBE171; this is due to the effect of the shorter gate length in XMBE56, which also tends to allow more electrons to be injected into the buffer layer [73].

The threshold voltages ($V_{th}$) for both devices are shown in Figure 5.17. This is an important parameter for operation of a pHEMT, and is determined by the thickness of the higher bandgap barrier layer [80] i.e. In$_{0.52}$Al$_{0.48}$As, or more specifically the gate to channel distance when the In$_{0.53}$Ga$_{0.47}$As cap layer is removed after gate recessing. Given these points, the $V_{th}$ for the LT-In$_{0.52}$Al$_{0.48}$As buffer of Improved pHEMT XMBE56 and Conventional pHEMT XMBE171 are approximately -1.10 V and -1.24 V respectively. These are not significantly different, because the difference in gate-to-channel distance between the devices is only 50 Å difference, referring to the epitaxial structures shown in Figure 5.10 and Figure 5.11.

![Figure 5.17](image)

**Figure 5.17** XMBE171 (Conventional pHEMT) and XMBE56 (Improved pHEMT) Threshold voltage ($V_{th}$) at $V_{DS} = 1$ V with 2 x 100 µm gate width.
In addition, Figure 5.18 shows the change of extrinsic transconductance \(g_m\) as a function of \(V_{GS}\) for both pHEMT devices, under biasing of \(V_{DS} = 1\) V. The peak from each plot is the maximum \(g_m\) value where XMBE56 peak is at \(V_{GS} = -0.46\) V with \(g_{m_{\text{max}}} = 403\) mS/mm and XMBE171 peak is at \(V_{GS} = -0.58\) V with \(g_{m_{\text{max}}} = 450\) mS/mm.

Moreover, there are two essential observations from Figure 5.18. The first observation is that the Improved pHEMT XMBE56 \(g_{m_{\text{max}}}\) is 11.7 \% lower compared to the Conventional pHEMT XMBE171, even though the Improved pHEMT has a 50 \% shorter gate (0.5 \(\mu\)m vs 1 \(\mu\)m). This is due to the fact that the extrinsic transconductance \(g_m\) of pHEMT devices is inversely proportional to the gate to channel distance [116], where the Conventional pHEMT XMBE171 distance is 50 \(\text{Å}\) shorter. Referring to Figure 5.10 and 5.11, the difference in the gate-to-channel distance is given by the spacer layer thickness, whereby the spacer layer for Improved pHEMT XMBE56 is thicker than the spacer layer of the Conventional pHEMT XMBE171, hence reducing the electron transfer efficiency from the delta-doped donor layer into the 2DEG quantum well. The impact of the thicker spacer layer thickness of the Improved pHEMT XMBE56 can be seen from the Hall Effect measurement data in Table 5.3, where the 2DEG Sheet Carrier Concentration of the Improved pHEMT XMBE56 is 22\% lower compared to the Conventional pHEMT XMBE171. Note that it is important to maximize the 2DEG Sheet Carrier Concentration to achieve large transconductance as well as large drive currents [80].

Furthermore, the transconductance is also related directly to the Saturation Velocity \(V_{sat}\) and Gate Capacitance \(C_g\), according to Equation 3.1. As the channel material of the Improved pHEMT XMBE56 and Conventional pHEMT XMBE171 are similar, i.e. In\(_{0.7}\)Ga\(_{0.3}\)As, their \(V_{sat}\) values are also similar, i.e. \(2.6 \pm 0.2 \times 10^7\) cm/s [75, 117] while the \(C_g\) for the Conventional pHEMT XMBE171 should be higher compared to the Improved pHEMT XMBE56, according to Equation 3.2. The fact that \(C_g\) for the Conventional pHEMT XMBE171 is higher than the Improved pHEMT XMBE56 is due to the shorter gate-to-channel distance, and the larger gate
length \( L_g \) compared to the Improved pHEMT XMBE56. In short, the extrinsic transconductance for the Improved pHEMT XMBE56 is lower than that for the Conventional pHEMT XMBE171, mainly due to the impact of gate to channel distance and \( C_g \), while the shorter gate length and \( V_{sat} \) do not seem to have much effect. On the other hand, the lower saturation current (\( I_{DSS} \)) and lower carrier concentration sheet carrier density mentioned leads to lower \( g_m \) in the Improved pHEMT XMBE56.

The second observation is that the shift in the two plots is consistent with the shift in the \( V_{th} \) in Figure 5.17, for same reason - i.e. the influence of gate-to-channel distance.

![Figure 5.18 XMBE171 (Conventional pHEMT) and XMBE56 (Improved pHEMT) Extrinsic Transconductance (\( g_m \)) at \( V_{DS} = 1 \) V with 2 x 100 \( \mu m \) gate width.](image)

Figure 5.18 XMBE171 (Conventional pHEMT) and XMBE56 (Improved pHEMT) Extrinsic Transconductance (\( g_m \)) at \( V_{DS} = 1 \) V with 2 x 100 \( \mu m \) gate width.
In the DC characteristics presented in Figure 5.19 and Figure 5.20, significant advantages can be seen of the Improved XMBE56 pHEMT over the Conventional XMBE171 pHEMT. In Figure 5.19 - the off-state Schottky gate leakage current - the reverse bias curves for the Improved pHEMT XMBE56 gate current leakage is -28 µA/mm @ $V_{GS} = -4$ V, compared to -2500 µA/mm or -2.5 mA/mm at the same $V_{GS}$ biasing for the Conventional pHEMT XMBE171. This is better than a 99 % reduction, which could result in an excellent low-noise device. In addition, at a reference gate current $I_{GS}$ of 1mA/mm, the XMBE56 off-state breakdown voltage ($V_{BR}$) is higher than that of XMBE171. The extrapolation of XMBE56 at the reference $I_{GS}$ gives roughly a $V_{BR}$ of -6 V compared to -1.6 V for XMBE171; this is about a 73 % improvement in $V_{BR}$ compared to the Conventional XMBE171 and also other reported research work [118, 119]. The benefit of this high- breakdown voltage of XMBE56 could also make it a good low noise amplifier in a receiver, while requiring minimal protection circuits.

The forward bias curves in Figure 5.19 are important in extracting the Schottky diode characteristics of the devices - the Barrier Height ($\Phi_B$) and Ideality Factor ($\eta$). XMBE56 has a $\Phi_B$ of 0.53 eV and $\eta$ of 1.37, thus demonstrating a good Schottky contact. Likewise, the extracted values for XMBE171 are a $\Phi_B$ of 0.50 eV and $\eta$ of 1.60, which are substantially degraded compared to the Improved pHEMT.
Figure 5.19 XMBE171 (Conventional pHEMT) and XMBE56 (Improved pHEMT) off-state Schottky gate leakage current at $V_{GS} = -4\,\text{V}$.

Another key advantage of the Improved XMBE56 pHEMT, as previously mentioned, is shown in Figure 5.20 and Figure 5.21; these figures show exceptional results for the on-state gate leakage current when compared to the Conventional pHEMT XMBE171. At biasing $V_{DS} = 1\,\text{V}$, the on-state Schottky gate current leakage, which is caused by impact ionization, is only about $-5.2\,\mu\text{A/mm}$ compared to $-2000\,\mu\text{A/mm}$ (or $-2\,\text{mA/mm}$) for XMBE171. Under the same circumstances, at $V_{GS} = -3\,\text{V}$, XMBE56 also shows very low reverse Schottky gate current leakage due electron tunnelling i.e. $-17\,\mu\text{A/mm}$, whereas XMBE171 has a very high value of $-6000\,\mu\text{A/mm}$ (or $-6\,\text{mA/mm}$).
Figure 5.20 XMBE171 (Conventional pHEMT) and XMBE56 (Improved pHEMT) on-state Schottky gate leakage current at $V_{GS} = -3$ V, in mA-range.

Figure 5.21 XMBE56 (Improved pHEMT) On-state Schottky gate leakage current, in $\mu$A-range.
As has been noted from the performance of both off-state and on-State Schottky gate current leakage of XMBE56, the excellent results are due to modification of the epitaxial layer design, not only the low temperature (LT) In$_{0.52}$Al$_{0.48}$As buffer (grown at $< 200$ °C), but also the thicker spacer, which gives a remarkable improvement over the conventional low noise pHEMT. As explained in sections 4.2.1.1 and 4.3.1, the thicker spacer used in XMBE56 has the same effect as the epilayer improvement in XMBE210, mentioned in these sections, where it reduces the efficiency of electron transfer from the donor/supply layer to the 2DEG. For this reason, the concentration of electrons in the 2DEG will be less, consequently lowering the rate of impact ionization in the channel. Furthermore, the thicker spacer is also capable of reducing the number of holes - generated from the impact ionization process in the channel - from being collected by the gate, which is negatively biased. Moreover, unlike other XMBE210 epilayers improvement i.e. the strained In$_{0.3}$Al$_{0.7}$As barrier which increase the Schottky barrier height, the mechanism to reduce the both off-state and on-state gate current leakages in XMBE56 is through the improvement of the buffer layer. As mentioned in Section 2.4.4, the leakage mechanism is also contributed by the buffer layer, hence one of the methods for buffer layer optimization is by using low temperature (LT) buffers. The LT buffer gives high resistivity [36, 50, 55, 120] and reduces injection of electrons from the channel into the buffer and substrate, and undesirable electron flow from source to drain in the buffer and substrate. As these electrons in the buffer and substrate are far from the gate, where the gate modulation will be inefficient, the reduction of these leakages through the buffer and substrate will lower the excess in drain current and suppress the reverse gate leakage current, and it will also increase the $V_{BR}$ [13, 55].

As mentioned previously in Section 2.4.4, the holes that are generated from impact ionization can create a leakage path for the holes inside the buffer, hence these holes have a positive fixed charge, increase the injection of the hot electrons to the channel and buffer, and hence increase the reverse gate leakage current [55, 56].
The high resistivity of the LT buffer also helps to make the electrons from source to drain more confined in the channel layer [121], and hence reduce leakage to the buffer. Furthermore, the In$_{0.52}$Al$_{0.48}$As Barrier$_1$ layer, grown after the LT-In$_{0.52}$Al$_{0.48}$As buffer (refer Figure 5.11 on the XMBE56 epitaxial layer) does not use the super lattice (SL) structure, as previously performed by other researchers [120, 122]. Without using SL, which is well-known to smoothen the layer surface and stop defect threading, XMBE56 epilayer still exhibits attractive pHEMT device features, and can be used in low noise millimetre-wave MMICs (Monolithic Microwave Integrated Circuits) and high power millimetre-wave application devices.

5.3.3.2 Radio Frequency (RF) Characteristics

The extraction of the small signal S-parameters through RF measurement at room temperature was performed for both the Improved XMBE56 and Conventional XMBE171 pHEMTs. The method of measurement was similar to that described in Chapter 3 and Chapter 4, but on two-gate- fingered devices, with 2 x 100 μm (200 μm) gate width and 5 μm Source-Drain separation. The RF characteristics of both of the measured devices were extracted under biasing at each device’s maximum or peak $g_m$ - details of the RF biasing values are summarized in Table 5.5.
Table 5-5 RF biasing conditions for XMBE56 (Improved) and XMBE171 (Conventional).

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Improved pHEMT</th>
<th>Conventional pHEMT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$g_{\text{mmax}}$ (mS/mm)</td>
<td>410 ± 5</td>
<td>459 ± 5</td>
</tr>
<tr>
<td>$V_{\text{DS}}$ (V)</td>
<td>1.0</td>
<td>1.0</td>
</tr>
<tr>
<td>$V_{\text{GS}}$ (V)</td>
<td>-0.47 ± 5</td>
<td>-0.61 ± 5</td>
</tr>
<tr>
<td>$I_{\text{DS}}$ (mA/mm)</td>
<td>171.5 ± 1</td>
<td>173.3 ± 1</td>
</tr>
</tbody>
</table>

The results from the RF measurement are shown in Figure 5.22 and Figure 5.23 for the cut-off frequency ($f_T$) and the maximum frequency ($f_{\text{max}}$) respectively. Note that the VNA used in this RF measurement have capability to sweep frequency only until 20 GHz, hence for the submicron device i.e. the Improved XMBE56, the value of $f_T$ and $f_{\text{max}}$ were extrapolated with a slope of -20 dB/decade.

Figure 5.22 Unity Current Gain or Cut-off Frequency ($f_T$) at $g_{\text{mmax}}$ for $V_{\text{DS}} = 1$ V biasing.
A high $f_T$ of 50 GHz was observed for the Improved XMBE56 device, compared with the Conventional XMBE171. The improvement is about a 58% increase in $f_T$, due to the employment of a 0.5 μm submicron T-gate length in XMBE56, compared to the 1 μm flat gate length in XMBE171. It is important to note that, even with lower output current ($I_{DS}$) and transconductance ($g_m$) as shown in the DC characteristics, the XMBE56 device can still achieve a very high $f_T$ compared to XMBE171. Further comparison of $f_T$ improvement of VMBE#1998 is shown in Chapter 3 and for XMBE56 in this chapter; the $f_T$ improvement of VMBE#1998 is just 30% compared to 58% for XMBE56. The improvement is significant for XMBE56, due to the incorporation of a “new optically-defined submicron gate length” method, which is able to shrink the gate length by roughly 50%, in contrast with VMBE#1998 where the gate shrinkage is just 20% when relying only on the new resist mix. Hence, Equation 5.1 proves that the $f_T$ is strongly dependent on the gate length i.e. the shorter the gate length the higher the $f_T$.  


In the same manner, the maximum frequency \( (f_{\text{max}}) \) of the XMBE56 submicron T-gate length device is also improved. The \( f_{\text{max}} \) is 60 GHz, which is about a 33 % increase compared to the 1 μm flat gate length in XMBE171. It is important to realize that, unlike \( f_{\text{r}} \), the parasitic elements such as \( R_{G} \) (gate resistance) and \( C_{GD} \) (gate-drain capacitance) play an important role in \( f_{\text{max}} \) [32]. Hence, the incorporation of T-shaped gate for the submicron gate length helps to minimize the parasitic elements, which is important for future fabrication of low noise amplifiers as it allows the noise figure to be minimised.

Figure 5.23 Unilateral Power Gain or Maximum frequency \( (f_{\text{max}}) \) at \( g_{\text{mmax}} \) for \( V_{DS} = 1 \) V biasing.
5.4 CONCLUSION

The early part of this chapter concentrated on finding ways to optimize the in-house developed submicron process, which uses a conventional closed-chamber setup. The key investigation was to develop techniques to further scale-down the bottom gate opening to less than 0.25 μm, for pattern transfer to a silicon nitride (Si$_3$N$_4$) hard mask layer. In reality, the conventional closed chamber design had limitations, and could only shrink the initial 1 μm opening down to a minimum of 0.25 μm. However, recently, the novel idea of using an open chamber design was tried, and proved to be very successful. Preliminary runs using this improved open soft reflow chamber setup look very encouraging, and may achieve 0.19 μm or 190 nm bottom gate openings. In fact, there is still room for further optimization of this - work is still in the development phase.

The practicality of this optimized soft reflow process has been realized through the fabrication of a T-gate pHEMT device, which for this study has a bottom gate footprint of 0.5 μm. The next part of the chapter focuses on the design of an epitaxial structure, fabrication and characterization of a 0.5 μm T-gate length InP-based pHEMT incorporating InGaAs-InAlAs material systems. The purpose of this part of study is to improve the conventional 1μm flat gate length InGaAs/InAlAs/InP pHEMT, reducing the high gate leakage current and improving the low breakdown voltage, which impede its performance in low noise devices.

This chapter confirms that, by employing a low temperature (LT) In$_{0.52}$Al$_{0.48}$As buffer (grown at < 200 °C), together with the thicker spacer in the new design, the improved pHEMT XMBE56 demonstrated a significant enhancement in the breakdown voltage and reduction in off-state and on-state Schottky gate leakage current. The DC characteristics, upon successful completion of the fabrication and characterization of improved structure, demonstrate breakdown voltage and gate current leakage improvements of over 70% and 90% respectively, compared to the
conventional XMBE 171 InGaAs-InAlAs pHEMT device. These are significant improvements that make this device suitable for low-noise applications.

The new optically-defined submicron gate length process using conventional I-line optical lithography also indicates an increase of about 58 % and 33 % in $f_T$ and $f_{\text{max}}$ respectively, compared to the conventional XMBE171 pHEMT with a 1 μm gate length and 200 μm gate width. Consequently, this improved structure, together with a submicron gate length, has demonstrated a device with a high breakdown voltage coupled with ultra-high speed and low noise.
CHAPTER 6

SUBMICRON T-GATE PROCESS OPTIMIZATION

6.1 OVERVIEW T-GATE

In submicron gate-length devices, a low gate resistance is essential to the fabrication of pHEMTs for high-gain, low-noise, and high-power applications. The most widely-used gate cross-sectional structure is the T-shaped or mushroom-shaped gate, formed using a multi-layer resist technique with e-Beam lithography [105, 123, 124]. In this structure, the smaller footprint - or bottom of the T - defines the gate length, and the wider top of the T provides a low resistance. A tri-layer resist system, PMMA/P(MMA,MAA)/PMMA is used to define T-gates [125] (PMMA is polymethylmethacrylate, and the other materials are copolymers of PMMA).

In this study, the new bi-layer soft-reflow process developed at the University of Manchester and described extensively in chapter 5 is used to fabricate sub-micron device feature lengths solely through optical lithography [126].

The conventional Manchester soft-reflow process flow to fabricate submicron pHEMT is shown in Figure 6.1, where the bottom gate footprint is defined after the Ohmic contact step. A modification to this process flow is shown in Figure 6.2, making it easier to deposit the hard mask layer at the very first step to define the bottom gate trench; this will help to save resources and time, and also allows for more control of the reflow process and optimization. In addition, deposition of the hard layer gives advantages in terms of better film uniformity and improved surface profile for the soft reflow stage.
6.2 OVERVIEW HARD MASK

Soft Reflow is an all optical process developed at the University of Manchester to realize a submicron T-Gate pHEMT without recourse to e-Beam lithography. The process uses Silicon Nitride (Si$_3$N$_4$) as a hard mask in order to mechanically support
the T-Gate structure [126]. Nevertheless, improvement and characterization of Spin-on-Glass (SoG) as a low cost fast process alternative material for hard masks was undertaken in this study, in order to replace Silicon Nitride (Si$_3$N$_4$) (See Figure 6.3 and 6.4). These processes, plus the use of SoG as a hard mask, offer a simple yet cost-effective solution to the e-Beam lithography of nanometre-scale gate length transistors.

Figure 6.3 Silicon Nitride (Si$_3$N$_4$) as stem for T-Gate structure. (Picture just for illustration).
Notably, in this study, SoG film thickness has been thinned down to 138 nm, permitting a ~ 150 nm gate length device to be realized through fabrication. The main challenge in achieving this is that it is typically necessary to plasma etch the SoG at high power (>100W), which is known to degrade the 2DEG carriers. Significantly, this study demonstrates that this type of SoG film can be etched at very low power (20W) and at very low pressure (< 25mTorr). To avoid film cracking, most researchers [111, 127] employ multiple coating and ramping techniques, with baking temperatures ranging from 80 °C to 230 °C. Remarkably, no cracks were observed in this study, even though only a single coating and baking temperature of 200 °C, were used - this further simplifies the SoG process.
In general, SoG had been used extensively for different types of applications, such as planarization in multi-level metal interconnect processes [127], and fabricating waveguide devices [128]. In this study, it is applied not only as the hard mask for a three dimensional T-gate geometry, but also demonstrates that the SoG can be used in a soft reflow process.

6.3 SPIN-ON-GLASS (SOG) MATERIAL DEVELOPMENT

6.3.1 Introduction

Typically, Silicon Nitride (Si$_3$N$_4$) is deposited through Plasma-enhanced Chemical Vapour Deposition (PECVD), which can take almost one day to perform. There is therefore a strong motivation to evaluate a substitute material which can lead to a shorter deposition time (~ 30 minutes) and a much simpler process (see Figure 6.5).

Figure 6.5 Silicon Nitride (Si$_3$N$_4$) and Spin-on-Glass (SoG) hard mask deposition with its respective equipment.
SoG it is in the form of a liquid, and the basic technique used is planarizing in nature when applied to a surface topography. In addition, the optical and dielectric characteristics are almost identical to those of pure Silicon Dioxide (SiO₂). For this reason, SoG material offers a promising alternative to Silicon Dioxide (SiO₂). Moreover, SoG film can be applied to a wide spectrum of flat surfaces, by means of dipping, spraying or spinning. Accordingly, the spinning coating method shown in Figure 6.5 is used for this study, to achieve precise flatness control and utmost uniformity.

The SoG film type that is utilized in this study is Silicafilm [129], an alcohol solution which produces a pure SiO₂ film when dispensed on to a semiconductor surface. The thickness of the SiO₂ film formed from Silicafilm is determined by the spinner speed, as will be shown in a later section of this chapter.

### 6.3.2 SoG Deposition

The thickness for the Emulsitone Silicafilm SoG used in this study can vary from 200 nm to 110 nm depending on the spinning speed. As the name implies, SoG is a spin-on process, where the fluid is deposited onto a sample; for this study, 1.5 cm x 1.5 cm silicon substrate tiles were used throughout the experiments.

The deposition process is divided into four steps: pre-heat, coating, spinning and baking. In the first step, a cleaned silicon sample is pre-heated at 150 °C for 5 minutes on a hot plate, and then cooled down for 1 minute by placing it on a metal plate - these steps are performed at room temperature. The purpose of these steps is to ensure a good adhesion between the coated SoG and the sample’s surface.

Secondly, the sample is put onto the spinner chuck and 10 drops of the Silicafilm SoG is dispensed at the centre of the sample prior to spinning. From experience, 10
drops is sufficient for the type of sample used; fewer than 10 drops will sometimes cause uneven coverage or uniformity throughout the sample after spinning.

The coated sample is then spun at the desired speed for the thickness of choice for 30 s. During this time, the liquid film will spread uniformly across the entire sample and the solvents in the liquid will eventually evaporate, leaving a thin film of solid component [130] on the sample.

Finally, baking the sample on a hot plate at 200 °C for 15 minutes will turn the thin film of solid component into SoG. Some studies [111, 127] use sequences of hot plate bakes from low to high temperature, with one minute of baking for each temperature, then high temperature (> 350 °C) curing in an oven with Nitrogen flow, to prevent oxidation of the SoG which will form flakes. However, such a lengthy baking sequence and curing were not performed in this study, as no flakes were observed during the process adopted here.

Figure 6.6 shows the surface profile of the SoG at 3000 rpm spin-speed - the surface roughness is normal and should be less than +/-5 % based on supplier feedback [131]. All of the samples produced in this study have the type of striations shown, which converge in the centre and spoke outwards.
6.3.3 Thickness Evaluation

Silicafilm SoG has a nominal thickness of 200 nm, but this can be varied as mentioned previously. Thickness variation can be performed by changing the spin speed from 1500 rpm to a maximum of 10,000 rpm, however, the spinner used for this study only has capability up to 8000 rpm. In order to determine the SoG thickness under these different coating spin-speeds, an experiment was conducted where the spinner speed was set at 1500 rpm, 3000 rpm, 6000 rpm and 8000 rpm, while the spin time was fixed at 30 seconds and the baking time 15 minutes at 200 °C. The data is presented in the spin-speed curve shown in Figure 6.7.
As expected, the thickness of the SoG film will be reduced if the spin-speed increases; the thinnest SoG film was found at the maximum speed of 8000 rpm, while the thickest film was at the slowest speed of 1500 rpm. The green curve is the data from the supplier, where the minimum spin-speed is 3000 rpm while the maximum spin-speed is at 10000 rpm. These two curves look comparable with the blue curve showing a slightly increased thickness of 16nm compared with the supplier data which is acceptable and within process tolerances. The colour of the SoG film is also different from one thickness to another, as shown in Figure 6.8. These colours represent variations in thickness as the light refracts differently.
Figure 6.8 Silicafilm SoG colours at different thickness with respect to spin speed.

It should be noted that the etch study had not yet been performed at this point, so the thickness check was performed using a lift-off process, which is illustrated in Figure 6.9. The SoG thickness measurements were performed using a DEKTAK 3 ST surface profiler, and a typical result is shown in Figure 6.10. The measurement indicates substantial surface roughness due to surface patterns formed similar to those in Figure 6.6. However, the average top value from the centre line is 225nm and the average bottom value from the centre line is 207nm, so the variance from 225 nm to 207 nm is +/-9 nm from the mean of 216 nm, or less than 5%. Therefore, this lift-off process concept is unique, repeatable and gives a high degree of confidence in the measurement results, where the thickness of the Silicafilm SoG can eventually be judged solely by its colour.
Figure 6.9 Lift-off process to determine Silicafilm SoG thickness.

Figure 6.10 Silicafilm SoG thickness measurement at spin-speed 3000 rpm and spin time 30 s.
6.3.4 Pin Hole Verification

The quality of a thin film is sometimes affected by the defects on the film surface, or by pinholes, which have the potential to cause reliability problems and short-circuits. Hence for this study, the SoG coated samples are inspected under a digital microscope for any major defects or pinholes. As far as this study is concerned, the 216 nm and 138 nm SoG thickness samples did not have any defects or visible pinholes. However, as a precaution, pinholes were investigated further by fabricating a Metal-Insulator-Metal (MIM) capacitor. If the thin film which is the dielectric or insulator of the capacitor has pinholes, then it will exhibit a short-circuit - Figure 6.11 illustrates this technique further.

Figure 6.11 Lift-off process to fabricate MIM capacitor using Silicafilm SoG as dielectric for pin holes verification.
Referring to Figure 6.11, visual inspection throughout the sample showed no pinholes, cracks or defect on the SoG on metal 1. After metal 2 or top metal evaporation, the capacitor structure was then tested for continuity (i.e. short-circuit) using a multimeter. If the SoG had pinholes, it would have allowed metal 2 to be in contact with metal 1 below. A 100% continuity check on the capacitors gave 100% yield with no short-circuits, therefore the 216 nm and 138 nm SoG films are reliable and suitable for use as an alternative hard mask layer for submicron reflow processes.

6.3.5 Etch Rate Study

Silicafilm SoG is actually formed from silicon dioxide, and the etching is therefore likely to be identical to that for silicon dioxide. In the literature [111, 132], the etching used is either thru plasma etching or wet etching. However, for this study, plasma etching is desirable as it is a more anisotropic method, and therefore suitable for defining submicron trenches.

In this study, the etching is done using a Reactive Ion Etching (RIE) plasma chamber. The etching parameters used need to be as close as possible to those used to etch Si₃N₄ as previously mentioned i.e. low RF power and low pressure. Low RF power needs to be maintained to avoid degradation of the 2DEG later on when making a device, and low pressure can minimize loading effects. The etching time must also be reasonably short, as longer times will erode the S1805 resist which is only 500 nm in thickness. All of these restrictions are a challenge in etching SoG, since - as reported in most literature [133, 134] - the minimum RF power required to etch SiO₂ or SoG is 100 W, and the resist thickness is usually more than 2 μm.

Initial etch rate studies were conducted using a silicon samples coated with Silicafilm SoG with a thickness of 216 nm. This thickness is achieved with a 3000
rpm spin-speed for 30 s and soft bake at 200 °C for 15 minutes. These etch study samples were then patterned with S1805 resist to determine the etch rate and selectivity. The runs and results for this study are tabulated in Table 6.1.

<table>
<thead>
<tr>
<th>Sample</th>
<th>O₂ (sccm)</th>
<th>CF₄ (sccm)</th>
<th>% O₂</th>
<th>Amount etched resist (nm)</th>
<th>Amount etched SoG (nm)</th>
<th>Selectivity dSoG/dRes</th>
<th>SoG etch rate (nm/min)</th>
<th>PR etch rate (nm/min)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>0</td>
<td>50</td>
<td>0</td>
<td>111.2</td>
<td>131.0</td>
<td>1.2</td>
<td>26.2</td>
<td>22.2</td>
</tr>
<tr>
<td>B</td>
<td>4</td>
<td>50</td>
<td>7</td>
<td>259.4</td>
<td>167.7</td>
<td>0.6</td>
<td>33.5</td>
<td>51.9</td>
</tr>
<tr>
<td>C</td>
<td>8</td>
<td>50</td>
<td>14</td>
<td>353.1</td>
<td>191.3</td>
<td>0.5</td>
<td>38.3</td>
<td>70.6</td>
</tr>
<tr>
<td>D</td>
<td>12</td>
<td>50</td>
<td>19</td>
<td>403.8</td>
<td>167.6</td>
<td>0.4</td>
<td>33.5</td>
<td>80.8</td>
</tr>
<tr>
<td>E</td>
<td>16</td>
<td>50</td>
<td>24</td>
<td>427.1</td>
<td>135.0</td>
<td>0.3</td>
<td>27.0</td>
<td>85.4</td>
</tr>
</tbody>
</table>

All 5 samples were run with a constant CF₄ at 50 sccm, and the Oxygen (O₂) flow rate was varied from 0 to 16 sccm. Details of the plasma etch parameters are described below.

Dry etching recipe:

- Power : 20 W
- CF₄ / O₂ flow rate : 50 sccm / (0, 4, 8, 12 and 16) sccm (keep CF₄ flow rate constant)
- Chamber pressure : 50 mTorr
- Time : 5 mins
As mentioned previously, the RF power is kept minimum at about 20 W and the chamber pressure is at its lowest possible level. The chamber pressure could not be lowered than 50 mTorr as it is already the gases mix (CF$_4$ plus O$_2$) pressure. However, if only CF$_4$ gas is used, the pressure can be further reduced to 21 mTorr, but for experimental purposes the pressure was kept constant at 50 mTorr. Further analysis can be deduced by referring to Figure 6.12 and 6.13.

![Figure 6.12 Silicafilm SoG 216 nm thickness etch rate vs percentage of O$_2$.](image)
Figure 6.13 shows that at 14% O$_2$ concentration, the SoG / PR selectivity has a ratio of approximately 1:2, which means that for a 10 nm SoG etch, 20 nm of photoresist (PR) will be etched at the same time. The selectivity to SoG also decreases as the O$_2$ concentration increases - this is expected as O$_2$ plasma can erode photoresist faster. At this stage, even though the selectivity to the photoresist is not promising at 14% O$_2$, the SoG etch rate is the highest (38.3 nm/min), and there is still half of the S1805 photoresist remaining from the 500 nm initial thickness. Hence 50 sccm CF$_4$ / 8 sccm O$_2$ mixtures was chosen to be used for Silicafilm SoG throughout the study, and motivating further etch studies to be performed on the thinner 138nm SoG. Based on the 38.3 nm/min etch rate, it should theoretically be possible to clear the 138 nm SoG in 3.6 minutes and yet still have half of the S1805 photoresist left.

Further etch rate studies used a silicon samples coated with Silicafilm SoG with a thickness of 138 nm. This thickness was accomplished using coating parameters of
8000 rpm spin-speed for 30 s and soft bake at 200 °C for 15 minutes. The sample for this etch study was also patterned with S1805 photoresist to determine the etch rate and selectivity. The plasma etching parameters were kept the same as those for the 216 nm SoG for comparison purposes later on. The results and comparison with 216 nm SoG thickness are shown in Table 6.2.

Table 6-2 Silicafilm SoG 138 nm and 216 nm thickness etch rate and selectivity comparison.

<table>
<thead>
<tr>
<th>Sample</th>
<th>Description</th>
<th>O2 (sccm)</th>
<th>CF4 (sccm)</th>
<th>% O2</th>
<th>Amount etched resist (nm)</th>
<th>Amount etched SoG (nm)</th>
<th>Selectivity dSoG/dRes</th>
<th>SoG etch rate (nm/min)</th>
<th>PR etch rate (nm/min)</th>
</tr>
</thead>
<tbody>
<tr>
<td>C</td>
<td>216 nm (Pattern)</td>
<td>8</td>
<td>50</td>
<td>14</td>
<td>353.1</td>
<td>191.3</td>
<td>0.5</td>
<td>38.3</td>
<td>70.6</td>
</tr>
<tr>
<td>F</td>
<td>138 nm (Pattern)</td>
<td>8</td>
<td>50</td>
<td>14</td>
<td>334.4</td>
<td>131.6</td>
<td>0.4</td>
<td>26.3</td>
<td>66.9</td>
</tr>
</tbody>
</table>

The result in Table 6.2 show that the etch rate of 138 nm SoG is lower than that for 216 nm SoG, which was evaluated previously. This shows that the changes to the SoG thickness will also change the etch rate, making it lower for thinner SoG. However the resist etch rate and selectivity for 14 % O2 in the CF4 / O2 gas mixture is roughly the same, and there was still approximately 150 nm of resist left. It might therefore not be possible to etch for more than 6 minutes for both SoG thicknesses mentioned. Figure 6.14 shows the images for the result shown in Table 6.2. Note that the 216 nm SoG is not fully etched after 5 minutes, but the 138 nm SoG is cleared (it is possible to see the silicon surface).
To further advance the etch studies, thicker resists were evaluated to cater for longer etch times, which in turn should give more margin on the etch rate for the 138 nm SoG. Therefore, the current S1805 resist was made thicker, from 500 nm to approximately 700 nm, by reducing the coating spin-speed from 4000 rpm in 30 s to 2000 rpm in 30 s. Shipley S1813 resist was also evaluated, as the thickness is about 1.5 µm or 1500 nm. However, S1813 resist needs 20 minutes for edge bead removal (EBR) - this is to ensure the 1µm gate opening is achievable. The results for these runs is shown in Table 6.3.
Table 6-3 Silicafilm SoG 138 nm etch rate and selectivity on thicker resist.

<table>
<thead>
<tr>
<th>Sample</th>
<th>Description</th>
<th>Average Resist thickness (nm)</th>
<th>O₂ (sccm)</th>
<th>CF₄ (sccm)</th>
<th>% O₂</th>
<th>Amount etched resist (nm)</th>
<th>Amount etched SoG (nm)</th>
<th>Selectivity dSoG/dRes</th>
<th>SoG etch rate (nm/min)</th>
<th>PR etch rate (nm/min)</th>
</tr>
</thead>
<tbody>
<tr>
<td>S1805 (2000 rpm)</td>
<td>138 nm (Pattern)</td>
<td>696</td>
<td>8</td>
<td>50</td>
<td>14</td>
<td>353.1</td>
<td>191.3</td>
<td>0.5</td>
<td>38.3</td>
<td>70.6</td>
</tr>
<tr>
<td>S1813 (20 mins EBR)</td>
<td>138 nm (Pattern)</td>
<td>1496</td>
<td>8</td>
<td>50</td>
<td>14</td>
<td>334.4</td>
<td>131.6</td>
<td>0.4</td>
<td>26.3</td>
<td>66.9</td>
</tr>
</tbody>
</table>

The experiment for the thicker resists were executed using similar plasma etching parameters as used before, except that the etching time was extended from 5 minutes to 7 minutes. The etch rate data from Table 6.3 also shows that the resist thicknesses remaining are sufficient for both types of the thicker resists (S1805 and S1813), even after 7 minutes of etching, with all the 138 nm SoG cleared. However the selectivity to photoresist remains low due to the use of 8 sccm O₂.

As a conclusion for this etch study on 216 nm and 138 nm SoG, the etch recipe developed in this experiment is the only one which uses very low power and low pressure compared to the literature, which uses RF power > 100W [133, 134]. It is suitable for etching the SoG, especially the 138 nm material. Most studies also use a thick resist (>2 μm), but in this study the resist thickness initially was only 500 nm, yet the etching of 138 nm SoG could be completed in 5 minutes with some resist still remaining. If it is necessary to over-etch to cater for micro-loading in small features less than 250 nm, such a thickness may not be sufficient. However,
evaluation of thicker resists of S1805 (2000 rpm) and S1813 made it possible to extended the etching time, and it is now possible to use 138 nm SoG as a hard mask for the submicron soft reflow study.

In addition, the 138 nm SoG could be used as a passivation layer, and can be etched with the plasma etching recipe previously discussed (5 minutes etching time for standard S1805 and 7 minutes for thicker S1805 and S1813 with 20 minutes EBR).

6.3.6 Soft Reflow Verification and Issue

The main motivation for the use of SoG is to offer alternatives for hard mask layers for the submicron soft reflow study. This SoG coating process is simpler and less time consuming compared with the Si$_3$N$_4$ deposition process. Hence, with the success in the etch rate studies using thicker resists, the study of 138 nm SoG could be continued in future for use in ~ 100 nm gate soft reflow. The trial runs used thick S1805 and S1813 (20 minutes EBR) patterned on silicon samples. To recap, the coating and plasma etching parameter were as follows:

Coating and Etching Parameters:

- 138 nm SoG on Silicon
  - 8000 rpm spin-speed for 30 s
  - 200 °C softbake for 15 minutes
- Dry etching recipe:
  - Power : 20 W
  - CF$_4$ / O$_2$ flow rate : 50 sccm / 8 sccm
  - Chamber pressure : 50 mTorr
  - Time : 7 minutes
The results for the 90 s soft reflow runs are shown in Figure 6.15 and Figure 6.16 for thicker S1805 and S1813 (20 minutes EBR), respectively.

Based on the results shown in Figure 6.15 and Figure 6.16, the soft reflow worked successfully on the 138 nm SoG as a hard mask layer. The initial 1 μm features shrunk after 90 s reflow at a temperature of 34 °C. However, unexpected results after plasma etching and cleaning show that the dimensions were enlarged back to nearly 1 μm. The only possible explanation for this phenomenon is that the longer etching time might have eroded the resist in the reflowed area, and the use of 8 sccm O₂ makes the erosion faster - Figure 6.17 illustrates the problem.

Figure 6.15 Soft reflow for 90 s at temperature 34 °C on S1805 (2000 rpm) thicker resist.
Figure 6.16 Soft reflow for 90 s at temperature 34 °C on S1813 (20 minutes EBR) resist.

Figure 6.17 Resist erosion is faster in the reflowed area during plasma etching.
It is clear from Figure 6.17 that the resist is thinner in the reflowed area. Hence, at present, the 138 nm SoG is not suitable for submicron hard mask layers, due to limitations in etching time, since a shorter etch time raises concerns about the micro-loading, and a longer etching time will erode the reflowed area, making the dimension enlarged after etching.

Another avenue which could be explored in the future is the use of much thinner SoG material, with a thickness of around 30 nm to 50 nm. The same process as described throughout this chapter will need to be repeated for the new SoG material.

6.4 CONCLUSION

This chapter was mainly focused on studying an alternative material for depositing a hard mask layer for submicron process realization. The aim is not only to reduce material cost, but also to reduce the time required from approximately 1 day to just 30 minutes. Further time savings can be achieved from not requiring a PECVD machine tool time and down time, which are much more complex compared to the spinner.

This study has had demonstrated and explored the possibility of using Spin-on-Glass (SoG) material as an alternative to Silicon Nitride (Si₃N₄) hard mask deposition. As mentioned earlier, the motivation for this study is that the SoG deposition process is much simpler than depositing Si₃N₄, additionally the deposition of this SoG film is also simpler, requiring only a single step spin coating and single step baking on a hot plate, yet without flakes or cracks being observed which had previously been seen by other researchers. The 100 % yield from a MIM capacitor test showed no pin holes, which demonstrate a high quality film.

The key challenging in the use of this SoG film is the etching, as it typically requires high RF power (>100W) due to its properties being similar to Silicon
dioxide (SiO$_2$), which is known to be a hard material to be etch. Nevertheless, in order to maintain low power (20 W) to avoid degrading future fabricated device 2DEG, intensive etch studies were performed, and a successful recipe to etch SoG of 216 nm and 138 nm thickness was developed. This study therefore validates the claim that this SoG film can also be used for soft reflow process.

Apparently, the developed etching recipe has low selectivity to resist, and was etched severely around the thinner reflowed area, making the reflowed area wider after etch. This prohibits the use of this excellent film in the hard mask for a submicron reflow process and also for a submicron T-gate’s stem.

Due to time constraints and the nature of this study, which could extend to several months, it was decide that the SoG film will not be implemented for the hard mask for subsequent research in this work. Under these circumstances, the next chapter on submicron device fabrication will revert back to the Si$_3$N$_4$ film. However, as mentioned previously, the developed Silicafilm SoG could be implemented as a passivation layer or as dielectric for an MIM capacitor, as the etching has no detrimental effect either on the 2DEG or reflowed area and thus from this perspective SoG offers an excellent alternative for both passivation and capacitor fabrications for MMICs.

Future advantage may be gained by exploring the etching of this SoG film - one option would be the use of either a more aggressive gas such as SF$_6$ [135], which has more Fluorine species, or a Buffered Oxide Etch (BOE), to etch the SoG. However, both of these options not available at the moment in the lab where this study is performed. Another key point to realize is that the thinner SoG i.e. 30 nm or 50 nm could be tried, which has good potential for the fabrication of 100 nm gate length InGaAs-InAlAs pHEMTs.
CHAPTER 7

CONCLUSIONS AND FUTURE WORK

7.1 CONCLUSIONS

This research was focused on the optimization and modification of advanced InGaAs/InAlAs/InP pHEMT devices. This material system enables the realisation of ultra-low noise and ultra-high speed devices, through careful device modification by means of bandgap engineering and lateral scaling of the gate length. The high off-state breakdown voltage ($V_{BR}$) resulting from such modification also offers potential for devices to operate in a high power regime. The primary source to produce the excellent pHEMT materials used in this study is an in-house MBE system.

Compared to the AlGaAs/GaAs HEMT and AlGaAs/InGaAs pHEMT, the InGaAs/InAlAs pHEMT is an essential material technology for high frequency operation, due to advantages in higher 2DEG concentration and higher mobilities in the channel, which consequently improve the microwave/millimetre wave noise and gain performance. In addition, the development of double-$\delta$ pulse doping, un-doped cap, low temperature buffer, and sub-micron gate lengths in this study have demonstrated improvements in the device’s DC and RF characteristics.

The conventional InGaAs/InAlAs pHEMT with a highly-strained channel, developed previously at The University of Manchester suffers from high gate current leakage and low breakdown voltage. Therefore the major contribution of this research was to optimise the InGaAs/InAlAs material system to achieve extremely low gate leakage and very high breakdown voltage compared to the conventional pHEMT. Apart from the improvements to the epilayer, the other important contribution of this research was the optimization of the 1 μm gate length and
submicron T-gate fabrication process, based purely on low-cost I-line optical lithography.

For the 1 μm gate length fabrication process optimization, the key issue is the enlargement of the gate length after thermal evaporation of the gate metal. A “mask printed” 1 μm gate opening defined using I-line lithography enlarges by about 13 % after metallization. To overcome this issue, it is possible to optimise the gate opening definition during lithography, rather than making relatively costly changes to the thermal evaporation process. As a result, mixing and diluting the gate masking resist, based on in-house calculation, successfully reduced the final gate opening to 0.8 μm and finally achieved a roughly 1 μm gate length after gate metallization.

Upon successful optimization of the 1 μm gate length, device fabrication was performed to allow the comparison of the performance of the device using the standard 1 μm resist with the newly- mixed 0.8 μm resist. The DC and RF performance showed significant improvement using the newly mixed 0.8 μm resist, most notably an increase in fT of 30 %. In addition, the device chosen for this fabrication (VMB#E1998) had a better epitaxial structure than the conventional pHEMT as the new material incorporated double delta-doping, a thicker spacer and a highly- doped cap. However, the DC results show unexpectedly high gate current leakage and thus low breakdown voltage. Further verification through a gate recess study showed no improvement. Therefore it is concluded that the issue may be caused by the doped cap; this result leads to the use of an un-doped cap layer for the next epilayer improvement.

The InGaAs/InAlAs material system was further improved with bandgap engineering, which involves a highly-strained Al-rich barrier, double δ-doping, a thicker spacer and an un-doped cap. These modifications significantly improved the conventional low-noise pHEMT, through reducing gate current leakage by 99 % and
increasing off-state breakdown voltage (V_{BR}) by 89%. However, the gate length used in this fabrication still used a 1 μm flat gate technology, which was previously optimised and showed no degradation in RF performance. The noise figure from the simulation also showed improvement compared to the conventional pHEMT. This improvement should allow for the production of excellent low-noise amplifiers, as well as high voltage and high efficiency power amplifiers (PAs).

The 1 μm InGaAs/InAlAs pHEMT cannot be developed to operate at higher frequencies, even with further optimization and band-gap engineering to the epilayer structures. Thus a shorter gate length is key to improving the operating frequency; for this reason, another study was conducted to reduce the gate length to sub-micron dimensions, whilst avoiding high-cost e-Beam lithography. The gate length optimization previously performed by mixing and diluting the gate’s resist was unfortunately found not to be capable of achieving gates shorter than 0.8 μm.

The University of Manchester had developed a soft reflow process for fabrication of submicron T-gates, using a closed-chamber process and incorporating of Si₃N₄ as a hard mask layer. Therefore, this research also aimed to improve the sub-micron soft reflow process and T-gate fabrication. The optimization was divided into two distinct parts - the first part of this optimization aimed to replace the conventional soft-reflow closed chamber with a new improved soft-reflow open chamber design while the second part aimed to replace the Si₃N₄ hard mask layer with a new material that is both cost and time effective and saves in fabricating the T-gate structure.

The first part of the submicron gate length optimization involved improving the conventional soft-reflow closed chamber used for the existing in-house soft reflow process. Such chambers are unable to achieve openings smaller than 0.25 μm. Therefore, the idea of a new and improved soft-reflow open chamber design is presented. This new chamber design leads to the availability of new optically-
defined submicron gate lengths which can shrink the initial gate opening to as small as 0.19 μm. To date, this new process is still under development, and shows promise to allow shrinking of soft-reflowed features down to 0.1 μm, whilst using purely low cost I-line lithography.

Finally, verification of the new optically-defined submicron gate length process was performed by fabricating devices. As this research is mainly aimed at improving the conventional pHEMT, a new device fabrication with a modified epilayer was compared with the conventional pHEMT. The modification of the improved epilayer has almost the same structure as the conventional pHEMT i.e. only a single δ-doped and latticed-matched barrier, but the supply layer is made thicker and the buffer is grown at low temperature. As expected, the improved device showed very low gate current leakage and high breakdown - more than 90% and 70 % respectively - compared to the conventional pHEMT. More significantly, an improvement of 58 % and 33 % in fT and fmax respectively were achieved, compared to the conventional pHEMT, proving that the improved structure, together with the sub-micron T-gate length results in a high breakdown voltage and ultra-high speed device for low noise devices applications.

It is important to note that the gate length used was 0.5 μm not 0.19 μm, achieved using the new improved soft-reflow open chamber design. The original intention was to fabricate pHEMT devices for 0.5 μm, 0.35 μm and then 0.19 μm, however due to unexpected issues, the development was halted at 0.5 μm for this study.

In the second part of this study, a new material hard mask material identified was Spin-on-Glass (SoG). An extensive study was performed to characterize the SoG, especially the etching of this hard-to-etch material. RIE etching recipes were successfully used whilst maintaining low power (< 20W), since for pHEMT processing, a low power level is desirable to avoid degradation of the 2DEG. A less-aggressive etching gas (CF4) was also used, compared to other research which
employed not only high power (>100W) but also more aggressive gas (C\textsubscript{4}F\textsubscript{8} or SF\textsubscript{6}). This SoG was able to act as a hard mask layer to support the soft-reflow process. Unfortunately, due to the nature of the soft reflow, the reflowed area enlarges after RIE etching, hence it is not yet able to replace Si\textsubscript{3}N\textsubscript{4} for T-gate fabrication. Nevertheless, this newly-developed SoG process could still be applied as a dielectric for capacitors, and also as a passivation layer for final device encapsulation.

As has been stated, this research is motivated by the exceptional performance of the InGaAs/InAlAs material system on an InP substrate. The intensive work done on the optimization and modification of the material system, together with the gate length reduction to submicron dimensions, should enable the production of ultra-low-noise and ultra-high-speed devices, mainly for low-noise amplifiers (LNAs) and low-noise receivers operating in the microwave and millimetre wave regime. In addition, the improved off-state breakdown voltage is also attractive for the production of high power amplifiers (PAs).

### 7.2 FUTURE WORK

To date, the device epilayer structures have achieved extremely low gate current leakages both in off-state and on-state operation. Further reduction in sub-micron gate lengths will allow higher frequency operation from X to W-bands applications. The new optically-defined submicron process has laid the groundwork for the fabrication of sub-micron devices while maintaining the use of low cost I-line lithography. Below are some suggestions for future work:

1. The new and improved soft-reflow open chamber design could be explored further to achieve smaller nodes than 0.19 \textmu m, simply by manipulating the shutter openings.

2. The SoG material could be optimised further to be realized as a hard mask
and replacing Si₃N₄. The etching technique could be changed to BOE wet etching rather than RIE etching, however there is a need to take note of the undercut, as wet etching is more isotropic.

3. A tri-layer process - i.e. a sandwich of LOR3A-Si₃N₄-Top resist could be used rather than a bi-layer process. This would be beneficial if there are pin holes or quality issues in the deposited Si₃N₄, as it will not cause shorting to the active layer i.e. parallel conduction, as the Si₃N₄ becomes just a sacrificial layer for the pattern transfer.

4. Development of a gate-first process to reduce misalignments. However this would require non-alloyed Ohmic contact, and would probably need a highly doped cap layer. There will be trade-off between the high leakage and low breakdown, as discussed previously.

5. For low power applications, there is a need to characterize the DC and RF performance at lower V_DS, i.e. less than V_DS = 1 V; a comprehensive characterization needs to be performed done to examine the impact on device performance.

6. The fabricated and characterised sub-micron devices need to be modelled and simulated to evaluate the noise figure, and also to understand the properties of sub-micron devices, which will be beneficial for the development of high-speed circuits, LNAs or PAs.
REFERENCES


[19] F. Packeer, M. M. Isa, W. M. Jubadi, K. W. Ian, and M. Missous, "Fabrication and characterization of tensile In_{0.3}Al_{0.7}As barrier and compressive In_{0.7}Ga_{0.3}As channel pHEMTs having extremely low gate leakage for low-noise applications," Journal of Physics D: Applied Physics, vol. 46, p. 264002, 2013.


[65] I. Thayne, M. Holland, Y. C. Chen, W. Q. Li, A. Pausden, S. Beaumont, et al., "Comparison of 80nm-200nm Gate Length Al0.25GaAs/GaAs/Al0.25GaAs, Al0.3GaAs/In0.15GaAs/GaAs and In0.52AlAs/In0.65GaAs/InP HEMTs," in International Electron Devices Meeting, 1993. IEDM '93. Technical Digest., 1993, pp. 225-228.


[70] M. M. Isa, "Low Noise Amplifiers Using Highly Strained InGaAs/InAlAs/InP pHEMT For Implementation In The Square Kilometre Array (SKA)," PhD, The University of Manchester, 2012.


[86] R. People, K. W. Wecht, K. Alavi, and A. Y. Cho, "Measurement of the conduction-band discontinuity of molecular beam epitaxial grown In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As, N-n heterojunction by C-V profiling," Applied Physics Letters, vol. 43, pp. 118-120, 1983.


[90] X. Letartre, P. Rojo-Romeo, J. Tardy, M. Gendry, D. Thompson, and J. G. Simmons, "InP-InAlAs and InGaP-InAlAs mixed spacers to reduce the gate leakage current in InAlAs/InGaAs/InP HEMTs," in International Conference on Indium Phosphide and Related Materials, 1997., 1997, pp. 384-387.


[100] A. Jin-Ping, Z. Qing-Ming, Z. Yong-Lin, L. Xian-Jie, L. Wei-Ji, I. Shi-Yong, et al., "InP-Based Enhancement-Mode Pseudomorphic HEMT with Strained In$_{0.45}$Al$_{0.55}$As Barrier and In$_{0.75}$Ga$_{0.25}$As Channel Layers," IEEE Electron Device Letters, vol. 21, pp. 200-202, 2000.


[113] K. W. Ian, "Routes To Cost Effective Relisation Of High Perfromance Submicron Gate InGaAs/InAlAs/InP pHEMT," PhD, The University of Manchester, 2013.


APPENDIX A :

BASICS 1 μM pHEMT FABRICATION PROCESS FLOW

<table>
<thead>
<tr>
<th>Structure name</th>
<th>Step</th>
<th>Step-name</th>
<th>Chemical / Solvent</th>
<th>Equipment / Machine</th>
<th>Temp (°C)</th>
<th>Time</th>
<th>Comments / Highlights</th>
</tr>
</thead>
<tbody>
<tr>
<td>MESA / Isolation</td>
<td>1.1</td>
<td>Sample preparation / cleaning</td>
<td>NMP(1165)-Acetone-IPA</td>
<td>USB</td>
<td>RT</td>
<td>5 min each</td>
<td>Lastly dry the sample with N₂.</td>
</tr>
<tr>
<td></td>
<td>1.2</td>
<td>Pre-heat</td>
<td>N/A</td>
<td>Hot-plate</td>
<td>120 °C</td>
<td>1 min</td>
<td>After baking, cool-down on the heat sink for 1 min.</td>
</tr>
<tr>
<td></td>
<td>1.3</td>
<td>Resist-coating</td>
<td>Photoresist: S1805</td>
<td>Spinner</td>
<td>RT</td>
<td>30 s</td>
<td>Program-4 : (Acc=2000, RPM=4000, Duration = 30 s).</td>
</tr>
<tr>
<td></td>
<td>1.4</td>
<td>Pre-bake</td>
<td>N/A</td>
<td>Hot-plate</td>
<td>115 °C</td>
<td>1 min</td>
<td>After hot-plate, heat sinks for 1 min.</td>
</tr>
<tr>
<td></td>
<td>1.5</td>
<td>Exposure</td>
<td>N/A</td>
<td>MA4</td>
<td>RT</td>
<td>20 s</td>
<td>Intensity = 0.9mW/cm² for I-line.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td>---</td>
<td>---</td>
<td>---</td>
<td></td>
</tr>
<tr>
<td>1.6</td>
<td>Develop with S1805</td>
<td>MIF319</td>
<td>Beaker</td>
<td>RT</td>
<td>1 min</td>
<td>Rinse with DI-water and dry with N\textsubscript{2}.</td>
<td></td>
</tr>
<tr>
<td>1.7</td>
<td>Post-bake</td>
<td>N/A</td>
<td>Oven</td>
<td>120 °C</td>
<td>30 min</td>
<td>To harden the resist before etch.</td>
<td></td>
</tr>
<tr>
<td>1.8</td>
<td>Ortho-phosphoric etching</td>
<td>H\textsubscript{3}PO\textsubscript{4}:H\textsubscript{2}O\textsubscript{2}:H\textsubscript{2}O (3:1:50) *H\textsubscript{2}O\textsubscript{2} High-grade</td>
<td>Beaker</td>
<td>RT</td>
<td>1 min</td>
<td>Ortho-phosphoric etch rate: 1.~100 nm/min:InGaAs/InAlAs type pHEMT, 2.~80 nm/min: GaAs/InAlAs type pHEMT. *It doesn’t etch InP. *Mesa height = ~100 nm.</td>
<td></td>
</tr>
<tr>
<td>1.9</td>
<td>Side-wall etching</td>
<td>Succinic acid powder (10 g), H\textsubscript{2}O (50 ml), NH\textsubscript{3} (~10 ml to pH of 5.5), H\textsubscript{2}O\textsubscript{2} (5 ml)</td>
<td>pH meter</td>
<td>RT</td>
<td>10 min</td>
<td>Succinic etch rate: 1. InGaAs = 240 Å/min 2. InAlAs = 2 Å /min Etch 50 Å InGaAs layer InGaAs/InAlAs selectivity = 120:1. *Add H\textsubscript{2}O\textsubscript{2} only after pH of 5.5 is achieved by the intermittent addition of ammonia. *Allow the solution to settle for 30 min before etching</td>
<td></td>
</tr>
<tr>
<td><strong>Ohmic Metal</strong></td>
<td>2.1</td>
<td>Sample cleaning</td>
<td>Acetone-IPA</td>
<td>USB</td>
<td>RT</td>
<td>5 min each</td>
<td>Lastly dry the sample with N\textsubscript{2}.</td>
</tr>
<tr>
<td>2.2</td>
<td>Pre-bake</td>
<td>N/A</td>
<td>Hot-plate</td>
<td>&gt;100°C</td>
<td>1 min</td>
<td>To eliminate moisture from the sample. After baking, cool down on the heat sink for 1 min.</td>
<td></td>
</tr>
<tr>
<td>2.3</td>
<td>Resist-coating</td>
<td>Photoresist: AZnLOF 2070 (2 μm grade)</td>
<td>Spinner</td>
<td>RT</td>
<td>1 min</td>
<td>Program-6: (Acc=2000, RPM=3000, Duration=30 s).</td>
<td></td>
</tr>
<tr>
<td>2.4</td>
<td>Edge bead removal (EBR)</td>
<td>Solvent: AZ EBR</td>
<td>Spinner</td>
<td>RT</td>
<td>1 min</td>
<td>Solvent applied on each corner, then spin again with Program-6.</td>
<td></td>
</tr>
<tr>
<td>2.5</td>
<td>Soft-bake</td>
<td>N/A</td>
<td>Hot-plate</td>
<td>110 °C</td>
<td>1 min</td>
<td>After baking, cool-down on the heat sink for 1 min.</td>
<td></td>
</tr>
<tr>
<td>2.6</td>
<td>Exposure</td>
<td>N/A</td>
<td>MA4</td>
<td>RT</td>
<td>5.5 s</td>
<td>Intensity = 0.9mW/cm² for I-line.</td>
<td></td>
</tr>
<tr>
<td>2.7</td>
<td>P-E-B (Post Exposure Bake)</td>
<td>N/A</td>
<td>Hot-plate</td>
<td>110 °C</td>
<td>1 min</td>
<td>After baking, cool-down on the heat sink for 1 min.</td>
<td></td>
</tr>
<tr>
<td>2.8</td>
<td>Develop AZnLOF 2070</td>
<td>MIF326</td>
<td>Beaker</td>
<td>RT</td>
<td>1 min</td>
<td>AZnLOF 2070 (2 μm grade) is a negative resist. The exposed region polymerizes and unexposed region gets dissolved in the developer. Lastly rinse with DI-water and dry with N₂.</td>
<td></td>
</tr>
</tbody>
</table>
2.9  | Loading evaporator with crude materials | AuGe/Au 70 mg/12 cm | JNR | RT | N/A  | Crude Au (plus boats in the same beaker if needed). Pre-cleaned in Trike-Acetone-IPA (5 min each). Then etched in H$_2$O:HCL (15 ml:15 ml) for 2 min to de-oxidize. Lastly cleaned with DI water and dried with N$_2$.  

2.10 | Remove residue via plasma etching | O$_2$ | Plasma-kit | RT | 20 s | Pressure: 60 mTorr, Power = 25 W(100 a.u.), O$_2$ flow: 50 sccm  

2.11 | De-oxidation | HCL:H$_2$O (1:1) | N/A | RT | 30 s | *15 ml : 15 ml  
| | | | | | Put the sample for 30 s and then rinse with DI-water and dries with N$_2$. Load the sample as fast as possible in the evaporator that to delay HCL evaporation.  

2.12 | Evaporation | AuGe/Au 50 nm/100 nm | JNR | N/A | N/A | Load ~70 mg AuGe and 10 cm Au *(Thin ohmic scheme)*  

2.13 | Lift-off | NMP (1165) | 85 °C | > 30 min | Can be left over-night at RT.  

2.14 | Sample cleaning | DI-water | 3 min | | Lastly dry the sample with N$_2$.  

<p>| 208 |</p>
<table>
<thead>
<tr>
<th></th>
<th>Metal Gate</th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>2.15</td>
<td>Annealing</td>
<td>N/A</td>
<td>Furnace</td>
<td>280 °C</td>
<td>90 s</td>
</tr>
<tr>
<td>2.16</td>
<td>TLM measurements</td>
<td>N/A</td>
<td>ICCAP</td>
<td>RT</td>
<td>N/A</td>
</tr>
<tr>
<td>3.1</td>
<td>Sample cleaning</td>
<td>Acetone-IPA</td>
<td>USB (Level 1)</td>
<td>RT</td>
<td>5 min each</td>
</tr>
<tr>
<td>3.2</td>
<td>Pre-bake</td>
<td>N/A</td>
<td>Hot-plate</td>
<td>&gt;100°C</td>
<td>1 min</td>
</tr>
<tr>
<td>3.3</td>
<td>Resist-coating</td>
<td>Photoresist: AZnLOF 2070 (0.5 μm grade)</td>
<td>Spinner</td>
<td>RT</td>
<td>30 s</td>
</tr>
<tr>
<td>3.4</td>
<td>Edge bead removal (EBR)</td>
<td>Solvent: AZ EBR</td>
<td>Spinner</td>
<td>RT</td>
<td>1 min</td>
</tr>
<tr>
<td>3.5</td>
<td>Soft-bake</td>
<td>N/A</td>
<td>Hot-plate</td>
<td>110 °C</td>
<td>1 min</td>
</tr>
<tr>
<td>3.6</td>
<td>Exposure</td>
<td>N/A</td>
<td>MA4</td>
<td>12 s</td>
<td>Intensity = 0.9mW/cm² for I-line. Wedge Error =1.</td>
</tr>
</tbody>
</table>
| 3.7  | **P-E-B**  
(Post Exposure Bake) | N/A | Hot-plate | 110 °C | 1 min | After baking, cool-down on the heat sink for 1 min. |
| 3.8  | Develop AZnLOF 2070 | MIF326 | Beaker | RT | 5 min | Developed in agitator. Rinse with DI-water for 30 s. |
| 3.9  | Loading evaporator with crude materials | Ti/Au/Au  
1.5 cm/15 cm/15 cm | EDWINA | RT | N/A | Crude Au (plus boats in the same beaker if needed). Pre-cleaned in Trike-Acetone-IPA (5 min each). Then etched in H₂O:HCL (15 ml :15 ml) for 2 min to de-oxidize. Lastly cleaned with DI water and dried with N₂. |
| 3.10 | Remove residue via Plasma etching | O₂ | Plasma-kit | RT | 20 s | Pressure : 60 mT, Power= 25W (100 a.u.), O₂ flow: 50 sccm |
| 3.11 | Gate Recess  
(Succinic etching) | Succinic acid powder  
(10 g), H₂O (50 ml), NH₃ (~10 ml to pH of 5.5), H₂O₂ (5 ml) | pH meter | RT | 5 min | Succinic etch rate:  
1. InGaAs = 240 Å/min  
2. InAlAs = 2 Å /min  
Etch 50 Å InGaAs layer  
InGaAs/InAlAs selectivity = 120:1.  
*Add H₂O₂ only after pH of 5.5 is achieved by the intermittent addition of ammonia.  
*Allow the solution to settle for 30 min before |
<table>
<thead>
<tr>
<th>Step</th>
<th>Process</th>
<th>Substrate</th>
<th>Temperature</th>
<th>Time</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.12</td>
<td>Evaporation</td>
<td>Ti/Au 50 nm/450 nm</td>
<td>EDWINA</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>3.13</td>
<td>Lift-off</td>
<td>NMP</td>
<td>USB</td>
<td>85 °C</td>
<td>~ 30 min</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Then rinse with DI-water and dry with N₂.</td>
</tr>
<tr>
<td>3.14</td>
<td>Sample cleaning</td>
<td>DI-water</td>
<td>Beaker</td>
<td>RT</td>
<td>3 min</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Then dry with N₂.</td>
</tr>
<tr>
<td>3.11</td>
<td>Diode Test</td>
<td>N/A</td>
<td>ICCAP</td>
<td>RT</td>
<td>N/A</td>
</tr>
<tr>
<td>4.1</td>
<td>Sample cleaning</td>
<td>Acetone-IPA</td>
<td>USB</td>
<td>RT</td>
<td>5 min each</td>
</tr>
<tr>
<td>4.2</td>
<td>Pre-bake</td>
<td>N/A</td>
<td>Hot-plate</td>
<td>&gt;100°C</td>
<td>1 min</td>
</tr>
</tbody>
</table>

* Load 1.5 cm Titanium (Ti), and 15 cm of Au in each of the two adjacent boats.
** Ti has high barrier height; do not allow Au to diffuse.

Lastly dry the sample with N₂. To eliminate moisture from the sample. After
<table>
<thead>
<tr>
<th>Step</th>
<th>Process</th>
<th>Photoresist</th>
<th>Spin-coater</th>
<th>Temp</th>
<th>Time</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.3</td>
<td>Resist-coating</td>
<td>AZnLOF 2070 (2 μm grade)</td>
<td>Spinner</td>
<td>RT</td>
<td>30 s</td>
<td>Program-6: (Acc=2000, RPM=3000, Duration=30 s)</td>
</tr>
<tr>
<td>4.4</td>
<td>Soft-bake</td>
<td>N/A</td>
<td>Hot-plate</td>
<td>110 °C</td>
<td>1 min</td>
<td>After baking, cool-down on the heat sink for 1 min.</td>
</tr>
<tr>
<td>4.5</td>
<td>Exposure</td>
<td>N/A</td>
<td>MA4</td>
<td>RT</td>
<td>5.5 s</td>
<td>Intensity = 0.9mW/cm² for I-line.</td>
</tr>
<tr>
<td>4.6</td>
<td>P-E-B (Post Exposure Bake)</td>
<td>N/A</td>
<td>Hot-plate</td>
<td>110 °C</td>
<td>1 min</td>
<td>After baking, cool-down on the heat sink for 1 min.</td>
</tr>
<tr>
<td>4.7</td>
<td>Develop AZnLOF 2070</td>
<td>MIF326</td>
<td>Beaker</td>
<td>RT</td>
<td>1 min</td>
<td>AZnLOF 2070 (2 μm grade) is a negative resist. The exposed region polymerizes and unexposed region gets dissolved in the developer. Lastly rinse with DI-water and dry with N₂.</td>
</tr>
<tr>
<td>4.8</td>
<td>Loading evaporator with crude materials</td>
<td>Ti/Au/Au = 1.5 cm/ 15 cm/ 15 cm</td>
<td>EDWINA</td>
<td>N/A</td>
<td>N/A</td>
<td>Crude Au (plus boats in the same beaker if needed). Pre-cleaned in Trike-Acetone-IPA (5 min each). Then etched in H₂O:HCL (15 ml :15 ml) for 2 min to de-oxidize. Lastly cleaned with DI water and dried with N₂.</td>
</tr>
<tr>
<td>4.9</td>
<td>Removal of residue by plasma etching</td>
<td>O₂</td>
<td>Plasma-kit</td>
<td>RT</td>
<td>20 s</td>
<td>Pressure :60 mT, Power= 25W (100 a.u.), O₂ flow: 50 sccm</td>
</tr>
<tr>
<td>-----</td>
<td>------------------------------------</td>
<td>----</td>
<td>------------</td>
<td>----</td>
<td>------</td>
<td>------------------------------------------------------------------</td>
</tr>
<tr>
<td>4.10</td>
<td>Evaporation</td>
<td>Ti/Au = 50 nm/450 nm</td>
<td>EDWINA</td>
<td>N/A</td>
<td>N/A</td>
<td>Load 1.5 cm Ti, and 15 cm of Au in each of the two adjacent boats.</td>
</tr>
<tr>
<td>4.11</td>
<td>Lift-off</td>
<td>NMP</td>
<td>USB</td>
<td>80 °C</td>
<td>~ 30 min</td>
<td>Then rinse with DI-water.</td>
</tr>
<tr>
<td>4.12</td>
<td>Sample cleaning</td>
<td>DI-water</td>
<td>Beaker</td>
<td>RT</td>
<td>3 min</td>
<td>Lastly dry with N₂.</td>
</tr>
<tr>
<td>4.12</td>
<td>Diode Test</td>
<td>N/A</td>
<td>ICCAP</td>
<td>RT</td>
<td>N/A</td>
<td></td>
</tr>
</tbody>
</table>

### Dielectric (SF11) bridge support

<table>
<thead>
<tr>
<th>5.1</th>
<th>Sample cleaning</th>
<th>Acetone-IPA</th>
<th>USB</th>
<th>RT</th>
<th>5 min each</th>
<th>Lastly dry the sample with N₂.</th>
</tr>
</thead>
<tbody>
<tr>
<td>5.2</td>
<td>Pre-bake</td>
<td>N/A</td>
<td>Hot-plate</td>
<td>&gt;100°C</td>
<td>1 min</td>
<td>To eliminate moisture from the sample. After baking, cool down on the heat sink for 1 min.</td>
</tr>
</tbody>
</table>
| 5.3 | Resist-coating  | Photoresist: SF11 | Spinner | RT | 45 s | Program-13 :
(Acc=10000, rpm=500,time=5s),
(Acc=10000, rpm=4000,time=45s),
(Acc=10000, rpm=7000,time=5s). |
<table>
<thead>
<tr>
<th></th>
<th>Process Type</th>
<th>Photoresist/Chemical</th>
<th>Temperature</th>
<th>Duration</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>5.4</td>
<td>Soft-bake</td>
<td>N/A</td>
<td>Hot-plate</td>
<td>190 °C</td>
<td>5 min</td>
</tr>
<tr>
<td>5.5</td>
<td>Resist-coating</td>
<td>Photoresist: S1805</td>
<td>Beaker</td>
<td>RT</td>
<td>30 s</td>
</tr>
<tr>
<td>5.6</td>
<td>Soft-bake</td>
<td>N/A</td>
<td>Hot-plate</td>
<td>115 °C</td>
<td>1 min</td>
</tr>
<tr>
<td>5.7</td>
<td>Exposure</td>
<td>N/A</td>
<td>MA4</td>
<td>RT</td>
<td>18 s</td>
</tr>
<tr>
<td>5.8</td>
<td>Develop S1805</td>
<td>MIF319</td>
<td>Beaker</td>
<td>RT</td>
<td>1 min</td>
</tr>
</tbody>
</table>
| 5.9 | DUV (Deep UV) | N/A | UV EPROM eraser | RT | 15 min | *Deep Ultraviolet Flooding.*  
- To make sure SF11 reacts to XP101A |
<p>| 5.10 | Develop SF11 | XP101A | Beaker | RT | 3 min | Observe visually see the colour, changed to bright grey of the exposed area. Then rinse the sample with DI-water. |
| 5.11 | Sample cleaning | Acetone-IPA | USB | RT | 5 min each | Lastly dry the sample with N₂. |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>5.12</td>
<td>Hard-reflow</td>
<td>N/A</td>
<td>Hot-plate</td>
<td>200 °C</td>
<td>10 min</td>
<td>Reflow rate = 0.17 μm / min.</td>
</tr>
<tr>
<td>6.1</td>
<td>Resist-coating</td>
<td>Photoresist: S1813</td>
<td>Spinner</td>
<td>RT</td>
<td>30 s</td>
<td>Program-4 : (Acc=2000, rpm=4000, time=30 s)</td>
</tr>
<tr>
<td>6.2</td>
<td>Soft-bake</td>
<td>N/A</td>
<td>Hot-plate</td>
<td>115 °C</td>
<td>1 min</td>
<td>After baking, cool-down on the heat sink for 1 min.</td>
</tr>
<tr>
<td>6.3</td>
<td>Exposure</td>
<td>N/A</td>
<td>MA4</td>
<td>RT</td>
<td>40 s</td>
<td>Intensity= 6 mW/cm². Dielectric bridge mask.</td>
</tr>
<tr>
<td>6.4</td>
<td>Develop S1813</td>
<td>MicroDev : H₂O = 1:1</td>
<td>Beaker</td>
<td>RT</td>
<td>1 min 30 s</td>
<td></td>
</tr>
<tr>
<td>6.5</td>
<td>Evaporation</td>
<td>Au = 500 nm</td>
<td>EDWINA then JNR</td>
<td>N/A</td>
<td>N/A</td>
<td>Load 15cm Au.</td>
</tr>
<tr>
<td>6.6</td>
<td>Lift-off</td>
<td>Acetone-IPA only</td>
<td>NO HEAT</td>
<td>RT</td>
<td>~ 30 min</td>
<td>Then rinse with DI-water.</td>
</tr>
</tbody>
</table>
APPENDIX B :

SUB-\( \mu \text{M} \) pHEMT T-GATE FABRICATION PROCESS FLOW

<table>
<thead>
<tr>
<th>Structure name</th>
<th>Step</th>
<th>Step-name</th>
<th>Chemical / Solvent</th>
<th>Equipment / Machine</th>
<th>Temp ( (^\circ C) )</th>
<th>Time</th>
<th>Comments / Highlights</th>
</tr>
</thead>
<tbody>
<tr>
<td>MESA / Isolation</td>
<td>1.1</td>
<td>Sample preparation / cleaning</td>
<td>NMP(1165)-Acetone-IPA</td>
<td>USB</td>
<td>RT</td>
<td>5 min each</td>
<td>Lastly dry the sample with ( \text{N}_2 )</td>
</tr>
<tr>
<td></td>
<td>1.2</td>
<td>Pre-heat</td>
<td>N/A</td>
<td>Hot-plate</td>
<td>120 °C</td>
<td>1 min</td>
<td>After baking, cool-down on the heat sink for 1 min.</td>
</tr>
<tr>
<td></td>
<td>1.3</td>
<td>Resist-coating</td>
<td>Photoresist: S1805</td>
<td>Spinner</td>
<td>RT</td>
<td>30 s</td>
<td>Program-4: (Acc=2000, RPM=4000, Duration=30 s)</td>
</tr>
<tr>
<td></td>
<td>1.4</td>
<td>Soft-bake</td>
<td>N/A</td>
<td>Hot-plate</td>
<td>115 °C</td>
<td>1 min</td>
<td>After hot-plate, heat sinks for 1 min.</td>
</tr>
<tr>
<td></td>
<td>1.5</td>
<td>Exposure</td>
<td>N/A</td>
<td>MA4</td>
<td>RT</td>
<td>20 s</td>
<td>Intensity=0.9 mW/cm(^2) for I-line.</td>
</tr>
<tr>
<td></td>
<td>1.6</td>
<td>Develop S1805</td>
<td>MIF319</td>
<td>Agitator &amp; beaker</td>
<td>RT</td>
<td>1 min</td>
<td>Then rinse with DI-water and dry with N₂.</td>
</tr>
<tr>
<td>---</td>
<td>-----</td>
<td>----------------</td>
<td>--------</td>
<td>--------------------</td>
<td>----</td>
<td>-------</td>
<td>------------------------------------------</td>
</tr>
<tr>
<td></td>
<td>1.7</td>
<td>Post-bake</td>
<td>N/A</td>
<td>Oven</td>
<td>120 °C</td>
<td>30 min</td>
<td>To harden the resist before etch.</td>
</tr>
<tr>
<td></td>
<td>1.8</td>
<td>Ortho-phosphoric etching</td>
<td>H₃PO₄:H₂O₂:H₂O (3:1:50)</td>
<td>Agitator &amp; beaker</td>
<td>RT</td>
<td>1 min</td>
<td>Ortho-phosphoric etch rate: 1. ~100 nm/min: InGaAs/InAlAs type pHEMT. 2. ~80 nm/min: GaAs/InAlAs type pHEMT. *It doesn’t etch InP. *Mesa height = ~100 nm.</td>
</tr>
<tr>
<td></td>
<td>1.9</td>
<td>Side-wall etching</td>
<td>Succinic acid powder (10 g), H₂O (50 ml), NH₃ (~10 ml to pH of 5.5), H₂O₂ (5 ml)</td>
<td>pH meter</td>
<td>RT</td>
<td>10 min</td>
<td>Succinic etch rate: 1. InGaAs = 240 Å/min 2. InAlAs = 2 Å/min Etch 50 Å InGaAs layer InGaAs/InAlAs selectivity = 120:1. *Add H₂O₂ only after pH of 5.5 is achieved by the intermittent addition of ammonia. *Allow the solution to settle for 30 min before etching</td>
</tr>
<tr>
<td>Ohmic Metal</td>
<td>2.1</td>
<td>Sample cleaning</td>
<td>Acetone-IPA</td>
<td>USB (Level 1)</td>
<td>RT</td>
<td>5 min each</td>
<td>Then dry with N₂</td>
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<tr>
<td>Step</td>
<td>Description</td>
<td>Temperature</td>
<td>Time</td>
<td>Notes</td>
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<tr>
<td>2.2</td>
<td>Pre-bake</td>
<td>N/A</td>
<td>&gt;100°C</td>
<td>1 min</td>
<td>To eliminate moisture from the sample. After baking, cool down on the heat sink for 1 min.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2.3</td>
<td>Resist-coating</td>
<td>Photoresist: AZnLOF 2070 (2 μm grade)</td>
<td>Spinner</td>
<td>RT</td>
<td>1 min</td>
<td>Program-6: (Acc=2000, RPM=3000, Duration=30 s)</td>
<td></td>
</tr>
<tr>
<td>2.4</td>
<td>Edge bead removal(EBR)</td>
<td>Solvent: AZ EBR</td>
<td>Spinner</td>
<td>RT</td>
<td>1 min</td>
<td>Solvent applied on each corner, then spin again with Program-6.</td>
<td></td>
</tr>
<tr>
<td>2.5</td>
<td>Soft-bake</td>
<td>N/A</td>
<td>110 °C</td>
<td>1 min</td>
<td>After baking, cool-down on the heat sink for 1 min.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2.6</td>
<td>Exposure</td>
<td>N/A</td>
<td>MA4</td>
<td>RT</td>
<td>5.5 s</td>
<td>Intensity=0.9 mW/cm² for I-line.</td>
<td></td>
</tr>
<tr>
<td>2.7</td>
<td>P-E-B (Post Exposure Bake)</td>
<td>N/A</td>
<td>Hot-plate</td>
<td>110 °C</td>
<td>1 min</td>
<td>After baking, cool-down on the heat sink for 1 min.</td>
<td></td>
</tr>
<tr>
<td>2.8</td>
<td>Develop AZnLOF 2070</td>
<td>MIF326</td>
<td>Agitator &amp; beaker</td>
<td>RT</td>
<td>1 min</td>
<td>AZnLOF 2070 (2 μm grade) is a negative resist. The exposed region polymerizes and unexposed region gets dissolved in the developer. Lastly rinse with DI-water and dry with N₂.</td>
<td></td>
</tr>
<tr>
<td>Step</td>
<td>Description</td>
<td>Material</td>
<td>Method</td>
<td>Temperature</td>
<td>Time</td>
<td>Notes</td>
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</tr>
<tr>
<td>2.9</td>
<td>Loading evaporator with crude materials</td>
<td>AuGe/Au 70 mg/12 cm</td>
<td>JNR</td>
<td>RT</td>
<td>N/A</td>
<td>Crude Au (plus boats in the same beaker if needed). Pre-cleaned in Trike-Acetone-IPA (5 min each). Then etched in H₂O: HCL (15 ml :15 ml) for 2 min to de-oxidize. Lastly cleaned with DI water and dried with N₂.</td>
<td></td>
</tr>
<tr>
<td>2.10</td>
<td>Remove residue via plasma etching</td>
<td>O₂</td>
<td>Plasma-kit</td>
<td>RT</td>
<td>20 s</td>
<td>Pressure: 60 mTorr, Power= 25 W(100 a.u.), O₂ flow: 50 sccm.</td>
<td></td>
</tr>
<tr>
<td>2.11</td>
<td>De-oxidation</td>
<td>HCL:H₂O (1:1)</td>
<td>N/A</td>
<td>RT</td>
<td>30 s</td>
<td>*15 ml : 15 ml *Put the sample for 30 s and then rinse with DI-water and dries with N₂. Load the sample as fast as possible in the evaporator that to delay HCL evaporation.</td>
<td></td>
</tr>
<tr>
<td>2.12</td>
<td>Evaporation</td>
<td>AuGe/Au 50 nm / 100 nm</td>
<td>JNR</td>
<td>N/A</td>
<td>N/A</td>
<td>Load ~70 mg AuGe and 10 cm Au <em>(Thin ohmic scheme).</em></td>
<td></td>
</tr>
<tr>
<td>2.13</td>
<td>Lift-off</td>
<td>Hot NMP then DI-water</td>
<td>Hot-plate</td>
<td>85 °C</td>
<td>&gt; 30 min</td>
<td>Can be left over-night at RT.</td>
<td></td>
</tr>
<tr>
<td>2.14</td>
<td>Annealing</td>
<td>N/A</td>
<td>Furnace</td>
<td>280 °C</td>
<td>90 s</td>
<td>N₂ flow: 150 (N₂ at 30 is idle), Rc = ~0.1Ω/mm.</td>
<td></td>
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<tr>
<td></td>
<td>Bottom Gate Foot Print</td>
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</tr>
<tr>
<td>2.15</td>
<td>TLM measurements</td>
<td>N/A</td>
<td>ICCAP</td>
<td>RT</td>
<td>N/A</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>File: Constant current (I = 1 mA)</td>
<td></td>
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</tr>
<tr>
<td>3.1</td>
<td>Sample cleaning</td>
<td>Hot NMP then DI-water</td>
<td>Agitator &amp; beaker</td>
<td>85 °C</td>
<td>15 min</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Immerse in hot NMP first, then clean with DI-water. Avoid USB.</td>
<td></td>
<td></td>
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</tr>
<tr>
<td>3.2</td>
<td>Pre-bake</td>
<td>N/A</td>
<td>Hot-plate</td>
<td>&gt;100°C</td>
<td>1 min</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>To eliminate moisture from the sample. After baking, cool down on the heat sink for 1 min.</td>
<td></td>
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</tr>
<tr>
<td>3.3</td>
<td>Silicon Nitride (Si$_3$N$_4$) deposition</td>
<td>Si$_3$N$_4$ = 200 nm</td>
<td>PECVD</td>
<td>250 °C</td>
<td>30 min</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3.4</td>
<td>Sample cleaning</td>
<td>Hot NMP then DI-water</td>
<td>Agitator &amp; beaker</td>
<td>85 °C</td>
<td>15 min</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Immerse in hot NMP first, then clean with DI-water. Avoid using USB.</td>
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</tr>
<tr>
<td>3.5</td>
<td>Resist-coating</td>
<td>Photoresist: S1805</td>
<td>Spinner</td>
<td>RT</td>
<td>30 s</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Program-4: (Acc=2000, RPM=4000, Duration=30 s)</td>
<td></td>
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</tr>
<tr>
<td>3.6</td>
<td>Soft-bake</td>
<td>N/A</td>
<td>Hot-plate</td>
<td>115 °C</td>
<td>1 min</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>After hot-plate, then heat sinks for 1 min.</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td></td>
<td>Bottom Gate foot print exposure</td>
<td>N/A</td>
<td>MA4</td>
<td>RT</td>
<td>20 s</td>
<td>Defining 1 μm gate footprint/opening.</td>
<td></td>
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</tr>
<tr>
<td>3.7</td>
<td>Develop S1805</td>
<td>MIF319</td>
<td>Beaker</td>
<td>RT</td>
<td>1 min</td>
<td>Lastly rinse with DI-water and dry with N₂.</td>
<td></td>
</tr>
<tr>
<td>3.8</td>
<td>Soft-reflow</td>
<td>NMP</td>
<td>Reflow chamber (New design)</td>
<td>&lt; 50 °C</td>
<td>Variable</td>
<td>Soft reflow process, size varies with reflow time.</td>
<td></td>
</tr>
<tr>
<td>3.9</td>
<td>Pattern transfer</td>
<td>CF₄</td>
<td>Plasma-kit</td>
<td>RT</td>
<td>6 min</td>
<td>Pressure: 20 mTorr (Fully open mechanical valve), Power = 20 W (90 a.u.), CF₄ flow: 40 sccm. *Etch time varies with Si₃N₄ thickness.</td>
<td></td>
</tr>
<tr>
<td>3.10</td>
<td>Remove residue via plasma etching</td>
<td>O₂</td>
<td>Plasma-kit</td>
<td>RT</td>
<td>20 s</td>
<td>Pressure: 60 mTorr, Power= 20 W(90 a.u.), O₂ flow: 50 sccm.</td>
<td></td>
</tr>
<tr>
<td>3.11</td>
<td>Sample cleaning</td>
<td>Hot NMP then DI-water</td>
<td>Agitator &amp; beaker</td>
<td>85 °C</td>
<td>15 min</td>
<td>Immerse in hot NMP first, then clean with DI-water. Avoid USB.</td>
<td></td>
</tr>
<tr>
<td>4.1</td>
<td>Pre-bake</td>
<td>N/A</td>
<td>Hot-plate</td>
<td>&gt;100°C</td>
<td>1 min</td>
<td>To eliminate moisture from the sample. After baking, cool down on the heat sink for 1 min.</td>
<td></td>
</tr>
<tr>
<td>Step</td>
<td>Process Description</td>
<td>Photoresist: AZnLOF 2070 (0.5 μm grade)</td>
<td>Equipment</td>
<td>Temperature</td>
<td>Time</td>
<td>Program Details</td>
<td></td>
</tr>
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<td>--------------------------------------------------------------------------------</td>
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</tr>
<tr>
<td>4.3</td>
<td>Resist-coating</td>
<td>Photoresist: AZnLOF 2070 (0.5 μm grade)</td>
<td>Spinner</td>
<td>RT</td>
<td>30 s</td>
<td>Program-6: (Acc=2000, RPM=3000, Duration=30s)</td>
<td></td>
</tr>
<tr>
<td>4.4</td>
<td>Edge bead removal (EBR)</td>
<td>Solvent: AZ EBR</td>
<td>Spinner</td>
<td>RT</td>
<td>1 min</td>
<td>Solvent applied on each corner, then spin again with Program-6.</td>
<td></td>
</tr>
<tr>
<td>4.5</td>
<td>Soft-bake</td>
<td>N/A</td>
<td>Hot-plate</td>
<td>110 °C</td>
<td>1 min</td>
<td>After baking, cool-down on the heat sink for 1 min.</td>
<td></td>
</tr>
<tr>
<td>4.6</td>
<td>Exposure</td>
<td>N/A</td>
<td>MA4</td>
<td>RT</td>
<td>12 s</td>
<td>Definition of 1 μm top gate. Intensity= 0.9mW/cm² for I-line. Wedge Error =1.</td>
<td></td>
</tr>
<tr>
<td>4.7</td>
<td>P-E-B (Post Exposure Bake)</td>
<td>N/A</td>
<td>Hot-plate</td>
<td>110 °C</td>
<td>1 min</td>
<td>After baking, cool-down on the heat sink for 1 min.</td>
<td></td>
</tr>
<tr>
<td>4.8</td>
<td>Develop AZ nLOF 2070</td>
<td>MIF326</td>
<td>Agitator &amp; beaker</td>
<td>RT</td>
<td>5 min</td>
<td>Developed in agitator. Rinse with DI-water for 30 s.</td>
<td></td>
</tr>
<tr>
<td>4.9</td>
<td>Loading evaporator with crude materials</td>
<td>Ti/Au/Au 1.5 cm/15 cm/15 cm</td>
<td>EDWINA</td>
<td>RT</td>
<td>N/A</td>
<td>Crude Au (plus boats in the same beaker if needed). Pre-cleaned in Trike-Acetone-IPA (5 min each). Then etched in H₂O:HCL (15 ml :15 ml) for 2 min to de-oxidize. Lastly cleaned with DI water and dried with N₂.</td>
<td></td>
</tr>
<tr>
<td>Step</td>
<td>Process Description</td>
<td>Reactants</td>
<td>Equipment</td>
<td>Temperature</td>
<td>Time</td>
<td>Notes</td>
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<td>----------------------------------------------------------------------</td>
<td></td>
</tr>
<tr>
<td>4.10</td>
<td>Remove residue via plasma etching</td>
<td>$O_2$</td>
<td>Plasma-kit</td>
<td>RT</td>
<td>20 s</td>
<td>Pressure: 60 mT, Power= 25 W (100 a.u.), $O_2$ flow: 50 sccm.</td>
<td></td>
</tr>
<tr>
<td>4.11</td>
<td>Gate Recess (Succinic etching)</td>
<td>Succinic acid powder (10 g), $H_2O$ (50 ml), $NH_3$ (~10 ml to pH of 5.5), $H_2O_2$ (5 ml)</td>
<td>pH meter</td>
<td>RT</td>
<td>5 min</td>
<td>Succinic etch rate: 1. InGaAs = 240 Å/min 2. InAlAs = 2 Å/min Etch 50 Å InGaAs layer InGaAs/InAlAs selectivity = 120:1. *Add $H_2O_2$ only after pH of 5.5 is achieved by the intermittent addition of ammonia. *Allow the solution to settle for 30 min before etching</td>
<td></td>
</tr>
<tr>
<td>4.12</td>
<td>Evaporation</td>
<td>Ti/Au 50 nm /450 nm</td>
<td>EDWINA</td>
<td>N/A</td>
<td>N/A</td>
<td>* Load 1.5 cm Ti, and 15 cm of Au in each of the two adjacent boats.</td>
<td></td>
</tr>
<tr>
<td>4.13</td>
<td>Lift-off</td>
<td>Hot NMP then DI-water</td>
<td>Agitator &amp; beaker</td>
<td>85 ºC</td>
<td>~ 30 min</td>
<td>Lastly rinse with DI-water and dry with $N_2$. Avoid USB.</td>
<td></td>
</tr>
<tr>
<td>4.14</td>
<td>Diode Test</td>
<td>N/A</td>
<td>ICCAP</td>
<td>RT</td>
<td>N/A</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>