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Thermally Evaporated SiO Serving as Gate Dielectric in Graphene Field-Effect Transistors

Letao Yang, Hanbin Wang, Xijian Zhang, Yuxiang Li, Xian Zhao and Aimin Song, *Senior Member, IEEE*

Abstract—A thermally evaporated silicon monoxide (SiO) film has been experimented as the gate dielectric in graphene field-effect transistors (GFETs) due to its room-temperature and low-damage deposition without introducing chemical gases or ionized particles as in other film deposition techniques which may cause damage to graphene. In order to evaluate the dielectric properties, a double-gated GFET was fabricated with a standard commercial thermally grown SiO₂ layer as the bottom gate dielectric and thermally evaporated SiO as the top dielectric. The electrical characterizations revealed that the top-gate carrier mobility was 1,081.3 cm²/Vs, reasonably comparable to the bottom-gate mobility. Furthermore, the breakdown strength of the SiO film reached 5.7 MV/cm, which was lower than that of the SiO₂ dielectric (~10 MV/cm) but in the same order of magnitude. The breakdown mechanism of the SiO film was studied, and the current-voltage characteristics were in agreement with the Frenkel-Poole emission model. Finally, the relative dielectric constant of SiO was found to be 5.3, significantly higher than that of SiO₂ (3.9). These results indicate that the thermally evaporated SiO can function as an excellent dielectric for graphene-based devices.

Index Terms—Gate dielectric, graphene field-effect transistor (GFET), silicon monoxide (SiO), thermal evaporation.

I. INTRODUCTION

GRAPHENE is a two-dimensional (2D) material of carbon atoms. It has many unique properties, such as high intrinsic carrier mobility ($> 200,000 \text{ cm}^2/\text{Vs}$), high saturation carrier velocity ($\sim 4 \times 10^7 \text{ cm/s}$), and field-effect modulation of the carrier density by two orders of magnitude [1]. Graphene field-effect transistor (GFET) [2], [3] has been intensively studied as the basic building blocks in graphene-based electronic circuits [4], [5]. The gate dielectric plays an important role in any GFET because graphene is extremely sensitive to interface properties. Thermally grown silicon dioxide (SiO₂) on highly doped silicon substrate has been

widely used as a gate dielectric for the ease of lithography [6]. However, this limits the device structure to bottom-gate GFET, and the common bottom gate hinders fabrication of circuits that consist of multiple GFETs. Deposited dielectrics can overcome the above limitations. However, being atomically thin, graphene is known to be not only extremely sensitive to the dielectric interface properties [7] but also any possible damage during the deposition process of the dielectrics [8], [10]–[12]. Both physical-vapor deposition (PVD) and atomic-layer deposition (ALD) techniques have been used to deposit dielectrics on graphene. PVD methods, such as electron-beam evaporation [13] and radio frequency sputtering [14], have been reported to introduce a large number of lattice defects in graphene. ALD technique has been known to be capable of producing high-quality dielectrics films on graphene but a chemical pre-treatment is necessary [15]–[17]. In comparison to electron-beam evaporation, thermal evaporation process does not require a high-energy electron beam which generates X-ray radiation when it hits the target [18]. Very recently, thermally evaporated silicon monoxide (SiO) has been experimented, and the analysis of Raman spectroscopy indicated little damage to graphene film [18]. Despite the evidence of the optical experiment, to the best of our knowledge, no GFETs have yet been made to determine any possible effects to the electrical properties of graphene.

In this work, GFETs with SiO dielectric deposited by thermal evaporation are fabricated. By analyzing the results of the electrical characterizations, we show that the carrier mobility of bottom-gate GFET has little change after the deposition of SiO on top of the graphene film. By further fabricating of a top gate on SiO, a double-gated GFET is formed. Very similar mobility values are achieved when the GFET are operated by the bottom gate and the top gate. In addition, metal-insulator-metal (MIM) devices are fabricated, revealing that the SiO film has a high breakdown strength and a high relative dielectric constant. These results demonstrate that the thermal evaporation technique is a low-damage deposition method to graphene, and thermally evaporated SiO could function as a suitable dielectric with little degradation to graphene properties.

II. EXPERIMENTAL DETAILS

The graphene samples were purchased from Nanjing XFNANO Materials Tech Co. Ltd. The graphene films were grown on Cu foils by chemical vapor deposition method. They were transferred onto a heavily doped silicon substrate with a 300-nm-thick thermally grown SiO₂ layer. GFET was fabricated using a conventional photolithography process. First,

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a metal stack of Ti/Au (5 nm/60 nm) was deposited by electron-beam evaporation and patterned by a liftoff process to form source and drain contacts. Second, an O₂ plasma etching process was used to define the geometry of the channel regions. Third, a SiO dielectric layer of 30 nm thickness was deposited onto the entire sample surface by thermally evaporating (Auto 306, HHV Inc.) SiO powders (99.95%, Zhongnuo Advanced Material Technology Co. Ltd.) under a vacuum pressure of 5.0×10^{-6} Torr. The evaporation rate was 1 Å/s and the substrate was not heated intentionally. In order to expose the source and drain contacts, the SiO film on the metal pads was etched by a CHF₃/Ar plasma. Finally, the top-gate gate stack of Ti/Au (5 nm/60 nm) was deposited by electron-beam evaporation and patterned by photolithography. In the case of the MIM structures, the two Ti metal layers films were deposited via electron-beam evaporation to sandwich the thermally evaporated SiO film. The electrical properties of the GFET and the MIM devices were characterized using an Agilent B2902A Precision Source/Measure Unit in ambient air at room temperature. The capacitance of the MIM devices was measured using an Agilent E4980A Precision LCR Meter.

III. RESULTS AND DISCUSSION

We first examined the impact of thermally evaporated SiO film to graphene. This was achieved by characterizing the transport properties of a bottom-gated GFET before and after the deposition of a SiO layer (schematics shown in the insets of Fig. 1(a)). Both transfer curves of the GFETs at a source-drain voltage ($V_{DS} = 0.1$ V) with and without SiO exhibited p-type characteristics, which might be induced by the adsorbed substances on the graphene surface from the ambient environment and the residues during the device fabrication process [19]. The decrease in the source-drain current, I_{DS} , after the deposition of SiO could be a results of multiple mechanisms including a reduction of carrier mobility and a reduction of carrier concentration which in the case of graphene corresponds to a shift of Dirac point. To determine the any possible change in mobility, we extracted the corresponding transconductance (g_m) curves of the two bottom-gated GFETs as shown in Figure 1(b). Somewhat surprisingly, the maximum $|g_m|$ increased from 1.93 to 1.98 μ S after coating SiO. Considering the following relationship between the carrier mobility and transconductance [19]:

$$\mu = \frac{L_{ch} |g_m|}{W_{ch} C_{ox} V_{DS}} \quad (1)$$

where L_{ch} and W_{ch} are the channel's length and width, respectively, C_{ox} is the capacitance per square centimeter of 300 nm SiO₂, the corresponding maximum carrier mobility actually increased from 1175 to 1205 cm²/V·s after the SiO deposition. This increase could be a result of passivation of graphene surface from ambient oxygen and water molecules. It is noted that at most gate voltages, the transconductance after SiO deposition is reduced as shown in Fig. 1(b). This could be due to a shift in the Dirac point caused by the passivation. The above results at least suggest that the thermally evaporated SiO did not induce obvious degradation on the quality of graphene.

Fig. 1. (a) Transfer characteristics of a bottom-gated GFET before (red) and after (blue) depositing SiO on the graphene channel. The source-drain voltage V_{DS} was 0.1 V. Right and left insets are the schematics of the GFET before and after SiO deposition, respectively. The channel length L_{ch} was 7 μ m and channel width W_{ch} was 10 μ m. (b) Transconductances ($|g_m|$) versus the bottom-gate voltage (V_{BG}).

To explore the possibility of using thermally evaporated SiO as a low-damage gate dielectric for GFET, MIM devices consisting of 30-nm-thick SiO between two Ti electrodes were fabricated, as shown in the bottom right inset of Fig. 2, in order to determine the breakdown strength (E_{BD}) and the relative dielectric constant. The active area of the MIM device was 0.01 mm². Fig. 2 shows the current density (J) versus the electric field strength (E), in which $E_{BD} = 5.7$ MV/cm can be determined. This is lower than the electrical breakdown strength of thermally grown SiO₂ (10 MV/cm), but is higher than typical Al₂O₃ and HfO₂ films deposited by ALD [20]–[23]. Below the breakdown at 5.7 MV/cm, $\ln(J/E)$ has been found to be fairly linearly dependent on $E^{1/2}$ as shown in the upper left inset in Fig. 2. This implies the dominated conduction mechanism just before electrical breakdown is Frenkel-Poole emission [24], which is common in the vacuum evaporated SiO films [25], [26]. The capacitance of the MIM device was measured at 100 kHz. Based on the capacitance value, 15.7 pF, and the thickness of SiO, the relative dielectric constant of the SiO film can be determined to be approximately 5.3. This is lower than those of high-k dielectrics but much higher than that of SiO₂, 3.9.

Fig. 2. Current density versus electric field strength (J - E) curve of a MIM device consisting of a 30-nm-thick thermally evaporated SiO. The upper left and lower right insets are the corresponding $\ln(J/E)$ - $E^{1/2}$ curve and the schematic of the MIM device, respectively.

Given the excellent breakdown strength of SiO and fairly large relative dielectric constant, a top-gated GFET was fabricated by simply adding a metal electrode on top of the SiO layer in the structure shown in the bottom left inset of Fig. 1(a). This results in a double-gated transistor structure, in which graphene film can be field modulated by both the top gate and bottom gate separately as shown in the inset of Fig. 3(a). The top gate length L_{TG} was 3 μm and gate width W_{TG} was 10 μm .

Fig. 3(a) shows I_{DS} versus V_{DS} curves at different top-gate voltages (V_{TG}) of -2, 0, 2, 4, and 6 V while fixing V_{BG} at 0 V. The absence of the drain-current saturation is due to the zero-bandgap nature of graphene. Fig. 3(b) shows the transfer characteristic (the black curve), I_{DS} versus V_{TG} under $V_{DS} = 0.1$ V and $V_{BG} = 0$ V. Thanks to the very thin SiO dielectric, the GFET can now operate at a low voltage, approximately one order of magnitude lower than that using the bottom gate where the Dirac point could not be reached even by applying +60 V as in Fig. 1(a). A well defined ambipolar conduction around Dirac point voltage was obtained at $V_{TG, \text{Dirac}} = 5.3$ V. The top-gate leakage current I_{GS} was below 40 pA throughout the measurement as shown in the inset of Fig. 3(b), which is comparable to the leakage of the bottom gate (below 90 pA). This is about six orders of magnitude lower than that of the source-drain current, despite a dielectric thickness of only 30 nm, and is hence negligible in the measurement.

Having the double-gated GFET, it is possible to also extract the gate relative dielectric constant of SiO and compare it with the value obtained in the capacitance measurement of the MIM device. Fig. 3(c) displays the top-gate Dirac voltage shifts as a function of V_{BG} , showing a quite linear modulation on the Dirac voltage via bottom-gate voltage. The slope of the fitting line gives the ratio of the top-gate capacitance and the bottom-gate capacitance (C_{TG}/C_{BG}) [8], [27] which is approximately 13.99. Using $C_{BG} = 11.5$ nF/cm², we estimate $C_{TG} = 160.9$ nF/cm², corresponding to a relative dielectric constant of SiO of 5.4,

Fig. 3. (a) Output characteristics of a top-gated GFET under different top-gate voltage. The inset shows a schematic of the top-gated GFET. (b) Transfer characteristic of the top-gated GFET under $V_{DS} = 0.1$ V. The top-gate leakage current is shown in the inset. (c) Top-gate Dirac voltage versus bottom-gate voltage. The black squares are the experimental data and the red line is a linear fitting of the data, indicating a linear modulation on the Dirac voltage via bottom-gate voltage. (d) Experimental (open square) and model fitting (red line) of total resistance (R_{total}) versus $(V_{TG} - V_{TG, \text{Dirac}})$

which is consistent with the value obtained from the MIM device.

Because the top gate only modulates a part of the graphene channel, it is not possible to use (1) to determine the carrier mobility using the transfer characteristic in Fig. 3(b). The total resistance measured between source and drain can be expressed by

$$R_{\text{total}} = 2R_c + \frac{L_{\text{TG}}}{W_{\text{TG}} e \mu \sqrt{n_0^2 + n^2}} \quad (2)$$

where R_c includes the source and drain contact resistance plus the resistance of ungated graphene channel (between the top gate and the source or drain electrode), n_0 is the residual carrier concentration at the Dirac point, and n is the carrier concentration induced by the top gate [15]. The value of n can be obtained from

$$V_{\text{TG}} - V_{\text{TG,Dirac}} = \frac{en}{C_{\text{TG}}} \quad (3)$$

Note that the quantum capacitance is neglected here because its value is approximately $2 \mu\text{F}/\text{cm}^2$, much larger than C_{TG} [28], [29]. By fitting the experimental data with this model, the relevant parameters, n_0 , μ , and R_c can be extracted. Fig. 3(d) shows the measured R_{total} (open square) versus $(V_{\text{TG}} - V_{\text{TG,Dirac}})$, and the fitting curve (red line) derived from (2) and (3). The extracted parameters are $n_0 = 9.0 \times 10^{11} \text{ cm}^{-2}$, $R_c = 573.8 \Omega$, and $\mu = 1081.3 \text{ cm}^2/\text{Vs}$, respectively. The mobility value is comparable to bottom-gate mobility. It is much higher than that of the GFET with an electron-beam evaporated top-gate dielectric SiO_2 ($710 \text{ cm}^2/\text{Vs}$) [30], which may be due to degradation of the graphene channel caused by the a few keV X-ray radiation emitted during the SiO_2 deposition process [18], [30].

IV. CONCLUSIONS

Thermally evaporated SiO has been used, to the best of our knowledge for the first time, as gate dielectric in graphene field-effect transistors. Different device structures have been fabricated to characterize the electrical properties of the SiO films. Little damage to the graphene has been found in the experiment and the achieved carrier mobility is comparable to that obtained using commercial thermally grown SiO_2 . The dielectric breakdown strength is shown to be higher than typically used Al_2O_3 and HfO_2 dielectrics grown by atomic-layer deposition technique. Even with a 30-nm-thin SiO gate dielectric, the gate leakage current was found to be six orders of magnitude lower than the source-drain current. The results demonstrate that SiO is a reliable, low-damage dielectric for fragile graphene films. It is possible that thermally evaporated SiO may find useful applications in devices based other novel 2D materials.

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Fig. 1. (a) Transfer characteristics of a bottom-gated GFET before (red) and after (blue) depositing SiO on the graphene channel. The source-drain voltage V_{DS} was 0.1 V. Right and left insets are the schematics of the GFET before and after SiO deposition, respectively. The channel length L_{ch} was 7 μm and channel width W_{ch} was 10 μm . (b) Transconductances ($|g_m|$) versus the bottom-gate voltage (V_{BG}).

Fig. 1

109x134mm (300 x 300 DPI)

Fig. 2. Current density versus electric field strength (J-E) curve of a MIM device consisting of a 30-nm-thick thermally evaporated SiO. The upper left and lower right insets are the corresponding $\ln(J/E)$ - $E^{1/2}$ curve and the schematic of the MIM device, respectively.

Fig. 2
65x48mm (300 x 300 DPI)

Fig. 3. (a) Output characteristics of a top-gated GFET under different top-gate voltage. The inset shows a schematic of the top-gated GFET. (b) Transfer characteristic of the top-gated GFET under $V_{DS} = 0.1$ V. The top-gate leakage current is shown in the inset. (c) Top-gate Dirac voltage versus bottom-gate voltage. The black squares are the experimental data and the red line is a linear fitting of the data, indicating a linear modulation on the Dirac voltage via bottom-gate voltage. (d) Experimental (open square) and model fitting (red line) of total resistance (R_{total}) versus $(V_{TG} - V_{TG,Dirac})$

Fig. 3

110x82mm (300 x 300 DPI)