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Effects of Substrate and Anode Metal Annealing on InGaZnO Schottky Diodes

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By studying different annealing effects of substrate and anode metal, high-performance Schottky diodes based on InGaZnO (IGZO) film have been realized. It is observed that a suitable thermal annealing of the SiO₂/Si substrate significantly improves the diode performance. In contrary, annealing of the Pd anode increases surface roughness, leading to degradation in the diode performance. As such, by only annealing the substrate but not the anode, we are able to achieve an extremely high rectification ratio of 7.2×10^7 , a large barrier height of 0.88 eV, and a near unity ideality factor of 1.09. The diodes exhibit the highest performance amongst IGZO-based Schottky diodes reported to date where IGZO layer is not annealed. The capacitance vs. voltage measurements indicate that the surface roughness is correlated with the trap state density at the Schottky interface.

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Amorphous oxide semiconductors represented by InGaZnO (IGZO) have superior characteristics to amorphous silicon due to their high carrier mobilities, low-temperature deposition, and excellent uniformity owing to their amorphous nature. Most studies on IGZO so far have focused on thin-film transistors (TFTs). TFTs with higher performance than conventional amorphous silicon transistors have been developed^{1,2} after intensive studies and improvements on carrier transport³⁻⁵ and stability.⁶⁻⁸ In contrast, very limited studies have been reported on IGZO-based Schottky diodes. A major challenge is the difficulty in forming stable and ideal Schottky contacts on oxide semiconductors, because the surface of oxide semiconductors is known to be sensitive to device fabrication processes and atmospheric exposure. The limited studies on IGZO Schottky diodes have been focused on achieving large barrier heights, Φ_B ,^{9,10} high rectification ratios, $I_{on/off}$,^{9,11,12} low ideality factors, n ,^{9,10,13} and high-frequency operation.^{11,12,14} So far, thermal annealing at $\sim 200^\circ\text{C}$ has been used in most studies. The best annealed diodes fabricated by using the sputtering technique showed an $I_{on/off}$ of $\sim 10^8$, Φ_B of $\sim 0.9\text{ eV}$, and n of ~ 1.2 .^{11,12} In the case of annealed diode based on an IGZO layer grown by pulsed laser deposition technique, the best ideality factor reached 1.04.⁹ However, thermal annealing at high temperatures is not preferred when fabricating low-cost, flexible diodes on substrates such as polyethylene terephthalate (PET). Recently, we reported as-deposited IGZO diodes on glass substrate that achieved an ideality factor of 1.14.¹⁵ Such an ideality factor is even lower than the value obtained by the annealed devices deposited using similar sputtering techniques mentioned above. It is therefore interesting to study how exactly annealing at different stages of the device fabrication may affect the device performance. So far, thermal annealing of IGZO Schottky diodes was generally performed on the whole device after the final device fabrication step,^{9,12} and in some cases additional annealing was carried out on the IGZO layer itself.^{10,11,13} Here, we first annealed the SiO_2/Si substrate before depositing any diode layer, and observed an improvement in diode performance. In contrast, thermal annealing on the Pd anode produced an adverse effect on the diode performance.

SiO_2/Si wafers were used as the substrates and they were sequentially cleaned in an ultrasonic bath of decon, de-ionized water, acetone, and ethanol and dried by N_2 . A 3-nm-thick Ti layer was deposited on the substrate for adhesion. A 47-nm-thick Pd layer was deposited as anode electrode, and then treated with oxygen plasma (PDC-32G, 10 min) for oxidation and to ensure good oxygen stoichiometry of the contact interface prior to IGZO deposition.^{11,16} **To study the effect of thermal treatment of SiO_2/Si substrate and Pd anode on the device performance, a hotplate (Model p-10, POLISH Co.) was used to anneal the samples in ambient air.** A 100-nm-thick IGZO layer was deposited by radio-frequency (RF) magnetron sputtering at room temperature with an InGaZnO_4 ceramic target ($\text{In}:\text{Ga}:\text{Zn} = 1:1:1$ in atomic ratio, Lesker Co.). The RF sputtering power was 70 W ^{15,17,18} and the mixed gas was argon with 2.5 % oxygen.^{15,17} The working pressure was 3.6 mTorr. Finally, $\text{Ti}(40\text{ nm})/\text{Au}(40\text{ nm})$ was deposited as top ohmic contact with a shadow mask. All the metals were deposited by electron-

beam evaporation. The device configuration is shown in the inset of Fig. 1. The diode active area is $9.5 \times 10^{-4} \text{ cm}^2$. The electrical characteristics of the Schottky diodes were analyzed by current density-voltage (J - V) and capacitance-voltage (C - V) measurements using an Agilent E2902B semiconductor analyzer and an Agilent E4980A LCR meter, respectively, at room temperature. The morphology of the Pd and the IGZO thin films were investigated using an atomic-force microscope (AFM, Dimension FastScan™).

The J - V curves of the fabricated Schottky diodes were analyzed using standard theory of thermionic emission of majority carriers over the junction barrier,¹⁹

$$J = A^* T^2 \exp\left(-\frac{q\Phi_{B,JV}}{kT}\right) \left(\exp\left[\frac{q(I - R_s)}{nkT}\right] - 1 \right) \quad (1)$$

where q is the element charge, R_s is the series resistance, k is the Boltzmann constant, A^* is the effective Richardson constant which is $41 \text{ Acm}^{-2}\text{K}^{-2}$ for IGZO,³ and $\Phi_{B,JV}$ is the effective barrier height measured by J - V characteristics.

The capacitance of a Schottky junction is given by,¹⁹

$$\frac{A^2}{C^2} = \left(\frac{2}{q\epsilon_s\epsilon_0 N_{depl}} \right) \left(V_{bi} - \frac{kT}{q} - V \right) \quad (2)$$

where A is the active area of the diode, ϵ_s is the static dielectric constant of the semiconductor, ϵ_0 is the dielectric constant of vacuum, V_{bi} is the built-in potential, and N_{depl} is the background doping density in the depletion region.

Figure 1 shows the J - V curves of IGZO/Pd Schottky diodes with and without thermal annealing at different stages of the device fabrication. For Sample A, the SiO_2/Si substrate was annealed at 300°C for 30 min but the Pd anode was not annealed; Sample B: the SiO_2/Si substrate was annealed at 300°C for 30 min, and after deposition of Pd on the substrate, the sample was annealed at 230°C for 60 min; Sample C: neither the substrate nor the anode was annealed; **Sample D: the SiO_2/Si substrate was not pre-annealed but after deposition of Pd, the sample was annealed at 230°C for 60 min. It has been found that water molecules bonded to the silanol groups of SiO_2/Si substrate can be desorbed via annealing at 220°C ,²⁰ thus the substrate annealing at 300°C removes moisture and organic adsorbates, thereby improving the uniformity of substrate surface and adhesion of Pd anode.**

As can be seen in Fig. 1, at an applied voltage of 1 V, the on-current densities (J_{on}) of the four samples are of the order of 10^9 A/cm^2 with R_s in the range of $0.06 \sim 0.08 \Omega\cdot\text{cm}^2$. In contrast, at an applied voltage of -1 V, the off-current densities (J_{off}) show clear dependence on the process conditions, resulting in significant differences in $I_{\text{on/off}}$ ratios. **Sample A, fabricated with annealed SiO_2/Si and as-deposited Pd anode, exhibits the highest performance with an $I_{\text{on/off}}$ of 7.2×10^7 , a $\Phi_{B,JV}$ of 0.88 eV, and a near unity n of 1.09.** Using Eq. (1), the extracted $\Phi_{B,JV}$ are 0.88, 0.86, 0.85, and 0.77 eV, for samples

A, B, C and D, respectively, as shown in Table 1, which could partly explain the differences in J_{off} . All four samples show near unity n of ~ 1.1 , indicating that the diodes have high-quality IGZO/Pd Schottky contact interfaces. A comparison of samples A and C shows that the substrate annealing enhances Φ_B by about 30 meV and enables a decrease of one order of magnitude in J_{off} . In order to further evaluate the surface morphology, AFM characterization has been performed. The results show that the as-deposited Pd films on annealed and unannealed SiO_2/Si substrates (Samples A and C) exhibit RMS roughnesses of 0.69 and 0.75 nm, respectively, as shown in Figs. 2(a) and (c). However, a comparison of samples A and B shows that Pd annealing contributes to a slight degradation in device performance, with $I_{\text{on/off}}$ and $\Phi_{B,JV}$ decreasing from 7.2×10^7 to 3.5×10^7 and 0.88 to 0.86 eV, respectively. This is correlated to an increase in Pd RMS roughness from 0.69 to 0.73 nm after annealing of the Pd anode, as shown in Figs. 2(a) and (b). The thermal expansion coefficient value is $5.2 \times 10^5 \text{ }^\circ\text{C}^{-1}$ for SiO_2 ²¹ and is $1.2 \times 10^7 \text{ }^\circ\text{C}^{-1}$ for Pd²². The latter is about 23 times higher, which induces large stresses in the SiO_2/Pd interface during the heating up and cooling down processes. This could increase the surface roughness of Pd surface as well as the Pd/IGZO interface.²³ Furthermore, desorption of water molecules bonded to the silanol groups of SiO_2/Si substrate by thermal annealing of the substrate is expected to improve the uniformity and surface roughness of SiO_2/Si substrate and perhaps more importantly strengthens the adhesion of Pd layer, resulting in sample A having the lowest Pd surface roughness. Although sample D appears to have a slightly low RMS roughness than sample C, the difference is only 0.02 nm, as shown in Figs. 2(c) and (d), which is within the measurement error range of the AFM that we used. In our experiments, we have fabricated a large number of devices (about 4) under each of the four conditions, and the J - V and surface roughness results are consistent among these devices.

Fig. 1 J - V characteristics of the as-deposited IGZO/Pd Schottky diodes on annealed (Ann.) and unannealed (No Ann.) SiO_2/Si substrates and with annealed (Ann.) and unannealed (No Ann.) Pd anodes. The annealing conditions are 300 $^\circ\text{C}$ / 30 min for SiO_2/Si and 230 $^\circ\text{C}$ / 60 min for Pd. The cross-section schematic of the diode is shown in the inset.

Table 1 The root mean square (RMS) roughness of Pd anode, series resistance (R_s), ideality factor (n), rectification ratio ($I_{\text{on/off}}$) at ± 1 V. Schottky barrier height calculated by J - V ($\Phi_{B,JV}$) and C - V ($\Phi_{B,CV}$), and the different between two ($\Delta\Phi = \Phi_{B,CV} - \Phi_{B,JV}$), built-in potential (V_{bi}), background doping density (N_{depl}), and free carrier concentration (N_c) for samples A, B, C and D.

Sample	A	B	C	D
RMS Pd_{anode} (nm)	0.69	0.73	0.75	0.73
R_s ($\Omega \cdot cm^2$)	0.06	0.08	0.08	0.06
n	1.09	1.13	1.12	1.14
$I_{on/off}$	7.21×10^7	3.48×10^7	2.93×10^7	1.08×10^6
$\Phi_{B,JV}$ (eV)	0.88	0.86	0.85	0.77
$\Phi_{B,CV}$ (eV)	0.79	1.04	0.87	0.69
$\Delta\Phi$ (eV)	-0.09	0.18	0.02	-0.08
V_{bi} (eV)	0.51	0.75	0.58	0.41
N_{depl} (cm^{-3})	4.0×10^{16}	5.0×10^{16}	5.2×10^{16}	5.2×10^{16}
N_e (cm^{-3})	9.9×10^{13}	7.7×10^{13}	8.1×10^{13}	9.9×10^{13}

Fig. 2. AFM images and the RMS surface roughness of as-deposited (a) and annealed (b) Pd surfaces on annealed SiO_2/Si substrates, and as-deposited (c) and annealed (d) Pd surfaces on **unpreannealed** SiO_2/Si substrates.

Figure 3(a) shows C - V characteristics of sample A in the frequency range of 1 kHz to 1 MHz at room temperature. It is found that the measured C strongly depends on the frequency. The curves shift towards positive voltage and the measured C decreases with increasing frequency due to the existence of interface traps.²⁴ At low frequencies, the time constant permits the charge to move in and out of interface trap states in response to an applied signal, that is, an excess capacitance is induced. However, at a sufficiently high frequency, the time constant is too short for the interface trap states to respond and the excess capacitance can be neglected.²¹ To minimize the influence of the interface trap states on C - V measurements, a high frequency of 1 MHz was used for all four samples A, B, C and D, as shown in Fig. 3(b). The relative dielectric constant of IGZO is 17.6 as we reported previously.^{15,17} From the A^2/C^2 - V curves and Eq. (2), the built-in voltage V_{bi} and N_{depl} are extracted. The free charge concentration, N_e , can be estimated from R_s by assuming an electron mobility of $10 \text{ cm}^2/Vs$.^{5,15} V_{bi} is decreased and the N_{depl} is increased in order of samples B, C, D, which results in a decrease of the depletion region

thickness, as shown in Fig. 3(c). The barrier height from C - V measurements, $\Phi_{B,CV}$, is given by $\Phi_{B,CV} = qV_{bi} + \frac{kT}{q} \ln\left(\frac{N_c}{N_e}\right)$, where the last term describes the energy gap between the conduction band and Fermi level, and $N_c = 5.2 \times 10^{18} \text{ cm}^{-3}$ is the conduction band density of states.²⁵ The calculated values are shown in Table 1. The discrepancy between $\Phi_{B,JV}$ and $\Phi_{B,CV}$, $\Delta\Phi = \Phi_{B,CV} - \Phi_{B,JV}$, is most likely due to the barrier inhomogeneities.^{26,27} $\Phi_{B,JV}$ obtained from the current-voltage measurement is rather sensitive to the barrier inhomogeneities and is more related to the regions where the barrier is the lowest.²⁶ In contrast, C - V measurements give the mean barrier height which is usually smaller than $\Phi_{B,JV}$ for single crystalline semiconductors with extremely low trap state densities.²⁸⁻³⁰ However, in amorphous semiconductors such as IGZO, due to the contribution of relatively large subgap trap density to the measured C , $\Phi_{B,CV}$ is sometimes higher than $\Phi_{B,JV}$.^{15,16} The very low $|\Delta\Phi|$ (0.02-0.18 eV) of samples A, B, C, and D indicates a high uniformity of barrier height and high quality of the Schottky contacts, which agrees well with the low n (~ 1.1) of these diodes. The best optimized device, sample A, has the lowest N_{depl} of $4.0 \times 10^{16} \text{ cm}^{-3}$ and the highest N_e of $9.9 \times 10^{13} \text{ cm}^{-3}$, as shown in Table 1. The discrepancy between N_{depl} and N_e is mainly attributed to the subgap traps in amorphous semiconductor.^{11,14,16} **Sample A has the lowest ratio N_{depl}/N_e of 4.0×10^2 , which means for each free electron, there are roughly 4.0×10^2 ionized atoms.** This indicates that among the four samples, sample A has the lowest subgap trap density.¹⁶ As the IGZO layer in all the samples is deposited under the same condition, it is expected that their bulk trap density should be the same. Thereby, the discrepancy of subgap trap density of these samples is due to different thermal treatments of the substrate and the anode, causing different interface trap densities. The interface state density is expected to depend greatly on the interfacial roughness.^{31,32} **Larger film roughness causes larger interfacial area, resulting in a possibility of more interface states even if their density per real interface area remains the same.**³³ Furthermore, the increased roughness was most likely caused by different thermal expansion coefficients, and the residual strain in the film may also lead to increased band-gap states.³⁴ Our C - V and AFM results therefore suggest that sample A has both the lowest interface trap density and the smoothest Schottky anode interface.

Fig. 3 (a) The capacitance-voltage ($C-V$) measurements of sample A at various frequencies. (b) $C-V$ curves measured at 1 MHz of samples A, B, C and D. (c) The corresponding background doping density (N_{depl}) as a function of depletion thickness. The dotted line indicates the depletion region thickness at zero bias.

In summary, by performing thermal treatment on individual layers during fabrication of IGZO Schottky diodes, we have observed a dependency of the device performance on the roughness of different layer surfaces. While thermal annealing of the SiO_2/Si substrate improves the device homogeneities, an opposite effect is observed on the annealing of the Pd electrode. Furthermore, a correlation between the roughness of the Schottky contact and the interface trap state density has also been

observed. Using the obtained optimized process, an on/off ratio as high as 7.2×10^7 and a near-unity ideality factor of 1.09 have been achieved. This is the highest performance among as-deposited IGZO Schottky diodes reported to date.

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