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DC-BUS POWER QUALITY FOR UAV SYSTEMS DURING GENERATOR FAULT CONDITIONS

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Abstract

High-voltage DC-bus power quality is examined experimentally and by computer simulation during a short-circuit fault across the phase terminals of a five-phase, permanent magnet fault-tolerant generator. The DC-bus transients are seen to exceed the limits in MIL-STD-704F [1] and a control algorithm is proposed for a supercapacitor-based energy storage device that mitigates the transients. The controller performance is illustrated by computer simulations.

1 Introduction

The increasing use and criticality of electrical systems on-board future aircraft is driving the development of new fault-tolerant generator technologies and new power distribution systems such as high-voltage DC networks. This paper examines the system-level impact of short-circuit faults across the terminals of a fault-tolerant generator, in particular the effect on the DC-bus voltage waveform. A control method is then proposed for a supercapacitor-based energy storage device to mitigate the DC-bus voltage transients.

A five-phase, fault-tolerant generator is considered in this work in which each phase is electrically, thermally and magnetically isolated from the others [2]. Furthermore each phase has a 1 p.u. impedance which limits the current flowing into a terminal short-circuit to 1 p.u. This property enables the machine to continue generating through the remaining healthy phases when one or more of the windings has a short-circuit fault.

To preserve the fault-tolerance of the system, each phase winding is passed through a separate H-bridge AC/DC converter before being connected to a common DC-bus as shown in Fig. 1. The PWM controllers on each H-bridge ensure that the generator currents are sinusoidal and also regulate the DC-bus voltage [3]. Load sharing between the H-bridge converters is achieved using simple droop controllers. The generator has a rating of 70kW, the nominal DC-bus voltage is set at 540V and the DC output voltage of the H-bridges is set to droop by 20V at full phase loading to ensure balanced phases.

Figure 1. System configuration

The DC-bus system under consideration in this work includes a number of load elements which may be configured to have either resistive or constant power characteristics [4]. The system also includes an energy storage device (ESD) comprising a supercapacitor bank and bi-directional DC/DC converter. The primary function of the ESD is to meet transient load demands, thereby protecting the generator and aircraft gas engine from rapid and/or repetitive load changes. A control method for the ESD has been described in previous work [5].

In the following sections experimental measurements and simulation results are presented to examine the effect of a short-circuit fault across one of the generator phase terminals. Large voltage deviations in DC-bus voltage are observed, partly at least due to the relatively small value of DC-bus capacitance, and this in turn is due to the requirement to avoid electrolytic capacitor types in aerospace systems. As there are no published standards for the power quality of 540V DC aerospace systems, the results are compared with the limits in MIL-STD-704F [1], which relates to 270V DC supplies. Since the observed deviations in DC-bus voltage are well outside the limits set by MIL-STD-704F, the control system for the ESD is modified to provide voltage support for the DC-bus. The system performance during multi-phase generator short-circuit winding faults is examined in subsequent sections by means of simulation and is seen to meet the requirements of MIL-STD-704F.

2 Validated Single-Phase Fault Response

A Simulink-based simulation of the system in Fig. 1 was developed using lossless averaged-value models of the PWM H-bridge converters. The generator was modelled as five sinusoidal back emfs in series with the corresponding winding inductance and resistance. Friction and windage losses were omitted. The total capacitance on the 540V DC-bus was 800 μ F. In these initial tests the ESD was not connected.

In the test-rig the short-circuit fault was applied to the machine winding through the converter as this provided a convenient way of setting and removing the fault. This condition is representative of the system response to either a machine winding or IGBT fault. In the event of an IGBT short-circuit fault, the system response would be to switch on the corresponding healthy device in the other leg, placing a short-circuit across the phase terminals. In these tests the short-circuit is applied to a phase winding by halting the PWM signals so that the top switch in each H-bridge converter leg is permanently closed with the bottom switches open [6].

Fig. 2 shows the response of the generator to a single-phase short-circuit fault on phase 'c' at approximately $t=1.03$ s. Experimental results [6] are shown in Fig. 2.a. and results from the averaged-value model in Fig. 2.b. The operating condition pre-fault was all five generator phases active at 1001rpm, 540V DC-bus voltage and a 26.7kW resistive load. The per-phase AC and DC currents, I_{gen-AC} and I_{gen-DC} , respectively, DC-bus voltage, V_{bus} , and torque, T_e , are shown

in the results. I_{gen-DC} is filtered by a 4.66Hz low pass filter to remove the second-harmonic component prior to its use in the generator droop controllers which ensure balanced phases.

Prior to the fault, $t < 1.03$ s, the five machine phases share equally the 26.7kW load power, top left plot in Figs. 2.a and 2.b. The second plots in Figs. 2.a and 2.b. show I_{gen-DC} per phase, which are identical prior to the fault at 9.9A.

Phase 'c' is switched to a short-circuit fault at $t=1.03$ s. The top centre plots in Figs. 2.a. and 2.b. show I_{gen-AC} in the faulted phase rising to the 1 p.u. value of 116A. I_{gen-AC} in the remaining four phases, top right plots in Figs. 2.a. and 2.b., show a slight increase as the control [3] now regulates these phases to share the total power. I_{gen-DC} in the faulted phase falls to zero in the second plots in Figs. 2.a. and 2.b. and the outputs of the remaining four phases increase to maintain the load requirements; this is possible as prior to the fault the phases were operating below the 14kW limit per-phase.

A negative deviation in the DC-bus voltage, V_{bus} , is apparent when the short-circuit is applied, shown in the third plots in Figs. 2.a. and 2.b. V_{bus} falls to 467V in the simulation and 468V in the test results. This 73V deviation in bus voltage marginally exceeds the +60/-70V limit in MIL-STD-704F [1] for a 270V bus. A significant ripple component is apparent on V_{bus} in the test results, third plot in Fig. 2.a which was attributed to parasitic effects in the system and measurement noise. The 5V amplitude second-harmonic V_{bus} ripple during faulted operation, third plot in Fig. 2.b., is within the 6V amplitude allowed in MIL-STD-704F.

a. test result [6]

b. simulation result

Figure 2. Single-phase short-circuit at $t=1.03$ s, 1001rpm, 540V, with a 26.7kW resistive load

a. test result [6]

b. simulation result

Figure 3. Single-phase fault recovery at $t=1s$, 1001rpm, 540V, with a 26.7kW resistive load

A slight deviation is noticeable in the generator torque, T_e , fourth plots in Figs. 2.a. and 2.b. after fault occurrence. The simulation results, raw data in Fig. 2.b. (red trace), shows the magnitude of the second-harmonic ripple component of T_e when the machine operates with only four phases. The mechanical couplings and the torque transducer in the test system filters this second-harmonic ripple component. For comparison purposes the simulation model T_e is filtered; this filtered T_e , shown in the fourth plot in Fig. 2.b. (blue trace) correlates closely with the measured T_e in the fourth plot in Fig. 2.a. The top right plots in Figs. 2.a. and 2.b. show I_{gen-AC} per phase in the machine post fault, with the current in phase 'c' being purely reactive and 1 p.u. due to the high winding inductance. The four healthy phases have approximately equal current magnitudes.

The recovery of a single faulted phase at $t=1s$ is shown in Fig. 3.a for the test-rig and Fig. 3.b for the averaged-value simulation. The top left plots in Figs 3.a. and 3.b. show the fault on phase 'c' with the remaining phases generating the 26.7kW load power at 1001rpm. Phase recovery is initiated by restarting the PWM for phase 'c' at $t=1s$, shown in the top centre plots in Figs. 3.a. and 3.b. Initially, within 500ms, the controller reduces the phase 'c' current from the fault level, then, gradually, over a period of three to four seconds the active power drawn from the phase is increased. There is a corresponding increase in the DC output current from phase 'c' and a complementary reduction in the output currents from the other phases as they adjust to share the total load current

equally, second set of plots in Figs. 3.a. and 3.b. When the recovery of phase 'c' is initiated there is only a very slight disturbance in V_{bus} and T_e , third and fourth plots in Figs. 3.a. and 3.b., as the fault current is brought under control. Also the second-harmonic component in T_e , which is particularly evident in the simulation, is virtually eliminated once phase recovery is complete.

3 Control of Energy Storage Device

The negative deviation in V_{bus} due to a single-phase short-circuit generator fault, shown in Fig. 2, exceeds the permissible voltage limits set for a 270V bus as defined in MIL-STD-704F [1] and a multi-phase short-circuit fault is likely to cause even larger deviations in V_{bus} .

The energy storage device (ESD) shown in Fig. 1 is primarily intended to protect the generator and gas engine from rapid load transients, thereby limiting the rate-of-change of torque applied by the generator on the engine [5]. An additional control element is introduced here to enable the ESD to support the DC-bus during generator faults, reducing the deviation in V_{bus} . This fault mitigation control is explained in the remainder of this section.

The ESD comprises a supercapacitor bank and a simple, unisolated, bi-directional DC/DC converter [5] as the interface to the DC-bus. A dual-input supercapacitor current reference control system for the ESD was developed [5]; I_{sc-L} is determined by a power-balance control to track

instantaneous load changes on the DC-bus, whilst I_{sc-rc} regulates the supercapacitor state-of-charge. The calculation of I_{sc-L} and I_{sc-rc} are shown in Fig. 4, together with a third reference value component, the output of the fault mitigation controller, I_{sc-F} , which enables the ESD to support V_{bus} during generator faults.

Figure 4. ESD control

The variables V_{bus} and I_{bus} are the bus voltage and current, V_{sc} is the terminal voltage on the supercapacitor bank and V_{sc}^* is the reference value for V_{sc} which is fixed at 135V as k_{rc} , the recharge gain, operates like a droop control, automatically adjusting the supercapacitor state-of-charge.

The use of I_{bus} in the calculation of I_{sc-L} ensures that the ESD responds rapidly to load changes, however, during a generator fault V_{bus} and I_{bus} both experience negative deviations, which reduces P_{bus} and therefore I_{sc-L} , and results in the ESD sinking power from the bus. This additional load may result in the generator exceeding its current rating and/or V_{bus} collapsing completely. A fault mitigation control has been added to the original ESD control, Fig. 4, based on a simple proportional term which increases I_{sc-F} when a negative deviation occurs on V_{bus} causing the ESD to supply power to the bus, thereby supporting the bus voltage. The fault mitigation control, Fig. 4, uses a fixed 540V reference value for V_{bus} to avoid the requirement for communication between the ESD and generator control unit. As the DC-bus voltage, V_{bus} , is programmed to droop below the nominal 540V level by 20V at full phase power the fixed V_{bus} reference for the ESD results in I_{sc-F} being zero only when there is no load on the bus.

The proportional term in the fault mitigation control has a bandwidth of 800Hz, significantly less than the current control bandwidth of 8kHz to ensure no interactions between the control loops.

The 55F supercapacitor bank has a terminal voltage of 145V and approximately 0.4MJ of usable energy capacity [5]. The bi-directional DC/DC converter was chosen to have a switching frequency of 30kHz and an inductor value of 100μH [5]. The total capacitance on the 540V DC distribution bus was 800μF.

The non-linear recharge function, k_{rc} , used to regulate the supercapacitor voltage within its working range, was set to

$$k_{rc} = 0.64\tilde{V}_{sc}^2 \quad (1)$$

The function, (1), was chosen to give a 33V drop in V_{sc} at 70kW load power and enables the ESD output to settle in approximately 10s.

4 Multi-Phase Fault Response with Energy Storage Device

The DC-bus voltage and generator torque are examined in this section during multi-phase generator faults with resistive and combined resistive and constant power loads on the bus, both with and without the ESD. All results relate to three generator phases suffering simultaneous short-circuit faults, with all phases being faulted on the zero crossing of phase 'a' terminal voltage, which results in a higher deviation in DC-bus voltage compared to the staggered faulting of the phases. The bus is nominally loaded with 26.7kW of resistive load which is the maximum power output of two active phases. The speed is constant at the minimum operating speed of 1000rpm as the phase current and torque are highest. The above conditions result in one of the worst case scenarios for the generator in normal service.

In Figs. 5 and 6 the bus is initially loaded with 26.7kW of resistive load and all five phases are active. At $t=5s$ three generator phases, a, b and c, suffer short-circuit faults, at $t=10s$ the load is reduced to 2.5kW for 5s then restored to 26.7kW and finally at $t=25s$ the three generator phases are restarted. In Fig. 5, the ESD is inactive, and large deviations are apparent in V_{bus} during the fault and load transients; the maximum and minimum bus voltages are 770V and 340V respectively. Currently the closest available standard, MIL-STD-704F [1], governing the instantaneous voltage of a 270V bus following a transient allows +60/-70V deviations.

When only two generator phases are active, $5s < t < 25s$, the second-harmonic component is noticeable on V_{bus} and T_e , second and third plots in Fig. 5; outside this time range the second-harmonics of the five active phases cancel. A 90Nm second-harmonic ripple is apparent on T_e during the high-load $5s < t < 10s$ and $15s < t < 25s$ which would be attenuated by the mechanical system in the experimental test-rig. The 6.8V amplitude second-harmonic ripple on V_{bus} during high-load marginally exceeds the MIL-STD-704F limit of 6V.

Fault and bus load changes, $t=5, 10$ and $15s$, result in large transients in AC-current, I_{gen-AC} , and torque, T_e , in the first and third plots in Fig. 5. The 177Nm T_e steps at $t=5$ and $10s$ will impact on the gas engine and may affect engine performance.

Due to the controller design, the phase recovery at $t=25s$ results in a gradual adjustment of the generator currents and virtually no deviation in V_{bus} , second plot in Fig. 5.

Figure 5. System behaviour with 26.7kW resistive load; ESD inactive

Figure 6. System behaviour with 26.7kW resistive load; ESD active

In Fig. 6 the same events are shown as in Fig. 5 but the ESD is active. The second plot shows V_{bus} and the large deviations in Fig. 5 are significantly reduced, the minimum and maximum values being 499V and 545V, well within the allowable limits defined by MIL-STD-704F [1].

I_{gen-AC} and T_e , the first and third plots in Fig. 6, with the exception of the instant of fault occurrence $t=5s$, demonstrate milder rates-of-change than in Fig. 5, due to the ESD which rapidly responds to V_{bus} deviations in the case of faults or phase recovery by supplying/drawing power to/from the bus. The high current and torque peaks immediately after fault occurrence are unchanged in Figs. 5 and 6 as the ESD has no direct effect on generator currents. The second-harmonic ripple on V_{bus} and T_e are unchanged in Fig. 6 due to the relatively low bandwidth (800Hz) of the V_{bus} regulation loop in the ESD. The fourth plot in Fig. 6 shows the contributions of the generator and ESD to bus current. Negative ESD current, and an increase in V_{sc} , fifth plot in Fig. 6, indicates power drawn from the bus. The ESD output settles to zero in approximately 10s.

Figs. 7 and 8 show the system behaviour when a 22.6kW resistive load together with a 9kW constant power load (CPL) are present on the DC-bus. In Fig. 7, with the ESD inactive, fault occurrence at $t=5s$ results in V_{bus} deviations of -294/+234V, larger than with only a resistive load. Switching the 9kW CPL off at $t=10s$ and back on at $t=15s$, also result in large bus transients. The second-harmonic ripple is apparent on V_{bus} and T_e , second and third plots in Fig. 7, during the generator fault. The total bus load in Figs. 5 and 6, and Figs. 7 and 8 are approximately equal at $t<10s$ and $t>15s$ and so fault occurrence at $t=5s$ has a similar effect on I_{gen-AC} and T_e , first and third plots in Fig. 7 and Fig. 5.

Fig. 8 shows the system behaviour for the same events as in Fig. 7 but with the ESD active. The deviations in V_{bus} , second plot in Fig. 8 are almost eliminated at the instants of fault occurrence and load switching. I_{gen-AC} and T_e (first and third plots in Fig. 8) exhibit very mild variations except at fault occurrence. The fourth and fifth plots in Fig. 8 demonstrate the performance of the ESD during both generator fault occurrence and load changes. The peak ESD currents and the excursions in supercapacitor voltage are lower than in Fig. 6 due to the smaller load changes at $t=10$ and $15s$.

5 Conclusions

A simple fault mitigation function is added to the load-tracking, power-balance controller of a supercapacitor-based energy storage device to control the DC-bus transient during short-circuit faulted operation of a multi-phase fault-tolerant generator. The fault mitigation controller enables the energy storage device to respond instantaneously to generator faults, virtually eliminating voltage transients from the DC-bus.

The operation of the controller has been demonstrated by computer simulation. The controller will also be effective in limiting DC-bus voltage transients that are caused by other phenomena such as bus switching and the connection or disconnection of other power sources.

Figure 7. System behaviour with 22.6kW resistive and 9kW CPL; ESD inactive

Figure 8. System behaviour with 22.6kW resistive and 9kW CPL; ESD active

Experimental data for the system during a single phase generator short-circuit fault has been used to validate the simulation model when the energy storage device is inactive. The generator behaviour under a converter short-circuit fault shows that the generator control automatically shares the power between the remaining healthy phases, providing the prefault power can be achieved without overloading the remaining active phases. Recovery of the faulted phase has then been demonstrated.

The simulation model was then extended to impose a three phase short-circuit fault on the five phase generator, which represents one of the worst case fault scenarios. Resistive and combined resistive and constant power loads, were used to demonstrate the system performance under faulted generator conditions both with and without the energy storage device.

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