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FPGA based Gate Signal Generator for Three-level Neutral Point Clamped Inverters

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Abstract—The gate signals in a commercial three-phase two-level induction motor drive are translated to operate a three-phase three-level neutral point clamped (NPC) inverter. An FPGA is used to demodulate the two-level gate signals and then to generate NPC gate drive signals by re-modulation. A sine PWM modulation strategy with in-phase disposition of carriers is used to generate NPC gate drive signals. The modulation strategy is simulated first and then implemented using an Altera FPGA. The close match between the simulation and experimental results proves the concept and demonstrates the accuracy of this unique modulation technique.

Keywords— NPC inverter; Modulation strategy; sine PWM; VHDL code; FPGA

I. INTRODUCTION

In any AC motor drive system, harmonics in the applied voltage cause losses and pulsating torques in the motor. The main reason for the development of pulse width modulation (PWM) technique for the motor-drive inverter was to reduce these harmonics and to ensure better control of the fundamental voltage. Again, three level inverters were developed to further reduce harmonics and consequently to increase the efficiency of the motor drive system. [1]

Compared to the two-level inverter a conventional three-level neutral point clamped (NPC) inverter features two additional active switches, two extra isolated gate drivers, and four extra diodes per phase leg (Fig. 1(a) and 1(b)). In case of three-level T-type neutral point clamped inverter (TNPC), a total of four active switches and four diodes are required per phase (Fig. 1(c)). Both NPC inverters have the advantage of better controllability of phase currents and DC link voltage, lower output current total harmonic distortion and therefore smaller passive components, higher efficiency at increased switching frequency (considering similar modulation technique), and lower voltage stress on the switching components (only for NPC inverter) [2, 3].

There are many PWM modulation techniques for both two-level inverter and three-level NPC inverter. For both inverters popular PWM techniques are sine-triangle PWM, space vector PWM, PWM with third harmonic injection, programmed PWM with selective harmonic elimination and current-regulated PWM from hysteresis control [4, 5]. In both cases the simplest form of PWM generation technique is sine-triangular PWM

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where sinusoidal control signals are compared with the triangular carrier signal(s) to generate gate pulses for the power switches.

Fig. 2(a) and 2(b) respectively show the simplified inputs and actual PWM inputs to the gate drivers of four switches (T1-T4) in a phase leg of a NPC or TNPC inverter circuit shown in Fig. 1(a) and 1(b). Fig. 2 also shows the respective hypothetical phase to neutral voltage output, $u(t)$. The auxiliary transistors (T2,T3) are driven with complementary gate signals to the main transistors (T1,T4). When the upper two switches (T1,T2) are on, the output voltage is equal to +DC, when the middle two switches (T2,T3) are on, the output voltage is zero, and when the bottom two switches (T3,T4) are on, the output voltage is equal to -DC.

Fig. 1. Phase leg of a (a) 2L inverter, (b) three-level NPC inverter and (c) three-level TNPC inverter

In this paper an FPGA based implementation of sine-triangular PWM modulation technique for three-level NPC inverter is presented. The uniqueness of the proposed technique is the derivation of the sinusoidal control signals directly from the gate signals of a commercial three-phase bridge (3PB) (two-level) converter. The two-level PWM gate drive waveform is demodulated and then re-modulated into a three-level PWM gate drive waveform. An example of the useful application of this technique is when investigating how an existing commercial two-level motor drive product would perform with an alternative three-level power output stage. In this case, it is not necessary to redesign an existing and proven Application Specific Integrated Circuit (ASIC) solution from the original product. In addition, if the existing ASIC lacks sufficient PWM output hardware, the cost associated with migrating this into a new ASIC is also avoided. This technique can dramatically reduce development time and is particularly useful in the early

prototyping an experimentation phase of a design when the advantages of a three-level output stage are under investigation. Although the technique requires the addition of an FPGA device to perform the de- and re-modulation, it could potentially be used in a final design to extend an existing product family whilst keeping common DSP hardware and avoiding a major redesign and qualification process.

Fig. 2. Hypothetical gate driver signals and output phase voltage of NPC or TNPC inverter (a) simplified signals and (b) PWM signals

II. MODULATION TECHNIQUES FOR THREE-LEVEL NPC INVERTER

Although there are many strategies for generating gate signals for NPC inverters most of them are extension of either sinusoidal PWM technique or space vector PWM technique or a hybrid technique between them. A brief description of the common modulation techniques from literature is given in this section.

A. Standard Sinusoidal PWM Techniques

Standard Sinusoidal PWM techniques for NPC inverters can be categorized according to the different types of carrier signals. Usually in three-level NPC inverters two triangular carrier signals are required for sine PWM modulation for each phase. These two carrier signals can be phase shifted or voltage shifted or both phase and voltage shifted. They are compared with a sinusoidal modulating waveform to generate the gate pulses for the semiconductor switches in each phase. The most common sinusoidal PWM techniques for NPC inverters are in-phase disposition method and phase-opposition disposition method [6, 7].

Fig. 3(a) and 3(b) show the two sine-PWM modulation strategies for three-level NPC or TNPC inverters. In both cases, the frequency of the carrier signals (f_c) determine the switching frequency of the output phase voltages and the frequency of the sinusoidal modulating wave (f_m) determines the fundamental frequency of the output voltages and currents. Also in both cases, the sampling is a natural sampling and the output phase voltage spectrum consists of harmonics at the frequencies, f_m (fundamental frequency), f_c (switching frequency), $m_f f_c$ (switching harmonics' frequencies) and $m_f f_c \pm m_f f_m$ (side-band harmonics frequencies); where m_f the frequency modulation index equals to the ratio between the

carrier frequency and the modulating frequency, f_c / f_m . The amplitude modulation index, m_a determines the peak of the fundamental component of output phase voltage, V_{u_peak} as shown in equation (1) for linear modulation.

$$V_{u_peak} = \frac{m_a V_{DC}}{2} \quad (1)$$

where, V_{DC} is the total DC link voltage and

$$m_a = \frac{A_m}{A_c} \quad (2)$$

Here, A_m is the peak value of the modulating waveform and A_c is the peak value of the carrier waveforms. For linear modulation, $A_m \leq A_c$.

The PWM gate signals shown in Fig. 2 (b) can be found from the comparison between the modulating and carrier signals shown in Fig. 3. For example, when the modulating signal is greater than the positive carrier signal in Fig. 3(a), then the corresponding semiconductor switch is turned on i.e. V_{g1} is positive. Otherwise the semiconductor switch is turned off i.e. V_{g1} is zero. Similarly, the negative carrier determines V_{g2} . V_{g3} and V_{g4} are found by taking the complementary signals of V_{g1} and V_{g2} , respectively. Sometimes, zero sequence voltages are added to the modulating signal to reduce switching losses and to gain better control of the neutral point voltage [8].

Fig. 3. Sine PWM strategies for NPC or TNPC inverter (a) in-phase disposition of carriers and (b) phase-opposition disposition of carriers

B. Space Vector PWM Techniques

As shown in Fig. 2 each output phase voltage of the NPC inverter depends on the switching state of any two phase-leg switches. Therefore, there are three types of switching states per phase and in total there are 27 switching states for the three phase inverter [7, 9]. If the three switching states corresponding to the DC, 0 and $-DC$ levels are denoted as P, G and N, the 27 switching states can be shown in a space vector diagram as in Fig. 4. Based on the magnitude and the angle of the output voltage phasor (a space vector voltage), four groups of the switching states are selected from the space vector diagram of Fig. 4. Different optimization techniques such as minimum commutations, commutations only between adjacent states,

easy transitions etc. are used to optimize the switching sequence of this modulation technique [7, 9].

Fig. 4. Space vector diagram of NPC or TNPC inverter output voltage

C. Double Signal PWM Techniques

Two modulating signals are used per phase to generate the gate pulses in double signal PWM techniques. The simplest of these techniques uses two sinusoidal modulating waves, one positive and one negative and one triangular wave to generate the gate pulses for a phase leg (dipolar modulation) [5]. In [10], two modified modulation signals were derived using a zero sequence voltage obtained from space-vector modulation patterns, which were then compared with two carrier signals to generate the gate pulses. Low frequency voltage oscillation of the neutral point was reduced by this method at the expense of increased switching losses compared to the sine PWM or space vector PWM techniques.

D. Other Hybrid Modulation Techniques

Several other hybrid modulation techniques were proposed for NPC inverters in the previous literatures. A hybrid modulation strategy combining the zero sequence voltage based double signal PWM and sine PWM is proposed in [11], where the two modulating signals are further modified using a separate controlling parameter. This strategy gives an optimum performance in voltage sharing of the DC-link capacitors under all power factor operations at the expense of slightly higher switching loss. A DSP based single carrier modulation strategy is proposed in [12], where gate signals between the three phases were cross-coupled to get the neutral point voltage balance.

III. CONFIGURATION OF THE SYSTEM

A three-level NPC inverter's modulator based on the sine PWM modulation was designed. In-phase disposition of carriers were used as the sine PWM modulation technique because of its better harmonic performance compared to others [6]. The three control signals for the sine PWM modulation had to be derived from an Emersion Control Techniques Unidrive SP0401. It is a commercial 400V rated motor drive based on a three-phase bridge (3PB) converter which can run in both open loop and closed loop mode. Space vector PWM with third harmonic injection is the modulation strategy for the Unidrive

[13]. The gate driving circuit of the Unidrive SP0401 was modified to access the three gate signals of either upper-leg power devices or lower-leg power devices of the 3PB converter. Then, the three gate signals were demodulated to get the three control signals for sine PWM modulation of three-level NPC inverter. An FPGA was used for the demodulation and also for the further sine PWM modulation of the NPC inverter.

IV. SIMULATION RESULTS

Both NPC and TNPC inverters were simulated in National Instrument Multisim Software considering 800V DC link. All the switches were considered ideal and independently operated and no parasitic was considered in the circuits. The parameters of a 4kW induction machine were used to simulate a fixed load, considering its fixed speed operation. Therefore, the frequency of phase to neutral voltage was 50 Hz.

Fig. 5 depicts the gate signal generation strategy using sine PWM modulation technique. Although, here it is shown for only one phase-leg, the arrangement for rest of the two phase-legs was exactly same except for the control voltages, which would be 120° phase shifted from each other. In the upper two comparators, the 50Hz sinusoidal control signal was compared with two 3 kHz triangular carrier signals. Both triangular signals (V3 and V4) had only positive values, but they were 1μs delayed from each other to ensure 1μs dead-time between the complementary gate signals. The output of these comparators produced the gate signals for the transistor, T1 and its complementary pair transistor, T3 (Fig. 1). Similarly, gate signals for the transistor T2 and its complementary pair, T4 were generated by comparing the same control signal with two triangular signals with only negative values (V1 and V2). Essentially, V1 and V2 were in phase with V3 and V4, respectively, but voltage shifted by an amount equal to the peak value of V3 and V4. The ratio between the peak values of control signal and carrier signal gives the modulation index, $m_a = 0.813$. This modulation index was calculated from (1) to get the 230V RMS phase to neutral voltage, V_u .

Fig. 5. Implementation of sine PWM modulation in one phase-leg of the NPC and TNPC inverters

The generated gate signals along with the control signal and carrier signals from the simulation are shown in Fig. 6. The generated gate signals have coherent shapes of the theoretical gate signals shown in Fig. 2(b).

V. FPGA IMPLEMENTATION

The sine PWM modulation strategy for the NPC inverter was implemented using an Altera DE0-Nano development board. The control signals for the modulator were found by

Fig 6. NPC inverter modulator's control signal, carrier signals, and gate driver inputs of a phase-leg (simulation results)

demodulating the gate signals of a three phase bridge (3PB) inverter of Unidrive SP0401. The block diagram of this FPGA implementation for a phase-leg of the NPC inverter is shown in the Fig. 7. At first, from the 3PB gate driver a PWM gate signal is taken as an input to the FPGA. The 'control signal generator' block demodulates the input PWM to generate a sinusoidal control signal (D_a) by making two measurements using a high speed internal clock (10 MHz):

1. The time between a rising edge and the subsequent falling edge of the input PWM signal, t_H
2. The time between two consecutive rising edges of the input PWM signal, T_{PWM}

From these two quantities, D_a may be calculated as, $D_a = t_H / T_{PWM}$ and is updated on every rising edge of the input PWM signal.

Assuming the 3PB inverter is operating with a modulation index below one i.e. in linear modulation range, the control signal, D_a will vary within a range of 0 to 1. Therefore, the maximum AC amplitude of D_a can be 0.5. T_{PWM} acts as an input to the 'Carrier signals generator' block which fixes the period of the two generated triangular carrier signals, the output of this block. The amplitude of both of the triangular waves has to be 0.5 so that the modulation index of the NPC PWM signal can change with respect to the change of modulation index in 3PB inverter. The 'comparator' block then compares the control signal with the two triangular waves to generate the PWM gate-driver signals for the upper two switches of the phase leg. The 'dead time' block generates the complementary gate signals for the lower two switches with a

specific dead time. Finally, three sets of blocks shown in Fig. 7 were required for three phases.

The FPGA was programmed using Quartus II software using VHDL programming language. The sampling of the signals was done with a 10 MHz clock derived from the 50 MHz oscillator of the DE0-Nano board.

A. Control signal generator block

This block continuously tries to detect the rising edges and falling edges of the input PWM signal by comparing an existing input with the immediate last input in every clock pulse. At every rising edge of the input it initiates a counter, which determines the width of the pulse at the falling edge of the input. The same counter determines the period of the input PWM, T_{PWM} at the next rising edge. Then the duty ratios are calculated by dividing the pulse width value with the period value. However, this division will create a fixed point number ranging from 0 to 1. Therefore, to eliminate the need for a fixed point calculation, each duty ratio is multiplied by a 17 bit number 65536 (2^{16}). The duty ratio of the 3PB gate signal changes in a sinusoidal manner [14] according to equation (3).

$$D_a(t) = \frac{1}{2} [1 + m_a \sin(2\pi f_m t)] \quad (3)$$

Here m_a is the modulation index and f_m is the frequency of the control signal. During the steady state operation of induction machine connecting to the drive, m_a will be 0.813 (Section IV). So, $D_a(t)$ will be changing from 0.0935 to 0.9065 (Fig. 7). The 17 bit multiplier, 65536 will increase the accuracy between the calculated duty ratios.

B. Carrier signals generator block

The basic logic behind this block for generating triangular wave is as follows: during half of the PWM period, T_{PWM} the amplitude of one triangular wave is incremented from 0.5 to 1 and the other half of the period the amplitude is decremented from 1 to 0.5. The other voltage shifted triangular wave is found by vertically shifting the first triangular wave by 0.5. Because the control signal is multiplied by 65536, so the triangular waves are also weighted by the same number to ensure clarity in further calculations between them.

C. Comparator block

The control signal is compared with the two triangular waves to generate the gate driver signals for the upper two switches using the logic explained in Section II.

D. Dead time block

The dead time blocks produce the final NPC inverter's gate driver signals with a specific dead time between the complementary signals. There is also an enable input to this block through which all the outputs can be forced to zero.

E. Input and output safety blocks

As the input PWM signals to the FPGA are not synchronised with the FPGA clock signal, therefore, there is a possibility that the input signal transition can fall near to a clock edge, which can violate any register's timing requirements causing metastability problems. One way to mitigate the metastability problem is to add some delay to the

Fig. 7. FPGA block diagram to produce gate driver signals for one phase-leg of an NPC inverter

input PWM by adding extra register stages as the probability of metastability decreases exponentially with respect to the propagation delay [15]. For this reason 3PB PWM signals went through some D-flip-flops before they enter the 'Control signal generator' block.

Again, output NPC PWM gate driver signals could be turned on or turned off by three DIP switches on the DE0-Nano board. Another safety block was also included to check input signals before turning on the output. In total 27% of the total logic elements and 588 dedicated logic registers of the Cyclone IV FPGA were used for the design.

VI. EXPERIMENTAL RESULTS

The programed FPGA was tested by using a TGI TG5011A function generator and a modified Control Techniques Unidrive SP0401. With the function generator only single phase-leg NPC gate driver signals could be observed because of its single channel output. With the Unidrive all the twelve gate driver signals for an NPC inverter were observed.

A. Testing the modulator with a function generator

A PWM signal was generated with the function generator by comparing a 50 Hz control signal with a 3 kHz switching signal. It was put as an input to the designed modulator and four gate driver signals were found for a phase-leg of an NPC inverter. Input and output signals are shown in Fig. 8.

The results showed good coherence with the theory and simulation. The generated PWM signals also showed close to 20ms fundamental period as shown in Fig. 8, which corresponded to the 50 Hz control signal. The switching frequency of the input PWM and the frequency of the control signal were changed to different values and the output gate driver signals were observed to validate the modulator's performance at different operating conditions.

B. Testing the modulator with a Unidrive

A modified Unidrive SP0401 was used to get isolated six 3PB inverter gate signals from it using its low voltage DC operation mode. The three gate signals to the lower phase-leg switches of the 3PB inverter were used as the inputs of the FPGA modulator. A resistive divider was used to interface the Unidrive with the DE0-Nano board. It converted the 24V logic signals from the Unidrive to 3.3V logic signals, a compatible level for the FPGA input pins.

The input DC link voltage of the Unidrive was fixed to 48V for its low voltage DC operation mode. Therefore, its maximum rotational frequency setting had to be fixed to 105 rpm to ensure the gate signals were under-modulated (the open loop V/f profile could not be changed in the Unidrive).

This corresponded to an output voltage frequency of 3.5 Hz. The output NPC inverter's gate driver signals were observed for different switching frequencies (3,4,6,8,12 and 16 kHz).

Fig. 8. Modulator input from a function generator and the NPC inverter gate driving signal outputs (3 kHz switching frequency)

The gate driver signals for the upper leg switches are shown in Fig. 9 and Fig. 10 for the switching frequencies of 3 kHz and 12 kHz, respectively. Here Vg11, Vg12, Vg21, Vg22, Vg31, and Vg32 correspond to the gate driver input signals for the upper-leg switches of a three phase NPC inverter. From both figures it is clear that all the produced gate driver signals closely match the theory and simulation results. However, as the input PWMs from the Unidrive was not as clean as the PWM from the signal generator, most of the gate signals had spearing pulses at around -0.004 second in Fig. 10.

It is believed that an improved signal conditioning circuit inserted between the Unidrive and the FPGA would eliminate this problem (for these tests only a crude potential divider circuit was used to translate the 24V drive signals to 3.3V). It is likely that a dedicated level-shifting device would improve matters considerably. Alternatively, a direct tap from the Unidrive ASIC PWM outputs (which are likely 3.3V or 5V logic signals) could be used as input to the FPGA instead of the gate signals. This would have the additional advantage of removing any pulse-length distortion introduced by the gate drive circuitry, but may bypass any additional protection logic external to the ASIC.

Fig. 9. NPC inverter gate driver signals for upper-leg switches (3 kHz switching frequency)

Fig. 10. NPC inverter gate driver signals for upper-leg switches (12 kHz switching frequency)

VII. CONCLUSIONS

The design procedure of a sine PWM modulator for a NPC or TNPC inverter has been presented in this paper. The practical implementation was done using an FPGA, where the input control signals were derived from PWM gate signals of a 3PB inverter. At first, the modulation technique

was verified by simulating the NPC and TNPC inverters in National Instrument Multisim software. Then VHDL code was prepared for different blocks of the modulator. Two safety features were included at the input and at the output to ensure its proper operation. The gate driver signals generated from the FPGA matched closely with the simulation results and theoretical predictions.

The study concluded with the production of proof-of-concept hardware demonstrating that the existing Unidrive design can be modified to extract the required PWM signals and that these signals can be practically re-modulated to drive an NPC output stage. One application of this modulation technique would be comparing the performance of an identically rated two-level 3PB inverter with a three-level NPC or TNPC inverter where both of them would use the same control loop.

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