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Azzouz Sellai
Piotr Kruszewski
Abdelmadjid Mesli
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Azzouz Sellai,^a Piotr Kruszewski,^{b,c} Abdelmadjid Mesli,^c
Anthony R. Peaker,^d and Mohamed Missous^d

^aSultan Qaboos University, Physics Department, 123 Muscat, Oman
asellai@squ.edu.om

^bInstitute of Physics Polish Academy of Sciences, 02-668 Warsaw, Poland

^cAix-Marseille University, IM2NP, UMR 6242 CNRS, 13397 Marseille Cedex 20, France

^dUniversity of Manchester, Microelectronics and Nanostructure Group,
School of Electrical and Electronic Engineering, United Kingdom

Abstract. GaAs based structures in which are embedded InAs self-assembled quantum dots are studied using admittance measurements taken over a large frequency spectrum and for several temperatures. The presence of quantum dots is evidenced in the capacitance-voltage characteristics by one, or more, plateau-like structures related to the processes of charging and discharging of the quantum dots. Concurrently, the measured conductance exhibits a peak in a certain bias range that coincides with the plateau-like structure in the capacitance but only for temperatures below 150 K. The conductance dependence on both the temperature and applied bias is attributed to two mechanisms of carrier escape/capture mechanisms from the InAs embedded quantum dots into/out of the hosting GaAs; a thermally activated process for temperatures above 80 K and a perceptibly nonthermal tunneling process for temperatures below 40 K. The conductance data is used to estimate rates and activation energies in association with the electron escape mechanisms from the quantum dots. © 2012 Society of Photo-Optical Instrumentation Engineers (SPIE). [DOI: 10.1117/1.JNP.6.063502]

Keywords: self-assembled quantum dots; admittance spectroscopy; capacitance-voltage characteristics; frequency and temperature dependence; electron capture rates.

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1 Introduction

Research into new electron devices of better quality and higher performance has intensified over the years in response to an increasing demand by designers of future systems in various fields of electronics and photonics. The tremendous advances in epitaxial growth techniques such as metal-organic chemical vapor deposition (MOCVD) and molecular beam epitaxy (MBE) allowed the fabrication of high-quality materials with the precise handling, control, and tailoring of growth parameters leading to newly engineered classes of devices based specifically on low-dimensional semiconductor structures. The ultimate electron and hole confinement in zero-dimensional semiconductor structures, namely quantum dots (QDs), results in new phenomena and unique properties that are interesting from the perspectives of both fundamental physics as well as device applications. It is particularly established that the use of QDs could lead to substantially improved performance in many aspects of photonic devices. In this respect, high-performance semiconductor lasers and optical amplifiers with QDs in their active region have been fabricated and are already in the commercialization stage.^{1,2} The use of QDs in multi-junction solar cells as an approach to enhance the solar cell efficiency has also been investigated and shown to be a promising alternative.^{3,4}

Knowing that QDs can be considered as multiple charge donors or acceptors with the possibility of carrier exchange (emission and capture) between QD quantized levels and the conduction band of the hosting semiconductor, a clear and detailed grasp of the electronic properties of the QDs and the processes of carrier exchange with the material in which these QDs are embedded is crucial to a proper understanding of the operation of envisaged QD-based devices.

In this context, we have studied some electronic properties of InAs QDs embedded in a GaAs structure using frequency and temperature dependent admittance. In particular, capacitance-voltage (C - V) and conductance-voltage (G - V) are used to examine qualitatively and quantitatively the electron states and charging mechanisms of self-assembled InAs QDs embedded in a GaAs structure. While most of the published studies on similar systems concentrate mainly on the C - V measurements, the emphasis here is on the conductance data, which is found to be more sensitive to some aspects of carriers exchange mechanisms and permits acquiring additional information that could not be accessed through capacitance measurements alone.

2 Device Fabrication and Characterization

The layers structure of the diodes under investigation is illustrated in Fig. 1. The structures were grown by MBE on a (100) n^+ GaAs substrate, with no miscut angle, followed by a 170 nm Si-doped (2 to $5 \times 10^{18} \text{ cm}^{-3}$) GaAs layer, then an approximately 400 nm-thick layer of Si-doped ($2 \times 10^{16} \text{ cm}^{-3}$) GaAs, a thin layer of InAs consisting of either a wetting layer (WL) followed by self-assembled QDs or a WL alone (as a reference sample) sandwiched between two undoped 5 nm spacer layers and finally another 400 nm-thick layer of Si-doped ($2 \times 10^{16} \text{ cm}^{-3}$) GaAs on the top. The undoped 5 nm spacer layers are used to separate the doped GaAs regions from the QD layer in order to avoid diffusion of impurities into the QDs during growth. Detailed growth conditions were given in Refs. 5 and 6. The growth conditions resulted in a QD density of approximately $3 \times 10^9 \text{ cm}^{-2}$ as revealed from both AFM imaging and deep level transient spectroscopy measurements.^{5,6} The top Schottky contacts of various diameters (200, 300, 350, 400, and 500 μm) were formed by evaporating Au-Ti through a shadow mask. The conventional Ohmic contact at the back of the substrate was fabricated with a AuGeNi alloy annealed at 450 $^\circ\text{C}$ for 2 min.

Fig. 1 Structure under study consisting essentially of a 2.8 ML of self-assembled QDs embedded in GaAs.

The samples were mounted on TO5 headers inside a cryostat, the temperature of which is varied using a helium-based closed cycle refrigeration system and a wire heater under the control of a Lakeshore temperature controller. The temperature can be measured to accuracies better than 0.5 K. The C - V and G - V measurements were performed over the temperature range 15 to 300 K at several frequencies between 50 kHz and 1 MHz using a HP4192 Impedance Analyser. The current-voltage (I-V) measurements were carried out using a Keithley 2400 Source-Meter.

3 Results and Discussion

To check the diodes quality, DC I-V measurements were performed at various temperatures. A sample of these measurements is shown in Fig. 2, from which it is clear that the diodes exhibit a rectifying behavior with the current being to some extent thermally activated more noticeably in the forward bias region. The reverse I-V characteristics did not evidently disclose any particular behavior that might be linked to the presence of QDs. The forward characteristics, which are obviously more relevant to the conduction processes at or close to the top metal-GaAs interface, are not a primary concern in our present study. It is, however, worthwhile mentioning that a closer look at these forward I-V characteristics reveal, at any given temperature, two distinct behaviors depending on the bias range (indicated by region I and region II in the inset of Fig. 2). Preliminary analyses of the forward I-V-T data, assuming the customary thermionic emission conduction model, lead to Schottky diode parameters that are nonphysical in region I, a likely indication of the inadequacy of the assumption that thermionic emission might be the dominant conduction process. Region II, however, yielded ideality factors, barrier heights, and saturation currents that show typical variations with temperature, well in line with results pertinent to Schottky contacts routinely reported in literature.⁷⁻⁹ Namely, the ideality factor increases with decreasing temperature while there is a decrease with decreasing temperature of both the barrier height and saturation currents. These variations are shown in Fig. 3 and could well be explained on the basis of a modified thermionic emission conduction mechanism that takes into account other contributions, such as thermally assisted tunneling as well as eventual potential barrier inhomogeneities.¹⁰⁻¹² Proper and detailed analyses of the I-V-T data both in its reverse- and forward-bias regimes could be the subject of a separate publication.

Typical measured C - V and G - V characteristics at a given frequency and temperature are shown in Fig. 4 for samples with a 2.8 ML of QDs or with just the WL (without any QD formation).

In the structure under investigation, the depletion region at zero bias is smaller than the distance between the top interface and the plane where the InAs QDs or WL are located, and as

Fig. 2 Measured DC I-V characteristics for the sample with QDs shown at three temperatures with an inset more clearly showing the forward bias region.

Fig. 3 Obtained ideality factors and barrier heights from the forward DC I-V data at different temperatures.

Fig. 4 The measured C - V and G - V characteristics at a frequency of 1 MHz for the samples with and without QDs.

such, the QDs are outside the depletion region and filled with electrons. By applying a reverse bias that extends the depletion zone to include the QDs layer and beyond allows changing the occupancy of the QDs. Electrons then start to be emitted from the QDs with given rates that depend on the escape mechanism. This will influence both the measured C - V and G - V characteristics. In fact, the presence of QDs is evidenced in the C - V characteristics at all temperatures and frequencies considered here by a plateau-like structure in the bias range -3 to -2 V that is related to charging and discharging of QDs. Concurrently, the G - V characteristics clearly show a manifest peak in the same bias range at all considered frequencies but only for temperatures below 150 K. In contrast, under the same measurement conditions, the samples with only the WL show complete absence of both the plateau-like structure and the peak in their respective C - V and G - V characteristics.

The C - V characteristics, including the well-defined plateau-like structure, can be explained as follows: for applied voltages between 0 and -1.5 V, the QDs are outside the depletion region and do not contribute to the measured capacitance. As the voltage reaches $U = -2$ V, the depletion region includes the QDs and, provided the temperature is low enough to avoid emptying the QDs, the capacitance reaches a plateau and stays constant up to about $U = -2.5$ V. A further increase in the applied voltage causes the capacitance to be solely due to the contribution from the bulk GaAs.

Also noted was the absence of any hysteresis in the measured admittance data with respect to the applied voltage, suggesting that the processes of filling and emptying (carrier capture and emission) of the QDs have the same influence on the measured admittance.

The C - V data could be used to calculate the carrier concentration profile, namely the carrier density (N) versus the edge of the depletion width (W) using the standard relations:¹³

$$N(W) = \frac{-2}{q\epsilon_0\epsilon_r} \left[\frac{d(\frac{1}{C})}{dV} \right]^{-1} \quad (1)$$

and

$$W = \frac{\epsilon_0\epsilon_r A}{C} \quad (2)$$

Here ϵ_0 and ϵ_r represent the permittivity of vacuum and the relative permittivity of GaAs, respectively, and A is the contact area.

The plateau-like structure in the C - V plots is converted to a prominent peak in the calculated concentration profiles $N(W)$ as shown in Fig. 5. The peaks in these concentration profiles correspond approximately to the position ($0.42 \mu\text{m}$) of the QD plane and are due to carrier accumulation in the QDs.

It has to be noted here that the accuracy in determining the carrier distribution throughout the structure is limited by the Debye length.^{13,14} In fact, the assumption in the calculations of $N(W)$ of a sharp edge between the depletion and neutral regions is not exact since the electric field does not vanish at the very edge but penetrates effectively over a few Debye lengths in the neutral region. An increment dV in the voltage causes a majority carrier density $dN(W)$ that does not sample $N(W)$. This increment is not locally located at W but spreads over a distance equal to at least one Debye length. Consequently, the measured capacitance does not define the width of the space charge layer better than this distance.

There are a couple of points to be highlighted with respect to the temperature variation of $N(W)$ shown in Fig. 5. First the peak, which is directly related to occupancy of charge states, increases as the temperature is decreased with a concomitant reduction of broadening of the profile. Second, in the low temperature regime, below 40 K in particular, a second peak appears consistently at a slightly higher depletion width of $\sim 0.48 \mu\text{m}$. This second peak, the magnitude of which is perceptibly independent of temperature below 40 K, becomes more prominent than the first one as the temperature is decreased further.

The temperature dependence of the peak in $N(W)$ and the appearance of the second peak at low temperatures can be directly linked to the temperature dependence of both the Fermi level and of the electron density in the InAs QDs. The latter was shown to saturate¹⁵ at

Fig. 5 Examples of calculated concentration profiles from C - V data at various temperatures ($f = 1 \text{ MHz}$).

temperatures below 80 K, stemming from the fact that the negative charge accumulating in the QDs plane causes a repulsive Coulomb potential and the subsequent formation of a space charge region, the width of which increases with the increase in the electron density in the plane of the QDs.

In line with the interpretation of Brounkov et al.,¹⁶ the thermionic emission rates of electrons from the QDs are much lower at very low temperatures. Consequently, electrons are no longer able to follow the applied ac signal leading to their freezing in the QD levels. Electrons can then only escape by tunneling under a higher applied electric field. This process is responsible for the appearance of a second peak in $N(W)$ at a higher reverse bias (a larger depletion width as shown in Fig. 5) for temperatures below 40 K in particular.

Moreover, we have systematically investigated the variations of conductance with both temperature and frequency since the conductance is known to be more sensitive to some aspects of carriers exchange mechanisms and, as such, permits acquiring additional information that cannot be accessed through capacitance measurements alone.

The global variations of conductance with both the temperature and applied bias, given by the 3-D contour plot of Fig. 6, show two regions of maximum conductance in the voltage range -3 to -2 V and for two temperature ranges 50 to 90 K and below 50 K.

The peak in the G - V characteristic can be seen as a signature of resonant carrier emission/capture between the InAs QDs and the matrix GaAs in which they are embedded. As the reverse bias is changed, the QD states are alternatively emptied or filled by the application of the 15 mV ac signal. When the rate of carrier emission or capture coincides with the frequency of the applied ac signal, a resonance condition occurs, leading to a maximum in the conductance.

With respect to the temperature dependence of the peak magnitudes of the concentrations, we unambiguously observed two different behaviors depending on the temperature range: for temperatures above 80 K, the concentration peak height decreases with increasing temperatures while it decreases, although only slightly, with decreasing temperatures below 80 K. Besides, below 40 K, the temperature dependence is significantly much less pronounced and barely noticeable. These observations concur for the fact that one of two different mechanisms of carrier escape from the QDs prevails over each temperature range; a thermally activated mechanism for temperatures above 80 K and a much less temperature dependent process at a temperature of 40 K and below. This latter observation is in line with previous findings that the thermal activation of electrons is negligible in the very low temperature range and the carrier exchange (charging and discharging) between the QDs and the bulk GaAs is governed essentially by a tunneling process.

The frequency dependence of the peak in the measured admittance could be related to capture and emission rates of electrons in the QDs. And to elucidate this point further, we have investigated the frequency dependence of both $N(W)$ and $G(V)$ in the low temperature range (below

Fig. 6 Variations of conductance with both applied bias and temperature, showing two regions of maximum conductance in the voltage range -3 to -2 V and two temperature ranges; the measurement frequency is 1 MHz.

60 K). It was observed that the peak in $N(W)$ increases, although only slightly for the frequency range considered, with decreasing frequencies which is in concordance with the interpretation above.

In contrast, the measured conductance at any given temperature shows (Fig. 7) a very significant increase with increasing frequency. Knowing that at a fixed temperature G is directly proportional to $\omega^2\tau/(1 + \omega^2\tau^2)$, with $1/\tau$ being the emission rate of carriers,^{17–19} the observed behavior of conductance with frequency suggests that the emission rates are much higher than the frequency of the applied ac measurement signal ($\omega\tau \ll 1$). This apparent inconsistency between the behaviors, with respect to frequency, of $N(W)$ (based on C - V data) and G - V needs to be elucidated further.

Examining more closely its temperature variations at a fixed applied bias, the conductance exhibits a peak at a certain maximum temperature (Fig. 8) at all considered frequencies (100, 200, 400, 600, and 800 kHz, and 1 MHz), with the maximum temperature being slightly shifted to lower values as the applied bias increases. The preliminary analysis of this spectroscopic data could be used to extract thermionic emission rates and activation energies in association with the electron thermally activated escape mechanism from the QDs. Starting from the fact that QDs can be considered as carrier traps with the possibility of carrier emission and capture between QD quantized levels and the Fermi level and noting that from this aspect standpoint, the issue is not fundamentally different from the case of interface traps known for a long

Fig. 7 The effect of frequency on the measured G - V characteristics at a given temperature (here $T = 70$ K).

Fig. 8 Typical variations of the conductance with temperature at 1 MHz and for various bias voltages.

Fig. 9 Arrhenius plot of the derived emission rate versus temperature at a voltage of -2.68 V (used to get the activation energies).

time in metal insulator semiconductor (MIS) or metal oxide semiconductor (MOS) structures. As such, the equations derived by Nicollian¹⁸ relating the conductance to the traps density and their time constant (τ) should be valid to obtain the carrier emission rates in relation to exchanges between the QDs and the host semiconductor. It is known^{18,20} that the maximum in (G/ω) in this instance occurs at $\omega\tau = 1.98$ from which the emission rate, defined here as $e_n = 1/\tau = \omega/1.98$, can be obtained. A similar expression ($e_n = \omega/2$) was derived in the appendix of Ref. 17 by considering the transient response of the electron population of a QD level to a small ac applied voltage. Observing (Fig. 8) that at each given voltage the maximum in G corresponds to a temperature $T_{\max}$, it is possible to obtain all the $T_{\max}$ values corresponding to all considered frequencies, and hence emission rates $e_n = \pi f$. The plot of $e_n/T_{\max}^2$ versus $1/T_{\max}$ of Fig. 9 then follows. Knowing that the emission rate of a thermally activated process is given²¹ by $e_n = \gamma T^2 \sigma \exp(-E_A/k_B T)$, where γ is a temperature-independent constant and σ is the capture cross-section, the activation energy E_A could be derived from the slope of the $e_n/T_{\max}^2$ versus $1/T_{\max}$ semi-logarithmic plots. These analyses yielded emission/escape times that are slightly above 10^{-6} s, with activation energies in the range 55 to 60 meV.

4 Conclusion

In conclusion, we have investigated the C - V and G - V characteristics, and their dependence on temperature and frequency, of a Schottky structure in which InAs self-assembled QDs are embedded in GaAs to reveal some of the properties related to carrier exchange between the QDs and the host GaAs. The effects of embedding the QDs in the structure are evidenced, depending on temperature, by one or two peaks in the calculated concentration profiles based on the measured C - V data as well as by a peak in the concomitantly measured conductance with a peak magnitude that is clearly frequency dependent at a given temperature. Moreover, depending on the temperature regime, two mechanisms seem to govern the exchanges between the InAs QDs and the GaAs matrix. The process above a temperature of 80 K is thermally activated while a non-thermal tunneling process seems to dominate at temperatures below 40 K. Finally, the emission rates and activation energies relevant to these processes were estimated from the conductance data.

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Azzouz Sellai graduated from Constantine University, Algeria in 1986, received his PhD degree in electronic engineering (resonant tunneling devices) from Nottingham University, UK in 1991. He spent few years as a postdoc at Queen's University of Belfast, School of Physics working on surface plasmon enhanced infrared detectors. He is now associate professor of physics at Sultan Qaboos University, Oman. His research interests are electrical and optical characterization of semiconductors in general. He is the author or co-author of over 60 publications in refereed journals and conference proceedings. He is a senior member of the IEEE.

Piotr Kruszewski graduated and received a PhD in solid state physics in 2010 at the Institute of Physics, Polish Academy of Sciences in Warsaw, Poland. He is now working as postdoc at the Institut Matériaux Microélectronique Nanosciences de Provence in the group of defects and nano-objects, which is a part of CNRS laboratory and Aix Marseille University. His current research interests are defects in semiconductors, wide band gap materials, and low dimensionality systems studied by DLTS-related techniques.

Abdelmadjid Mesli graduated from the University of Strasbourg, France and received his state doctorate in 1998. He is now director of research at Centre National de Recherche Scientifique (CNRS). His current research interests deal with charge and spin transport in semiconductors both at the macroscopic and nanometric scale with a special emphasis on the role of point defect. He has authored more than 100 papers and communications and launched about 30 collaborations with both national and foreign laboratories and institutes.

Mohamed Missous is a fellow of the Academy of Engineering and the Institute of Physics and a senior member of the IEEE. He is a professor of semiconductor materials and devices at the University of Manchester. Over the years he has concentrated, with considerable success, on establishing practical approaches and techniques required to meet stringent doping and thickness control, to submonolayer accuracy, for a variety of advanced quantum devices, from room temperature operating midinfrared quantum well infrared photodetectors to Terahertz materials for 1 μm imaging. He has a proven track record of technology transfer and a strong feature of his work is the close industrial involvement he maintains with the leading players in the microwave and optoelectronics fields. Examples of these include the design and MBE growth of graded gap Gunn diodes for e2v Ltd for use in Intelligent Cruise Control systems in cars at 77 GHz, with fully working devices fitted in BMW and Audi cars. He is developing technologies for the international Square Kilometre Array (SKA) radio telescope, which involves the design and fabrication of super low noise receivers and super fast analogue to digital converters using advanced InP technologies.