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Effects of three-dimensional electric-field coupling on a side-gated nanotransistor

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Abstract

Using a two-dimensional (2D) ensemble Monte Carlo method self-consistently coupled with three-dimensional (3D) Poisson equations, a two-dimensional electron gas (2DEG)-based planar nanodevice, or a side-gated nanotransistor (SGT), is analyzed. Compared with the previous entirely 2D simulations, the extra inclusion of a 3D electric-field solver has allowed for a quantitative study of electric-field coupling beyond the active layer (2DEG). Our results show that the device characteristics are very sensitive to not only the depth of insulating trenches into the device substrate but also a change in dielectric layers on the device surface. A coating of a dielectric thin film with a thickness of only 5 nm on the device surface is enough to significantly enhance the current. Also continuously increasing the distance between a dielectric layer and the SGT surface results in an exponential decrease in the source–drain current. Moreover, the dependence of the source–drain current on the dielectric thickness is non-monotonic. The current presents a peak when the dielectric thickness is about 150 nm and then reduces to a saturated state when the dielectric thickness is more than 300 nm. We discuss these effects in terms of the special geometric structure and working principle of the SGT.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Progressive miniaturization of semiconductor devices has in the past decades led to high-speed operations and large-scale integrations of electronics. A single silicon chip is now able to contain over a billion transistors and operate at GHz frequencies. With further miniaturizing semiconductor devices down to the nanoscale, a large number of novel effects, which are negligible in larger semiconductor devices, are exploited to demonstrate novel electronic device concepts. Among the examples are the single electron-transistor (SET) [1–3], the ballistic rectifier [4, 5] and the three-terminal ballistic junction [6–8].

At the same time, planar device architecture is also introduced to complement the conventional vertical one. In planar devices, electrodes are connected side by side to the active semiconductor layer rather than being placed on top of each other, as in conventional multilayered

vertical-structured devices. As such, very low parasitic capacitances are attainable, resulting in a very high operating speed. Planar nanodevices based on two-dimensional electron gases (2DEGs) in semiconductor heterostructures have been demonstrated for operations at tens of GHz or above [9–12]. In particular, self-switching diodes (SSDs) have been shown to have a zero threshold voltage and be able to rectify microwave signals up to 110 GHz at room temperature and up to 2.5 THz at a temperature of 150 K [11, 13].

Apart from the experiments on planar nanodevices, there has been theoretical work to further understand the device operations. An analytical model has been first introduced followed by more sophisticated models based on ensemble Monte Carlo (EMC) methods [14–16]. The EMC simulations do not only obtain good agreement with experiments but also predict additional features of the planar devices, such as very low noise spectra in the THz range and enhanced THz detections by plasma [16–21]. However, the entirely 2D EMC

methods used in previous work are unable to directly deal with electric-field coupling beyond the 2DEG layer.

In this work, a 2D–3D combined EMC method has been developed, so that 3D electric-field coupling on the device performances can be studied in detail. The paper is structured as follows. In section 2, the structure and working principle of the side-gated nanotransistor (SGT) are firstly introduced and then the 2D–3D combined EMC model is described. In section 3, electric-field coupling through the substrate is studied by simulating devices with a different depth of insulating trenches. After making sure the influence of trench depth on the device performances, the characteristics of the SGT are also studied. In section 4, efforts are devoted to discussing the effects of dielectric layers on the SGT and the corresponding potential applications. Finally, the conclusions of this work are summarized in section 5.

2. Device working principle and Monte Carlo model

Figure 1(a) shows schematically the top view of a planar nanodevice, named the SGT. The device is based on an $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{In}_{0.53}\text{Al}_{0.47}\text{As}$ heterostructure, where a 2DEG with a carrier concentration of $1.0 \times 10^{12} \text{ cm}^{-2}$ is formed at the hetero-interface 50 nm below the device surface. The L-shaped insulating trench (LSIT) and the U-shaped one (USIT) are etched through the 2DEG layer, which ensures that electrons have to pass through the narrow channel between the two trenches in order to conduct a current between the left (source) and right (drain) terminals. Such a SGT combines functionalities of a diode and lateral gate transistor [22]. Using fixed zero or negative gate bias, the SGT works as a diode. When a negative voltage is applied to the right terminal, the induced negative charges around the LSIT deplete the channel, impeding the current flow, thus switching the device off. However, when a positive voltage is applied to the right terminal, the induced positive charges around the LSIT attract electrons into the channel for the current to flow easily. This leads to diode-like characteristics, as demonstrated experimentally [22]. Although the source–drain current–voltage characteristic of a SGT is similar to the current–voltage characteristics of a p–n junction or a Schottky barrier diode, it is based on neither a doping junction nor a tunneling barrier, i.e. no built-in electric field along the current direction. As such, the threshold voltage could be made to be zero, ideal for microwave applications. If used as a transistor, a SGT may provide two different characteristics, depending on the sign of the source–drain voltage, V_{SD} [22].

It is noteworthy that an advanced fully 3D EMC method has been developed to study three-terminal T-branch junctions (TBJs) in detail [23–25]. The advantage of such a 3D simulator over a 2D one is that it is able to accurately model complex geometrical devices, such as TBJs with a gate terminal. But in many other cases, in spite of minimizing the need for parameter fitting and including the effect of electron transfer from the channel to other layers, the 3D model leads to almost the same results as those obtained from the 2D model [26]. Moreover, in order to overcome huge time consumption, the EMC domain of 3D simulation should be limited to a small region.

Figure 1. Schematic top view (a) and side view (b) of the simulated SGT (not to scale). The gray areas and the white area in the top view represent insulating trenches and 2DEG, respectively. An interface of $\text{In}_{0.53}\text{Al}_{0.47}\text{As}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ heterostructures in (b) is just 50 nm below the device surface, at which a sheet of 2DEG forms.

In this work, the three dimensions of the EMC domain are all in the order of micrometers (see figure 1 for details). For not significantly increasing the simulation time and being able to do a more accurate modeling, a 2D–3D combined model is developed from our entirely 2D EMC model, which has been successfully used in earlier work [19–21, 27]. This model is based on a semi-classical 2D EMC method [28] self-consistently coupled with 3D Poisson equations. In this model, we assume that all electrons are well confined within the 2DEG layer, ignoring the effect of electron transfer from the channel to other layers, so that the 2D EMC method is enough to depict the micro behavior of the electrons in the device. By summing the micro information (such as position) of each electron, macro electronic properties (for example, the distribution of electron density) of the device can be obtained. In order to update the electric field in the device, which changes with the transportation of the electrons, the distribution of electron density in the 2DEG layer is calculated in $5 \times 5 \text{ nm}^2$ meshes at each time step of 1 fs. Since all the electrons are confined in the 2DEG layer, the distribution of electron density throughout the device is also known. Then we are able to solve the 3D Poisson equations to obtain the electric field within the 2DEG layer, which is required by the next step of 2D EMC simulation. By using the finite difference scheme, the solution of the 3D Poisson equations can be obtained by solving the linear systems of equations,

$$Ax = b, \quad (1)$$

where A is an $n \times n$ matrix for dielectric coefficients and b is an $n \times 1$ vector for electron densities. Then the unknown electric potentials in the device can be calculated by

$$x = A^{-1}b, \quad (2)$$

where $\mathbf{A}^{-1}$ is the inverse matrix of $\mathbf{A}$. Usually equation (2) is not preferred during solving equation (1), since the calculation of $\mathbf{x}$ using it is time consuming. However, in our case, the calculation time can be significantly reduced for the following two reasons. First, what we need are the electric potentials within the 2DEG layer, so that only a small part of $\mathbf{x}$ should be calculated. Secondly, the electrons are all confined in the 2DEG layer, so that the vector $\mathbf{b}$ possesses a lot of unchanged entries. Once the calculation related to these unchanged entries has been performed, the calculation results can be stored for using at each time of electric-field updating. Supposing that the calculation domain along the direction perpendicular to the 2DEG layer is divided into m meshes for solving the 3D Poisson equations, the calculation time of equation (2) can be reduced almost by a factor of $(m-1)^2$. Moreover, the memory needed for $\mathbf{A}^{-1}$ is also reduced by a factor of $(m-1)^2$. This means that, from the calculation point of view, a 3D problem is degenerated into a 2D one.

Upgrading the electric-field solution from 2D to 3D enables us to quantitatively study the effect of electric-field coupling through the substrate and beyond the device surface on the nanodevice performances. Figure 1(b) shows schematically the side view of the simulated SGT. In order to properly study the 3D electric-field coupling, Poisson equations are solved in a domain beyond the geometric structure of the SGT. As one can find from figure 1(b), a volume with a height of $1\ \mu\text{m}$ above the device surface is also included. The dielectric constants used in the simulations for air, $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ and $\text{In}_{0.53}\text{Al}_{0.47}\text{As}$ are 1, 13.88 and 11.4, respectively. In order to model the influence of surface states at the semiconductor–air interface, a uniform negative charge density, $N_S = 0.35 \times 10^{12}\ \text{cm}^{-2}$, is also added at the edge of the insulating trenches during the simulations. Geometric parameters of the simulated SGT can be found in figures 1(a) and (b). In order to obtain an obvious diode-like characteristic of the SGT, we ensure the width of the USIT being wider than that of the LSIT [29]. All simulations are carried out at room temperature, with the left terminal grounded.

3. Electric-field coupling through substrate and device performances

As mentioned earlier, the insulating trenches of the SGT are required to pass through the 2DEG, so that any trenches with a depth more than 50 nm are all eligible. It seems that the exact value of the trench depth is not needed during device fabrications. However, this may not be true if the electric-field coupling through the device substrate cannot be ignored.

In order to analyze the effect of electric-field coupling through the device substrate, SGTs with different trench depths are simulated. Since the dielectric constant of the trenches is different from that of the substrate, deepening the insulating trenches will change the dielectric distribution of the substrate and then the electric-field coupling through the substrate. During these simulations, the gate is biased with a voltage of 0.3 V and the right terminal is also grounded. Under these conditions, only the electric-field coupling through the substrate will change with the trench depth, resulting

Figure 2. Average electron density in the nanochannel versus the depth of insulating trenches, when the left and the right terminals are both grounded and the gate is biased with a voltage of 0.3 V.

in a corresponding change of the electron density in the nanochannel.

Simulation results, average electron density in the nanochannel versus depth of insulating trenches, are shown in figure 2. One can find that the deeper the insulating trenches, the lower the average electron density, implying weaker electric-field coupling through the device substrate. Moreover, the phenomenon that the reduction of the electron density can be up to about 50% strongly suggests the importance of electric-field coupling through the device substrate. We also find that the change of the electron density is saturated when the trenches are more than 400 nm in depth. Since the 2DEG is 50 nm below the device surface, we obtain that the effective depth of electric-field coupling through the device substrate is about 350 nm. The above results tell us that the fluctuation of the trench depth will strongly change the device performances. This may become more serious for circuit applications. To avoid this effect, the depth of the insulating trenches should be more than a special value, which is 400 nm in our case. In the following studies, all insulating trenches are ensured to be more than 400 nm in depth.

Figure 3 shows simulated source–drain current–voltage characteristics of a SGT sketched in figure 1, with different fixed-gate biases V_G . The green dot curve in figure 3 represents zero gate bias, showing a threshold voltage of 0.5 V. Beyond the threshold voltage, the source–drain current increases dramatically. Such a threshold voltage can be adjusted through the gate bias V_G . As shown in figure 3, positive gate bias reduces the threshold voltage (blue asterisk or pink circle curve) and negative one increases it (red triangle curve). By carefully adjusting the gate voltage, the threshold voltage can be tuned to be virtually zero (pink circle curve), ideal for microwave applications. Below the threshold voltage, the channel is closed, so that the source–drain current can become zero. This is true supposing that the drain voltage is small. When a large negative drain voltage is applied, leakage current emerges. This leakage current is also gate-voltage correlative, i.e. the higher the gate voltage the larger the leakage. Obviously, the increase in gate voltage degrades the diode-like characteristics of a SGT, indicating that at large positive gate biases, a SGT provides only one characteristic. The above results are similar to those obtained experimentally

Figure 3. Current–voltage characteristics of the SGT shown in figure 1 with different gate biases $V_G = -0.3$ V (red triangle curve), 0.0 V (green dot curve), 0.3 V (blue asterisk curve) and 0.6 V (pink circle curve).

or by using an entirely 2D method in the previous works [22, 29].

4. Effects of dielectric layers on the SGTs

Apart from modifying the diode-like characteristics of a SGT by gate bias, one can also adjust them by changing the electric-field coupling through altering the channel width, the insulating trench width or even the dielectric constant of the trenches [16, 20, 22]. Other than these in-plate coupling studies, we focus on quantitatively studying the effect of electric-field coupling beyond the device surface on the device performances in this section. Figure 4 shows the influence of dielectric layers on the source–drain current of the SGT sketched in figure 1. As shown in figure 3, the device working around threshold voltage has strong nonlinearity, so that it may be more sensitive to the change of physical or geometric parameters. As such, all simulations shown in figure 4 are carried out at a threshold voltage of $V_{SD} = 0.5$ V. For making a convenient comparison, all the data are normalized to the source–drain current of the SGT without any dielectric layer coating on its surface.

The red triangle curve in figure 4 is obtained when the gate is zero biased and it shows the source–drain current of the SGT when thin films (dielectric constant $\epsilon_r = 12$) with different thicknesses are coated on the device surface. One can find that with the growth of the thin-film thickness, the current increases dramatically and even doubles when the thin-film thickness is only 5 nm. Moreover, the response of the current with the growth of thin-film thickness is non-monotonic. The current presents a peak when the thin-film thickness is about 150 nm and then reduces to a saturated state when the thin-film thickness is beyond 300 nm. Since the device performances are very sensitive to the thin-film thickness, such a SGT may be useful for measuring dielectric thickness or monitoring the thickness change of the dielectric layer in nanoscale.

The above non-monotonic phenomenon should come from an interaction between the gate-controlled field effect and drain-controlled field effect. As shown in figure 1(a), a 50 nm wide channel is formed between a USIT and an LSIT. Thus, the electron density in the nanochannel can be regulated by the electric-field potential of the USIT or the LSIT, which

Figure 4. Effects of dielectric layers ($\epsilon_r = 12$) on the source–drain current of the SGT with a source–drain voltage of 0.5 V. All the data are normalized to the source–drain current of the SGT without any dielectric layer coating on its surface. The red triangle and green dot curves show thin-film thickness versus the current responses of the SGT with zero gate bias and without gate bias, respectively. The blue asterisk curve shows the source–drain current of the SGT without gate bias versus the position of a dielectric layer (distance between a dielectric layer and the SGT surface).

are controlled by the gate voltage and the drain voltage, respectively (see section 2 for detailed discussions). In our simulations, the gate is zero biased and the drain is applied with an electric potential of 0.5 V, so that the nanochannel feels two field effects. One is controlled by gate through the USIT and the other by drain through the LSIT. We know that the electric-field potentials along the nanochannel range from 0 to 0.5 V, so that the USIT-to-channel voltages are always negative and the LSIT-to-channel voltages are always positive. Negative voltage depletes the channel, making it difficult for the current to flow and positive one attracts electrons into the channel for the current to flow easily. These two field effects are opposite and would compete with each other.

The coating of a dielectric thin film on the SGT surface increases both the USIT-to-channel and the LSIT-to-channel capacities. But the difference of trench widths (20 nm for LSIT and 50 nm for USIT) leads to an inconsistent capacity increment with the growth of thin-film thickness. Keeping in mind that the gate- and the drain-controlled field effects have opposite effects on the flow of the channel current, a current peak can be expected at which the increment of capacity related to the LSIT is the same as that related to the USIT. After that, the increment of capacity related to the LSIT drops below that related to the USIT, so that the current reduces. With the further growth of thin-film thickness to be more than 300 nm, the increments of capacity related to the LSIT and the USIT are both saturated and then the current no longer changes, indicating that an effective thickness for 3D electric-field coupling beyond the device surface is about 300 nm. Since the 2DEG is 50 nm below the device surface, this effective thickness agrees with the effective depth mentioned in the previous section.

To confirm the above explanation of the non-monotonic phenomenon, a SGT without gate bias is also simulated. Under such a condition, the influence of gate voltage is eliminated and the nanochannel feels only one-field effects. The green dot curve in figure 4 shows the simulation results. One can find

that the current peak exactly disappears and the curve shows a monotonic increase.

Moreover, the blue asterisk curve in figure 4 is also obtained when the gate is without bias. The current peak also does not present itself. This blue asterisk curve shows source–drain current responses of a SGT versus the distance between a dielectric layer and the SGT surface. In these simulations, the dielectric constant for the layer is 12 and the layer thickness is assumed to be 1000 nm, much larger than the effective thickness of the 3D electric-field coupling, excluding the effect of the layer thickness. One can find that when the distance between the dielectric layer and the device surface is too large, the source–drain current is hardly affected by changing the distance. However, when the distance is less than 100 nm, the change in the distance results in a dramatic increase or decrease in the source–drain current. Since such a nanometer device is sensitive to the position of the thin film, it may be useful to know the exact location.

The above extreme sensitivity of device performance to the changes of the dielectric thin film comes from the following two facts. First, the device is based on the 2DEG, which is a 2D conducting material. Unlike the 3D conducting material in vertical devices, the surface-to-volume ratio of such a 2D material is so large that much electric field leaks from its surface. At the same time, the 2DEG is embedded below the device surface with a depth of only 50 nm, which is too thin to efficiently confine the leaking electric field within the device. As a result, powerful 3D electric-field coupling beyond the device surface can be expected. Secondly, the device performances are based on electric-field coupling, with a strongly nonlinear response near the threshold voltage. In our studies, the devices are all working at the source–drain threshold voltage of 0.5 V and, thus, fully exploit the effect of electric-field coupling on device performances.

It is worth noting that such planar nanodevices can work in the THz range, so that the SGT may be applied for counting the number or recording the motion of dielectric nanoparticles at a very high speed. Moreover, being a planar device, the SGT can be easily integrated with other planar devices in a single step of nanolithography without the need for interconnect [11, 13]. For example, one can integrate a SGT with SSDs, whose possibilities for microwave detection and emission have been proved [16, 20, 27, 30]. In such a case, lineless data transfer can be realized at the same time. Here, we study only the possibility of exploiting the leakage electric field from the planar nanodevice surface to detect a change in dielectric layers in the nanoscale. In fact, it is interesting to study the interaction of devices through this leakage electric field, which may result in additional device functions or be useful for a 3D integrated circuit.

5. Conclusion

In this paper, we have carried out 2D–3D combined EMC simulations to analyze the effects of 3D electric-field coupling on the performances of a SGT. We find that electric-field coupling through the device substrate plays an important role in the device performance. As such, the depth of insulating trenches,

which is seldom studied in previous work, deserves a careful consideration during device designs and fabrications. We also find that the effective depth of electric-field coupling through the device substrate is no more than 400 nm, so that by ensuring all the trenches to be more than 400 nm in depth, designers can be free from considering the accurate value of the trench depth. This may be desired in circuit applications. Moreover, the simulation results reveal that a lot of electric-field coupling occurs outside the device, within several hundred nanometers height from the device surface. As a result, the device operations are very sensitive to a change in dielectric layers on the device surface, implying a promising application for measuring the properties of nanometer thin films.

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