Development of Reactive-Ion Etching for ZnO-Based Nanodevices

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Abstract—We report on the systematic studies of reactive-ion etching (RIE) conditions for zinc oxide (ZnO) films with methane and hydrogen gases. The etching conditions were optimized to ensure high selectivity of ZnO to poly(methyl methacrylate) (PMMA), which is commonly used as an etching mask in nanolithography. We also show the feasibility of fabricating nanofeatures patterned onto a thin layer (<200 nm) of PMMA by nanoimprint technique and electron -beam lithography with the optimized RIE process parameters. Finally, planar nanodevices including self-switching diodes and side-gate transistors were successfully fabricated.

Index Terms—Nanoimprint technique, reactive-ion etching (RIE), semiconductor device fabrication, zinc oxide devices (ZnO).

I. INTRODUCTION

ZINC oxide (ZnO), among the various metal oxide materials, is an important electronic and photonic material because of its wide direct band gap of 3.37 eV, which make it transparent to visible light. It also exhibits a large exciton binding energy of 60 meV, as compared to GaN of 25 meV. The high exciton binding energy allows greater luminescence efficiency of light emission. In fact, efficient excitonic ultraviolet lasing has been demonstrated at 300 K [1]. ZnO has also found applications in displays [2], and in transparent conducting films [3]. The rapidly growing interest in low-cost, transparent, and potentially flexible electronics has recently led to intensive research on ZnO-based transistors [4]–[7] and diodes [8].

Although ZnO can be easily wet etched by various solutions [9]–[12], the lateral etching is found to be significantly large in certain cases for ZnO films due to the poly-crystalline nature [13]. This makes it very challenging to fabricate nanostructures and nanodevices, where the lateral dimension is very small. One possible route is to develop reactive-ion etching

(RIE) techniques for ZnO. A few groups have reported different RIE approaches for ZnO using gas combinations, such as CH₄/H₂ [14], CH₄/H₂/Ar [10], SiCl₄ [15], etc. So far, most of the work focused on the factors that determine the etching rate, which is excellent in fabricating large features using photolithography, since the photoresist etching mask, normally in micrometer, is much thicker than the typical ZnO-film thickness (~10–100 nm). When it comes to the fabrication of nanostructures, however, the study of etching selectivity becomes crucial since the most commonly used organic etching mask material in both standard electron-beam (e-beam) fabrication and also nanoimprint lithograph is a thin layer of poly(methyl methacrylate) (PMMA). Therefore, in this paper, we purposely use PMMA as the etching mask and optimize RIE conditions for etching ZnO, such as gas compositions, pressure, power, etc, in order to achieve the best selectivity and lowest damage to the films. The determined optimal condition was then validated by fabricating planar nanodiodes called self-switching diode (SSD) [16] and side-gate transistors [17], which were chosen because they require well-defined nanotrenches to function properly.

Generally, the RIE etching process is rather complex, involving diffusion of radicals to the surface, chemical reactions, desorption and ion bombardments of surface, etc. The chemical reaction may be an inverse of chemical vapor deposition (CVD), and the etch products may include volatile organometallic compounds and hydrides. For the hydrogen and methane RIE process, H and CH₃ radicals are generated in the plasma. The CH₃ radicals can react and form polymers on the ZnO film surface during etching. If hydrogen concentration is too low, significant polymer deposition may occur on the ZnO surface. Therefore, the optimization of various parameters of RIE process is very important to fabricate nanostructures. The most important optimization of this paper is to achieve the highest etching selectivity of ZnO with respect to PMMA. Both nanoimprint technique and e-beam lithography impose some constraint on the thickness of PMMA for RIE. Typically, the stamps for the nanoimprint have feature depths of around 100–200 nm. And after imprinting, there always remains some residual layer of PMMA [18], and therefore, the residual PMMA has to be etched with a short time of O₂ plasma, resulting in a reduced thickness of PMMA serving as the etching mask. For the e-beam lithography, we also adopted the standard PMMA thickness of 150 nm.

II. EXPERIMENTAL PROCEDURE

To begin, the ZnO were sputtered onto oxidized silicon wafers to a thickness of 30 nm with the Edward Coating system. The ZnO target of purity of 99.999% was obtained commercially

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Fig. 1. ZnO etching rate as a function of RF plasma power with $\text{CH}_4:\text{H}_2 = 10:50$ and at a pressure of 75 mtorr.

from the Kurt J. Lesker Company. For the RIE etching of ZnO, we have chosen to use methane (CH_4) and hydrogen (H_2) plasma chemistry [14], which are less toxic and corrosive than the more commonly used chlorine plasma chemistry [19]. The RIE chamber from JLS RIE-80 was precleaned by an oxygen plasma process to prevent contamination. The etching rate of the ZnO material was investigated by systematically varying the composition of the methane and hydrogen gas ratio, the RF plasma power, and the work pressure. A total etching time of 5 min was used for all samples under various etching condition. After etching, the remaining PMMA was removed and the surface of ZnO was analyzed with an atomic force microscopy (AFM) to evaluate the etched depth and surface roughness.

III. RESULTS AND DISCUSSION

A. Reactive-Ion Etching of ZnO

We determine the ZnO etching rate as a function of RF plasma power at a pressure of 75 mtorr with the etchant gases at a proportion of $\text{CH}_4:\text{H}_2 = 10:50$ in the flow rate. As shown in Fig. 1, a linear etching rate within the RF power of 100–200 W could be observed. Next, we investigate the ratio of the etchant gas proportion of CH_4 to the total combine gas flow rate ($\text{H}_2 + \text{CH}_4$), with fixed RF power (150 W) and chamber pressure (75 mtorr). To investigate the ratio effect, we keep the total gas flow rate at 60 sccm and change both CH_4 and H_2 gas flow rates. We found that the ZnO material etches fastest when the ratio is around 8%, see Fig. 2. However with this ratio, we also found that it etches the PMMA faster. Increasing the CH_4 gas ratio is normally expected to enhance the etching of PMMA and ZnO. However, a higher CH_4 gas concentration may also induce CH_x radicals to form a polymer byproduct layer on the PMMA or ZnO surface, as indeed observed in our experiments, and hence, reduce the etching rate. Our experiments show that the highest PMMA etching rate is achieved at $\sim 8\%$ gas ratio. It is worthy to note that for successful e-beam lithography and nanoimprint

Fig. 2. Etching rate of ZnO and PMMA as a function of different etchant gases ratio. The chamber pressure is set to 75 mtorr, while the RF plasma power is 150 W.

technique, the thickness of the PMMA has to be around 200 nm. Therefore, to minimize the etching and significant roughening of the PMMA layer, we have chose to perform ZnO etching at the gas ratio of around 16% ($\text{CH}_4:\text{H}_2 = 10:50$). In this case, the selectivity of the ZnO to the PMMA has a factor of 2, as indicated in Fig. 3. Under a low pressure, the etching rate is mostly limited by the CH_x radical concentration in the plasma. Hence, the etching rate increases with the pressure. However, as the pressure is above a threshold value, the CH_x radical concentration may no longer be a limiting factor. The etching rate will then be limited by other factors of the chemical reaction, including the ion mean-free path, which might reduce as pressure increases. Also, the dc bias in our system would decrease as the pressure increases. Such a threshold pressure may be different for ZnO and PMMA, due to their different material properties, which may explain the highest selectivity around 75 mtorr.

Fig. 4 shows a graph of the self-bias voltage and ZnO etching rate as a function of pressure in the chamber. At a gas flow rate ratio of $\text{CH}_4:\text{H}_2 = 10:50$ and at 150-W RF plasma power, the bias voltage decreases as the pressure increases. For the ZnO, the etching rate increases as a function of pressure up to 70 mtorr, and then decreases with further increase in pressure. It is possible to say that the etching mechanisms differ in these two regimes above and below 70 mtorr. It is known that when both the self-bias voltage and the etching rate decrease as a function of pressure, the etching mechanism is principally due to the presence of ion bombardment on the surface. This is because when the chamber pressure increases, the ions mean-free path decreases, resulting in lower ion energies, and thus, a decrease in the etching rate. On the other hand, when the etching rate increases with an increase in the chamber pressure, the etch rate is not dependent on ion impact energy, but instead on the concentration of some reactive particles like radicals, particles in metastable states. When the pressure is higher than 70 mtorr, the etching rate is already down to a quite low value. The roughness

Fig. 3. ZnO etching rate and selectivity of ZnO/PMMA as a function of chamber pressure. Gas ratio is set to $\text{CH}_4:\text{H}_2 = 10:50$, while the RF plasma power is 150 W.

Fig. 4. ZnO etching rate and self-bias voltage as a function of chamber pressure. Gas ratio is set to $\text{CH}_4:\text{H}_2 = 10:50$, while RF plasma power is 150 W. When the pressure is lower, a lower concentration of CH_x radical may reduce the etching rate even though the ion energy increases slightly due to the increased bias voltage.

also significantly increases, which makes it more difficult to accurately determine the etch rate.

It is important to note that RIE etching may cause severe surface damage to the PMMA mask layer. Fig. 5 shows the etching rate of PMMA and its rms roughness of the etched surface roughness with respect to the chamber pressure. The experiments were performed at a gas ratio of $\text{CH}_4:\text{H}_2 = 10:50$ and at 150 W. The PMMA etching rate decreases with an increase in the chamber pressure just like the self-bias voltage. The rms remains at values between 5 and 10 nm until the pressure reaches 80 mtorr and then it increases to 20 nm. The chemical reaction and ion bombardment in the etching cause surface damage or roughness, but the etching process also constantly removes at least some of the top layer of the material. When the etching rate is very low, the latter effect becomes less effective, which may result in the significantly increase in roughness as observed at 80 mtorr.

Fig. 5. PMMA etching rate and rms of surface as a function of pressure.

Fig. 6. Schematic diagram of the process flow of fabricating an SSD diode by nanoimprint technique. ZnO was (a) sputtered on a substrate, (b) layer of PMMA coated on the substrate, (c) nanoimprinting a stamp onto the PMMA, (d) layer of residual PMMA without pattern was removed, and (e) ZnO etched, and (f) remaining PMMA removed by O_2 plasma.

B. Fabrication of ZnO Devices by Nanoimprint and E-Beam Lithography

Finally, with our set of optimized RIE parameters, we have fabricated two types of novel nanodevice, which are chosen because their narrow nanochannels are very sensitive to the perfection of geometry. Fig. 6 depicts a schematic illustration of the nanoimprint fabrication process of the SSD. Firstly, a 30-nm-thick layer of ZnO was sputtered onto an oxidized silicon wafer by RF sputtering using Ar gas at 40 W of RF power and

Fig. 7. (a) AFM topology of a series of SSDs aligned in parallel, and (b) I - V characteristic of the SSDs.

at room temperature [see Fig. 6(a)]. The ZnO deposited onto an oxidized silicon wafer was polycrystalline consisting of grains of 200 nm in diameter. Following this, a 200-nm-thick layer of PMMA was spin-coated onto the substrate [see Fig. 6(b)]. The wafer was then hard baked at 140 °C for 15 min. The stamp that contains the SSD features was then hot embossed into the PMMA at 130 °C for 30 min [see Fig. 6(c)]. The substrate was cooled down to room temperature to allow the PMMA to be hardened before the stamp was retrieved. Fig. 6(d) shows a layer of residual PMMA and has to be etched away with an O_2 plasma at 50 W for 40 s at a pressure of 50 mtorr. Finally, the ZnO layer is etched with the optimized condition of a pressure of 75 mtorr, at RF power of 150 W and with a gas ratio of $CH_4:H_2 = 10:50$ [see Fig. 6(e)]. The remaining PMMA was removed with acetone and O_2 plasma [see Fig. 6(f)]. In addition, we have also fabricated devices by e-beam lithography, which is similar to nanoimprint, except that the O_2 plasma to remove PMMA residual is not needed as the patterns are well defined by the e-beam. Electrode metallization were thermal evaporated and patterned onto the ZnO by photolithography with photoresist. The lift-off technique was performed to complete the devices.

Fig. 8. (a) AFM image of a side-gate transistor. (b) I_{DS} versus V_{GS} with $V_{DS} = 20$ V, and (c) I_{DS} versus V_{DS} characteristic curves for V_{GS} ranging from 0 to 30 V. G denotes the gate, while D and S are the drain and source, respectively.

C. I - V Characterization of ZnO Devices

Fig. 7(a) shows an AFM image of a series of SSDs in parallel fabricated by nanoimprint technique. These back-to-back L-shaped grooves (merging into U-shape grooves) on the ZnO originate a strongly nonlinear rectifying I - V characteristic [see Fig. 7(b)], which is a consequence of the opening/closing of the channel due to the field effect of the surrounding regions. The electrical measurements were performed with an Agilent E5270B precision measurement mainframe at room temperature in a shielded probe station to avoid external spurious signals. Such I - V characteristic of SSD has been observed in InGaAs quantum well material and matches Monte Carlo simulation [20]. An advantage of SSD is that it neither requires doping nor tunneling barrier. It is known currently that it is difficult to grow high mobility and highly doped p-type ZnO

material [21], thus, rendering growth of high quality p-n ZnO diode difficult. To realize high-performance diode in ZnO, it is possible to fabricate SSD-like structure in n-type material.

An AFM image of the side-gate transistor fabricated by e-beam lithography is shown in Fig. 8(a). For this typical transistor, the channel length is 1.5 μm and the width is 400 nm. The etched grooves, which separate the channel from the gates, are 100-nm wide. The transfer curve is performed with $V_{\text{DS}} = 20$ V and is shown in Fig. 8(b). The threshold voltage is estimated to be at -4 V and an on/off ratio of $\sim 10^3$. The device exhibits excellent gate controlled of the linear and saturation operation regimes for the ZnO transistor, as shown in Fig. 8(c). Both types of nanodevices have worked well, showing that the optimized RIE process is suitable for fabricating nanoscale electronic structures. In this paper, we have not investigated the sidewall profile of the etched trenches, which may be studied by imaging the cross section using a high-resolution scanning electron microscope.

IV. CONCLUSION

In conclusion, we have systematically studied the RIE etching conditions for ZnO films in combination with e-beam lithography and nanoimprint techniques using PMMA as the etching mask. Nanofeatures down to 100 nm were successfully fabricated using a set of optimized condition for etching ZnO, thus, allowing functional nanodevices based on ZnO.

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