Analysis and Design of
Synchronisation Methods for
Power Converters Connected to
Weak Grid

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Abstract

Modern power systems are continually shifting towards greater integration of renewable energy sources and interconnection of existing AC grids that may operate asynchronously with respect to each other. The high-voltage direct current (HVDC) transmission and the associated voltage source converters (VSCs) are considered the most efficient technology for integrating the various energy sources. However, one of the key underlying requirements for the effective control of power flow in these VSC-HVDC systems is the appropriate synchronisation of the VSC converter with its corresponding AC grid, which relies on the accurate information regarding the phase angle of the AC voltage at the point of common coupling. This information is typically obtained using the so called Phase-Locked Loop (PLL). The task of grid synchronisation becomes particularly challenging in the cases where the grid interconnection may be located at a large distance from the area within which its voltage is tightly controlled. This is reflected by a large value of the Thevenin equivalent AC grid impedance and such systems are called "weak grids". Weak grid condition introduces significant stability and dynamic challenges since, due to the large grid impedance, both the phase and the magnitude of the voltage at the point of common coupling, which itself is used for both grid synchronisation and active/reactive power control, experience severe fluctuations as a result of variations in the active/reactive power flow.

Therefore, this thesis addresses the effect of the grid strength on the operation of the PLL utilised by the VSC converter. The results show that the previously proposed impedance conditioned PLL (IC-PLL) has the ability to increase the upper bound on the achievable power transfer achieved by the VSC converter connected to the weak grid. The effectiveness of this approach is examined by comparing its steady-state power transfer capability and the dynamic performance with that of VSC-HVDC that relies on conventional synchronous reference frame PLL (SRF-PLL) based synchronisation method. Furthermore, the challenge of the variable grid strength is also addressed in this thesis, whereby proposing the adaptive IC-PLL (AIC-PLL), which estimates virtual impedance by utilising feedback signal. The results show that the converter that relies on AIC-PLL has the ability to transfer power that is approximately equal to the theoretical maximum power whilst maintaining satisfactory dynamic performance.
Declaration

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I would like to dedicate this thesis to my family
Publication

JOURNAL PUBLICATIONS

"Adaptive Impedance Conditioned Phase Locked Loop (AIC-PLL) for VSC-HVDC system connected to weak AC grid" In preparation

CONFERENCE PUBLICATIONS

Chapter 1

Introduction

1.1 Background

The ever-increasing integration of distributed generation systems should fulfil the highly rigid requirements imposed by national grid of any country in the world aiming to maintain grid stability. The renewable energy sources, such as photovoltaic (PV) and wind turbine should comply with these requirements in terms of the voltage quality [3]. In order to have a stable operation for the interfaced renewable energy sources to the grid, the grid variables, such as voltage and frequency at the point of common coupling are required to be monitored. Hence, the operation of these sources should satisfy specified certain requirements, which are provided in the so-called grid code [3]. Adherence to this grid code is ensured by using power converters to accurately control the grid variables at the point of common coupling. This requirement for accurate observation and control ensures that the grid variables do not exceed their limits specified by the grid code and prevents disconnection of the renewable energy sources interconnected to the grid at the point of common coupling [4], [5]. For instance and based on [6] maximum voltage total harmonic distortion (THD) is 8%, for the voltage unbalance for three phase system the maximum unbalance is 3% and frequency
variations is ±1%. In all of these cases, interconnection with the main AC grid is realised by utilising power converters. A power conversion system converts the electric energy from one form to another, in which the new form is more feasible for certain systems or devices, which require specific waveforms of voltage and current in order to function properly. Electrical power generated by various sources of energy needs to be appropriately conditioned and controlled so that the resultant voltage and current are compatible with the grid or the transmission system characteristics. For example, the power that is generated by WT or PV cell needs to be converted so that the new voltage has, for instance, a 240V/50Hz characteristic, which is compatible with the grid voltage at a point of common coupling. However, due to a number of eventualities, such as increase or decrease of the electrical load in the power system, presence of harmonics, instances of faults occurring due to mistakes in the operation of electrical equipment or lightning strikes, electrical variables such as voltage, current and frequency cannot be considered as constant magnitudes. Hence, these variables should be monitored to ensure the grid state is appropriate for the correct operation of the power converter. Therefore, interconnecting the overall power grid with electrical energy sources such as WT or PV via power converters can affect the stability and the safety conditions of the power system, especially since these power converters are often employed to participate in supporting the grid frequency and voltage [3].

In the case of offshore wind farms, a high voltage direct current (HVDC) technology is considered more feasible technology than the AC transmission for high power transfer over long distances [7]. For the overhead lines when the distance exceed 600 km, the lines would have high inductive characteristics [8], and high capacitive characteristics in the case of underwater cables longer than 40 km. In the case of the AC system, the long distances of transmission lines absorb reactive power, which has a negative impact on the voltage level. Therefore, it requires intermediate compensation
1.1 Background

stations in order to maintain the voltage level in a certain value [7]. Since 1954, when the first commercial HVDC link between mainland Sweden and Gotland island was commissioned, the installed power transferred using HVDC transmission has significantly increased worldwide [1].

There are two types of the converter technologies utilised in HVDC transmission system: the conventional line-commutated converter (LCC) and self-commutated voltage source converter (VSC). Figure 1.1 shows the HVDC system with LCC converter, and Figure 1.2 shows the HVDC with VSC converter.

Fig. 1.1 Conventional HVDC with current source converters [1].
The conventional LCC converters, also known as Current Source Converter (CSC), is a thyristor based system. The switching of the valves, i.e. the thyristors, is controlled by a gate signal for the turn-on, and by the zero-crossing of the AC current for the turn-off. However, since AC current is determined by the AC voltage, the operation of the LCC-HVDC depends on the stiffness of the grid [9]. If the grid is weak, the system will not work properly since the voltage exhibits high fluctuations in the case of weak grid connection. The disturbances in the voltage cause problem well-know as commutation failures at the inverter station, which creates short circuit on the DC side, and temporarily stop the power transmission [9].

The recently developed voltage source converter (VSC) has progressively gained ever increasing popularity as the power conversion technology of choice in the case of HVDC systems due to its several advantages over the LCC based system [1]. The VSC-HVDC system is self-commutated by using pulse-width modulation (PWM) technique to control power transistors, typically Insulated Gate Bipolar Transistors (IGBTs). The voltage that is used to control the switching devices is independent of the AC system [10]. VSC-HVDC is capable of controlling both real and reactive power in both directions without the need to reverse the voltage polarity [1]. Moreover, VSC-HVDC introduces
1.2 General aspects of high-impedance ac systems

much lower harmonic content when compared to LCC-HVDC, which significantly reduces filtering and reactive power compensation requirements and, therefore, reduces the footprint of the power converter stations [1].

The phase angle of the AC grid voltage at the point of common coupling is considered to be critical to ensure correct synchronisation of the connected power converter with the grid. Through synchronisation, only information of the fundamental component is extracted and provided to the converters[3]. This information is typically obtained using so called Phase-Locked Loop (PLL). When the PLL is locked, the output signal of the PLL synchronises with the input signal, where both signals oscillate at the same frequency with a particular value of a phase shift [11]. In addition, the phase angle of the grid voltage is utilised to transform the sinusoidally varying AC quantities into quasi-stationary dq-axis quantities by means of the Park Transformation. Hence, three-phase AC currents are transformed into their corresponding active and reactive components that can then be controlled independently using standard PI/PID regulators [12],[13] and [14]. Therefore, the ability of the PLL to accurately synchronise with the grid and accurately estimate the phase angle of the grid voltage at the point of common coupling directly impacts the performance of the overall closed-loop system, and, in particular, its ability to independently control the exchange of active and reactive power with the AC grid at the point of common coupling. Hence, if PLL loses synchronisation with the grid then, as a consequence, the corresponding VSC converter will also lose synchronisation with the AC system to which it is connected [15].

1.2 General aspects of high-impedance ac systems

In some parts of the world, renewable energy resources are usually located in remote areas, far away from the load centres [16]. These sources are integrated into grids with long transmission lines, which leads to a large value of the Thevenin equivalent AC grid
impedance, and such system is called "weak grid" [17] [18]. The grid strength is one of the main factors that affect the operation of the grid connected converter; it influences the stability and the dynamic performance of the converter [19]. Typically, the strength of the grid is measured by the short circuit ratio (SCR). According to [20][21] the SCR is the ratio of the short circuit capacity to DC link rated power, and it is mathematically defined as

\[
SCR = \frac{S_{ac}}{P_{dc}} = \frac{U^2}{Z_g P_{dc}}. \tag{1.1}
\]

Where \( S_{ac} \) is the short circuit capacity of the AC system at the point of common coupling and \( P_{dc} \) is the rated DC power of the HVDC link. If the voltage at PCC is assumed to be identical to the base value, and the rated power of the HVDC is used as the base power of the AC system, equation (1.1) can be further simplified as

\[
SCR = \frac{U^2}{Z_g P_{dc}} = \frac{U^2}{Z_g \frac{U_{base}^2}{Z_{base}}} = \frac{1}{Z_g(p.u.)} \tag{1.2}
\]

where \( U_{base} \) and \( Z_{base} \) are the base values of the voltage and impedance, respectively, and \( Z_g(p.u.) \) is the value of the impedance in per unit. Based on [20], the strength of the AC system is strong if \( SCR > 3 \), \( 2 < SCR < 3 \) for weak grid and \( SCR < 2 \) for very weak grid.

Weak grid connections impose challenges on the operation of the VSC-HVDC system. The voltage at the PCC becomes more sensitive to power variations in the case of the weak grid connections, this, in turn, will affect the stability and dynamic performance of the system [22], [23]. The high sensitivity to power variations leads to high voltage fluctuations. Therefore, the utilised PLL needs to be sufficiently fast to lock with the variations in the voltage. However, fast PLL, i.e. large bandwidth, leads to high frequency components and noise to propagate through the system and causing system
1.3 Thesis objectives

instability [19]. In addition, there is a theoretical limitation for each value of SCR on the maximum power that the VSC-HVDC system can transmit to or from the AC system [8] [20]. Another challenge emerges when the converter connected to the weak AC grid, which is the mutual coupling in controlling the active power and voltage. The interactions between the active power control and voltage control increases as the value of the grid impedance increases [24].

Moreover, the task of grid synchronisation becomes particularly challenging in the case of the weak grid. As the active/reactive power flow changes, both the phase and the magnitude of the voltage exhibit severe fluctuations, which, in turn, introduces significant stability and dynamic challenges. It is therefore essential to consider the PLL both in terms of the static (steady-state) power transfer and the dynamic performance of the power converter. Various PLLs were proposed in order to deal with the weak grid connection issue, such as Damping Factor-PLL (DF-PLL) and Impedance-Conditioned PLL (IC-PLL) [25], [26]. However, the extensive study on the effect of different PLLs parameters on the power transfer capability and the dynamic performance is largely absent from literature. In addition, the estimation of the grid impedance is essential in order to appropriately deploy IC-PLL, and the task is even more challenging in the realistic case of varying grid impedance. Thus, there is a need for an adaptive PLL to address the variation that may occur in the grid impedance, so that the converter maintains the ability to transfer near-maximum power with satisfactory dynamic performance.

1.3 Thesis objectives

The objectives of this project are:

- To develop and validate the mathematical models of the VSC-HVDC that utilises several different types of already proposed PLLs.
• To investigate and compare different types of PLL based systems in terms of their steady-state (static) power transfer capability and dynamic performance.

• To develop and evaluate a new PLL that can deal with the variable grid impedance.

1.4 Contributions of the thesis

The main contributions of the thesis are given as follows

• A new adaptive Impedance-Conditioned PLL (AIC-PLL) is proposed and evaluated. This method utilises the internally generated angle in the PLL to estimate the value of the virtual impedance. Therefore, the requirement for advanced estimations techniques becomes redundant. In the case of the variation of SCR, the AIC-PLL has almost the same ability to the IC-PLL with $Z_v^v = Z_v$ in terms of maximum power transfer and the dynamic performance.

• The mathematical model derivation procedures that are used in the literature for the VSC-HVDC system are validated. The method that provides validated results is chosen for developing mathematical models of the different types of PLL based converters.

• Comparisons of power conversion systems that employ different types of PLL are curried out. These comparisons include both the steady-state maximum power transfer capability and the dynamic performance, considering different design parameters for different values of the grid impedance.

1.5 Outline of the thesis

The outline of the thesis is as follows
1.5 Outline of the thesis

**Chapter 2** - This chapter provides a general overview of the main elements of the studied VSC-HVDC system, a mathematical description for each element is given in this chapter.

**Chapter 3** - This chapter introduces the standard formulation of PLL, with a detailed description of each of the main PLL’s components. The literature review on developments and applications of PLL is included in this chapter, where the PLL’s implementations in different applications fields and theoretical works in PLL are given. The general mathematical model of the PLL is provided in detail. The key parameters of the PLL are provided in this chapter with time-domain simulation examples. Finally, descriptions on different types of PLL, namely, SRF-PLL, DF-PLL and IC-PLL, are provided.

**Chapter 4** - In this chapter, the mathematical models of the three types of PLL based system are developed and validated. The nonlinear mathematical model is first derived and validated, the linearised mathematical models are then developed and validated.

**Chapter 5** - The comparison and evaluation of different types of PLLs in terms of the steady-state transfer capability and dynamic performance are given in this chapter. The effect of each of the PLL’s parameters on the maximum power transfer capability and dynamic performance is studied.

**Chapter 6** - The proposed adaptive IC-PLL is introduced in this chapter. An explanation of the AIC-PLL with mathematical description is provided. Comparisons with other types of PLLs in terms of stability limits and dynamic performance are provided.

**Chapter 7** - This chapter summarises the thesis and provides suggestions for future work.
Chapter 2

General System Description of the VSC-HVDC System

This chapter aims to describe the studied VSC-HVDC system. Figure 2.1 shows the block diagram of the overall system. The main elements of the system are considered individually and mathematical description is provided for each element. The system consists of four main parts, which are

1. *The power circuit system, which is derived in Section 2.1.*

2. *Park and Inverse Park Transformation, which is described in Section 2.2.*

3. *Phase-Locked Loop (PLL) (this element is studied in details in Chapter 3).*

4. *Vector current control, which is provided in Section 2.4.*
The studied system in the project is shown in Figure 2.1. The overall system consists of two main parts: the upper part which represents the AC network, in this part, $R_c$ and $L_c$ represent the converter resistance and inductance, and $R_g$ and $L_g$ represent the grid resistance and inductance, respectively. The $C_f$ represent the AC capacitor connected to the filter bus. The symbols $v$, $u$ and $e$ represent the voltage vector of the VSC converter, the filter bus and AC source, respectively. $V$, $U$ and $E$ are their corresponding voltage magnitudes. The AC source is considered as the voltage reference, and it is a constant-frequency stiff voltage source. The phase angle of $v$, $u$ are $\theta_v$ and $\theta_u$, respectively. The symbols $P$ and $Q$ are the active and reactive powers from the VSC to the AC system. The quantity $i_c$ is the current vector of the phase reactor, and $i_g$ is the current vector to the AC source. The lower part, which
represents the Park transformation, inverse Park transformation and control system, are presented in details in the next sections.

2.1 The power circuit system

In this section, the mathematical model of the power circuit is derived. From a feedback control perspective, this model represents the plant to be controlled. In this part, the controlling signals are the value of the $dq$ components of the converter voltage $v$, which are manipulated to control the values of the current of the grid $i_g$ and voltage $u$ to produce the desired values of the active power $P$ and reactive power/voltage magnitude ($Q/U$). The power circuit model of the system is represented in Figure 2.2, which is the upper part in Figure 2.1,

![Fig. 2.2 Open loop AC circuit model](image)

The mathematical model of the three phase AC system can be defined in a stationary frame ($\alpha\beta$ frame), where the bold symbols with superscript $s$ represents the vector in $\alpha\beta$ frame written in the form given by 2.4, and the vector in the $dq$ frame written in the form given by 2.5.

The voltage across the converter inductance $L_c$ can be defined as

\[
L_c \frac{d{i_c}^s}{dt} = {v}^s - {u}^s - R_c{i_c}^s,
\]  

(2.1)
2.1 The power circuit system

and the voltage across the grid inductance $L_g$ is

$$L_g \frac{di_g^*}{dt} = u^* - E^* - R_g i_g^*, \quad (2.2)$$

and the current flow through the capacitor $C_f$ is

$$C_f \frac{du^*}{dt} = i_c^* - i_g^*. \quad (2.3)$$

$$x^* = x_\alpha + j \cdot x_\beta. \quad (2.4)$$

$$x = x_d + j \cdot x_q. \quad (2.5)$$

When the $dq$ frames are introduced for the voltages and currents the following relations are established

$$v^* = v e^{j \omega t}, \quad u^* = u e^{j \omega t}, \quad i_c^* = i_c e^{j \omega t}, \quad i_g^* = i_g e^{j \omega t}, \quad E^* = E e^{j \omega t} \quad (2.6)$$

In relations 2.6 the angle $\omega t$ is the angle that is used by the Park transformation and inverse Park transformation to generate the $dq$ components of the voltage and currents. Substitute 2.6 in equations 2.1-2.3 to obtain a mathematical model represented in the $dq$ frame

$$L_c \frac{di_{cd}}{dt} = V_d^* - u_d - R_c i_{cd} + \omega L_c i_{cd}, \quad (2.7)$$
General System Description of the VSC-HVDC System

\[
L_c \frac{d i_{cq}}{dt} = V_q^* - u_q - R_c i_{cq} - \omega L_c i_{cd}, \tag{2.8}
\]

\[
C_f \frac{d u_d}{dt} = i_{cd} - i_{gd} + \omega C_f u_q, \tag{2.9}
\]

\[
C_f \frac{d u_q}{dt} = i_{cq} - i_{gq} - \omega C_f u_d, \tag{2.10}
\]

\[
L_g \frac{d i_{gd}}{dt} = u_d - E_d - R_g i_{gd} + \omega L_g i_{gq}, \tag{2.11}
\]

\[
L_g \frac{d i_{gq}}{dt} = u_q - E_q - R_g i_{gq} - \omega L_g i_{gd}. \tag{2.12}
\]

The mathematical model (2.7)-(2.12) is the general open loop model for the AC circuit in the \(dq\) frame where the voltages and the currents are synchronised to any point. \(\omega t\) is the phase angle at which the space vector of the reference voltage rotates, therefore the value of \(\omega t\) indicates the reference voltage to which the other voltages and currents are synchronised. The \(d\) components of the voltages and the currents are aligned with the space vector of the reference voltage, and the \(q\) component of the reference voltage is equal to zero. When the value of \(\omega t = \omega_c t\), where \(\omega_c\) is the angular frequency of the infinite bus voltage, the reference voltage will be the voltage at the infinite bus \(E\). In this case, all the voltages and the currents are synchronised to the infinite bus; as a result, \(E_d = E\) and \(E_q = 0\). Therefore, the mathematical model (2.7)-(2.12) represents the model of the system in a \(dq\) frame for the open loop AC power circuit, where the voltage \(E\) is considered as the reference voltage for all other variables, where the phase angle of this voltage \(\theta_E = 0^\circ\). In the converter side, the reference voltage is chosen to be at the point of common coupling which is the voltage \(u\). In this case, the value of the phase angle \(\omega t\) is the phase angle at which the space vector of the voltage \(u\)
rotates. Therefore, in the converter side all the manipulated voltages and currents are synchronised to the voltage $u$. Figure 2.3 illustrates the concept of the two $dq$ frames,

\begin{figure}[h]
\centering
\includegraphics[width=0.5\textwidth]{fig2.3}
\caption{Two frames for the VSC-HVDC system}
\end{figure}

In Figure 2.3 the two frames, Grid frame and Converter frame, represent the reference frames of the grid and converter sides, respectively. As was explained above the $d$ axis of the Grid frame is aligned with the space vector of the voltage $E$, and the $d$ axis of the convert frame is aligned with the voltage $u$. The phase shift between the two frames is the angle $\theta_{PLL}$, which represents the phase angle between the voltages $u$ and $E$. Therefore, in the next chapters, the rotation matrix $T_{dq}$ in 2.19 models the Park transformation and $T_{dq}^{-1}$ models the inverse park transformation.

2.2 Park and Inverse Park Transformation

The idea behind the proposing of Park Transformation refers back to the 1920s, when R. H. Park proposed a new theory of electric machine analysis to simplify the complexity of the machine model [27]. This complexity is due to the time-varying mutual inductances parameters of the differential equations for the three phase synchronous motor [27]. Park Transformation refers variables (voltages, currents, and flux linkages) of the stator to fictional windings that synchronously rotate with the rotor [27]. Since this transformation was introduced, it has become an essential block in controlling three
phase system. The natural time dependent three phase frame (abc) is converted to synchronously rotating time-independent reference frame (dq). The balanced (abc) natural frame can be represented as [28]

\[
\begin{bmatrix}
v_a \\
v_b \\
v_c \\
\end{bmatrix} =
\begin{bmatrix}
V_m \cos(\theta) \\
V_m \cos(\theta - \frac{2\pi}{3}) \\
V_m \cos(\theta + \frac{2\pi}{3}) \\
\end{bmatrix}
\]

(2.13)

where \(v_a, v_b\) and \(v_c\) are the three voltage vectors, \(V_m\) is the peak value of the voltage, and \(\theta\) is the phase angle of the phase \(a\) which is time-varying quantity. Note that three phases \(a, b\) and \(c\) are distributed in a spatial diagram, which is different from the widely used phasor diagrams. In a spatial diagram, the vectors that are used to express the phases do not rotate, while the vectors in a phasor diagram rotate. The length and direction of the vectors in a spatial diagram change with time, so that the instantaneous values of the vector voltages \(v_{abc}\) is represented by the length of the vector and its direction. The length and direction of vectors in the phasor diagram do not change, while the phase angles change [28].

The three phases in spatial diagram are displaced from each other by \(\frac{2\pi}{3}\) rad, the \(v_a\) is generally assumed to be aligned with horizontal axis, \(v_b\) is rotated with respect to \(v_a\) by \(-\frac{2\pi}{3}\) radians, i.e. in the same direction of the vector \(\alpha = e^{-j\frac{2\pi}{3}}\) and \(v_c\) is in the same direction of the vector \(\alpha^2 = e^{-j\frac{4\pi}{3}}\) [28]. Figure 2.4 illustrates the reference frames
2.2 Park and Inverse Park Transformation

For the balanced system, the space vector $\bar{v}_s$ can be represented in terms of the natural frame as

$$\bar{v}_s = v_a + \alpha v_b + \alpha^2 v_c = v_a + \left(-\frac{1}{2} - j\frac{\sqrt{3}}{2}\right)v_b + \left(-\frac{1}{2} + j\frac{\sqrt{3}}{2}\right)v_c = v_a - \frac{1}{2}(v_b + v_c) + j\frac{\sqrt{3}}{2}(-v_b + v_c)$$

(2.14)

for the balance system $v_a + v_b + v_c = 0 \rightarrow v_a = -(v_b + v_c)$, and substitute in equation 2.14 to have

$$\bar{v}_s = \frac{3}{2}v_a + j\frac{\sqrt{3}}{2}(-v_b + v_c).$$

(2.15)

Multiply equation 2.15 by a factor $k = 2/3$, and it can be rewritten in the form of equation 2.16
General System Description of the VSC-HVDC System

\[
\begin{bmatrix}
v_{\alpha} \\
v_{\beta}
\end{bmatrix} =
\begin{bmatrix}
v_a \\
\frac{\sqrt{3}}{3}(-v_b + v_c)
\end{bmatrix},
\] (2.16)

hence, the \(\alpha\) component in the form of \(\alpha\beta\) is always the same as \(v_a\) in the \(abc\) form.

Therefore, the space vector \(\bar{v}_s\) can be rewritten as (see Figure 2.4)

\[
\bar{v}_s = v_{\alpha} + jv_{\beta}.
\] (2.17)

As a result, \(v_{\alpha}\) and \(v_{\beta}\) can be represented as functions of \(v_a, v_b\) and \(v_c\)

\[
\begin{bmatrix}
v_{\alpha} \\
v_{\beta}
\end{bmatrix} = T_{\alpha\beta}
\begin{bmatrix}
v_a \\
v_b \\
v_c
\end{bmatrix},
\] (2.18)

where the \(abc \rightarrow \alpha\beta\) transformation matrix can be defined as

\[
T_{\alpha\beta} = \frac{2}{3}
\begin{bmatrix}
1 & -\frac{1}{2} & -\frac{1}{2} \\
0 & -\frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2}
\end{bmatrix}.
\]

The transformation given in equation 2.18 is called the Clarke transform or \(abc \rightarrow \alpha\beta\) [28]. However, \(v_{\alpha}\) and \(v_{\beta}\) are still time-varying quantities. If a reference frame \(dq\) is introduced so that it rotates synchronously with the space vector \(\bar{v}_s\), the space vector \(\bar{v}_s\) that is defined in the \(dq\) frame become time-invariant quantity and it does not rotate. The \(T_{dq}\) is a rotating matrix that describes the transformation between \(\alpha\beta\)
and the $dq$ reference frames, in which the $dq$ frame rotates at a synchronous speed

$$T_{dq} = \begin{bmatrix} \cos \theta_g & -\sin \theta_g \\ \sin \theta_g & \cos \theta_g \end{bmatrix}. \quad (2.19)$$

Therefore,

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = T_{dq} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix}. \quad (2.20)$$

Substitute equation 2.18 in 2.20 and simplify by using trigonometric function properties to finally have

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} V_m \cos(\theta_g - \theta) \\ V_m \sin(\theta_g - \theta) \end{bmatrix}. \quad (2.21)$$

The transformation $abc \rightarrow dq$ is called Park Transformation. It is clear from equation 2.21 that $V_d$ and $V_q$ are constant, provided that the frame $dq$ rotates at frequency $\dot{\theta}_g$ which is the same frequency $\dot{\theta}$ of the space vector $\bar{v}_s$ where $\int (\dot{\theta}_g - \dot{\theta}) \, dt \rightarrow \theta_g - \theta = c$, $c$ is a some constant, see Figure 2.4 [28]. In addition, from Figure 2.4, $\bar{v}_s$ can be defined as a function of $V_d$ and $V_q$, that is

$$\bar{v}_s = V_d + jV_q. \quad (2.22)$$

Finally, the relation between the space vector $\bar{v}_s$ defined in $\alpha\beta$ frame and $dq$ frame can be represented in equation 2.23

$$\bar{v}_s = V_d + jV_q = (v_\alpha + jv_\beta)e^{j\theta_g} = V_me^{j(\theta_g - \theta)}. \quad (2.23)$$
2.3 Phase-Locked Loop (PLL)

Phase-Locked Loop (PLL) is considered as an essential element in the voltage source converter (VSC), as it plays a significant role for synchronising the various energy sources that the VSCs are connected [3]. It monitors the grid and provides the phase angle of the grid voltage at the point of the common coupling (PCC) to the Park Transformation ($abc/dq$) and inverse Park Transformation ($dq/abc$). When the converter is well synchronised the angle that is produced by the PLL $\omega t$ (as it is shown in Figure 2.1) will be the phase angle of the voltage at which the converter is synchronised. Therefore, if the point of common coupling (PCC) is chosen as a synchronisation point, the estimated phase angle $\omega t$ will be the phase angle of the voltage $u$. Hence, all the $d$ components of the manipulated voltages and the currents in the converter are aligned with the voltage $u$ and, $u_d = U$, $u_q = 0$. The phase angle $\omega t = \theta_{PLL} + \omega_c t$, $\omega_c$ is the central frequency for the PLL, which equals to the value of the frequency at which the grid operates on, i.e, the frequency of the voltage $E$. It can be deduced that the phase $\omega t$ is a periodic signal that oscillates between $(0 - 2\pi)$, and the angle $\theta_{PLL}$ is a step change signal, which is equal to the phase difference between $u$ and $E$, with an assumption the system is in a steady state and synchronised. The detailed description about PLL will be discussed in Chapter 3.

2.4 Vector current control

The function of the converter control is to control the active and reactive power transfer/ voltage magnitude by manipulating the value of the amplitude and the angle of the converter produced voltage. This can be achieved by controlling the $dq$ components of the voltage $v$, which as a result controlling the current $i_c$. Therefore,
2.4 Vector current control

Vector current control is a current control based method, in which the flowing current into the converter is limited so that the valves of the converter are protected from the over current problem that may occur due to disturbances [23]. By utilising the vector current control the instantaneous active power and reactive power are controlled independently through a fast inner current control loop [29]. The inner controller decouples the current into \( d \) and \( q \) components. The \( d \) component is used by the outer loop controller to control the active power, and the \( q \) component to control the reactive power/ voltage amplitude. One of the main advantages of transforming the voltages and the current into \( dq \) components, which are constant quantities, is facilitating controlling the system by using a straightforward controller such as PI controller. As this type of controller has the ability to deal with the constant quantities. This is due to the internal-model principle which states that "any good tracking controller must stabilize the closed-loop system and must contain a model of the reference signal" [30].

Hence, the mathematical model of the manipulated signals, which are in a \( dq \) form, can be represented by first order differential equations which are consistent with the differential equation of the PI controller.

In the literature, different control strategies have been proposed in order to overcome the drawbacks of the conventional vector current control in terms of dealing with the weak grid issues and the challenging of the variation of the operating points. An alternative approach referred to as a power synchronisation control (PSC) was proposed in [29] [18]. This technique emulates the idea of the power transmitted in the synchronous machines which are governed by the well-known power angle equation. Despite the fact that this method does not require for PLL to provide synchronisation, the converter needs to switch to the vector current control during the severe AC system faults for protection from over current of the converter valves. In addition, in this method the controller needs to operate on lower bandwidth when connected to a very
weak ac system in order to maintain the stability of the system. Study in [24] shows that the weak grid causes a dependent and coupled control for high power injected values. It is reported that for the system with a very weak grid SCR=1 and low transmitted power, the independent between controlling the voltage at the point of common coupling and controlling active power is presented, and this is violated for the higher power demand. For this reason, a modification in the outer loop controller is proposed to include decoupling gains on the error signal of the outer loop controller before being processed by its PI controller, and the gains are tuned by $H_\infty$ control design methodology. However, the controller is complicated, and it does not match the standard vector current control that is used in the industry. In [31] $H_\infty$ controller methodology is also used to replace the vector current control to control the system considering the parametric uncertainties and operating point variation.

The vector current control approach basically consists of two controller loops, the inner and outer loops as shown below;

### 2.4.1 Outer loop controller

The function of the outer loop is to control the active and reactive/ voltage magnitude at PCC by manipulating the value of the $dq$ components of the converter current $i_c$, where in this thesis the case of controlling voltage magnitude is chosen. As it is shown in Figure 2.1, the reference input signals of this controller are the reference active power $P^*$ and reference voltage magnitude $U^*$, and they are fed with the feedback of the active power $P_m$ and voltage magnitude $U_m$ into two PI controllers. These controllers produce two current reference signals $i_{cd}^*$ for the active power and $i_{cq}^*$ for the voltage magnitude, to be fed into the inner loop controller. Low pass filters are also applied to the signals of the power and the voltage flow of the feedback. The following set of mathematical equations represent the model of the outer loop controller [26]:

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2.4 Vector current control

The PI controller of the active power is

\[ c_{i_{cd}}^* = K_{Pp}(P^* - P_m) + K_{Pi} \cdot \gamma_P, \]  
(2.24)

and

\[ \gamma_P = \int_0^t (P^* - P_m)d\tau. \]  
(2.25)

The model of the low pass filter that is applied to the feedback signal of the active power is

\[ P_m = \int_0^t (\omega_P \cdot P - \omega_P \cdot P_m)d\tau. \]  
(2.26)

The PI controller of the voltage amplitude is

\[ c_{i_{cq}}^* = -K_{Up}(U^* - U_m) - K_{Ui} \cdot \gamma_U, \]  
(2.27)

and

\[ \gamma_U = \int_0^t (U^* - U_m)d\tau. \]  
(2.28)

The model of the low pass filter that is applied to the feedback signal of the voltage amplitude is

\[ U_m = \int_0^t (\omega_U \cdot U - \omega_U \cdot U_m)d\tau. \]  
(2.29)

The produced \( c_{i_{dq}}^* \) are the control input signals represent the set-points for the inner loop controller which is explained in the next subsection.
2.4.2 Inner loop controller

The function of the inner loop is to control the value of the converter’s currents by manipulating the values of the converter voltages $cV_{d,q}^*$, which are fed into the switching device, as it is shown in Figure 2.1. The inner loop consists of two PI controllers and the cross coupling terms $\omega \cdot L_c$. The function of the cross coupling terms is to control the $d,q$ components of the converter current $c_i_c$ independently. An active damping algorithm is also included in the inner loop controller in order to attenuate the oscillation in the voltage at PCC [32]. The following set of the mathematical equations represent the model of the inner loop controller;

The mathematical model of the reference converter voltage $V_d$ is

$$cV_d^* = c u_d - \omega \cdot L_c \cdot c_i_{cq} + k_{pd}(c_i^{*d} - c_i^{cd}) + k_{id} \cdot \gamma_d - v_{AD,d}, \quad (2.30)$$

where

$$\gamma_d = \int_0^t (c_i^{*d} - c_i^{cd})d\tau. \quad (2.31)$$

The mathematical model of the active damping part can be defined as

$$v_{AD,d} = K_{AD}(c u_d - \phi_d), \quad (2.32)$$

where

$$\phi_d = \int_0^t (\omega_{AD} \cdot c u_d - \omega_{AD} \cdot \phi_d)d\tau. \quad (2.33)$$
2.5 Conclusion

The mathematical model of the reference converter voltage $V_q$ is

$$^cV_q^* = ^c u_q + \omega \cdot L_c \cdot ^c i_{cd} + k_{pq}(^c i_{eq}^* - ^c i_{eq}) + k_{iq} \cdot \gamma_q - v_{AD,q},$$  \hspace{1cm} (2.34)

where

$$\gamma_q = \int_0^t (^c i_{eq}^* - ^c i_{eq})d\tau.$$  \hspace{1cm} (2.35)

The mathematical model of the active damping part can be defined as

$$V_{AD,q} = K_{AD}(^c u_q - \phi_q),$$  \hspace{1cm} (2.36)

where

$$\phi_q = \int_0^t (\omega_{AD} \cdot ^c u_q - \omega_{AD} \cdot \phi_q)d\tau.$$  \hspace{1cm} (2.37)

2.5 Conclusion

In this chapter, descriptions about the main elements of the VSC-HVDC are provided with a mathematical model that represents each element. For the PLL (the next chapter is dedicated to it) an explanation about the phase angles is provided. A mathematical model of the AC circuit system is derived in a $dq$ frame. This chapter also introduces the concept of two frames (Converter frame and Grid frame), as this concept is essential in modelling the overall system in Chapter 4.
Chapter 3

Phase-Locked Loop

3.1 Introduction

Grid synchronisation is considered as an important issue in the operation of the power conversion systems, since it allows the grid and the synchronised power converter to work in unison. The estimated information by the grid synchronisation algorithm is used by the control system of a grid connected converter in order to have an effective control of the power flow. One of the typical synchronisation algorithms is a phase-locked loop (PLL), it is a closed-loop system in which the generated output signal has characteristics (phase, frequency and amplitude) related to a reference input signal, where the obtained information by PLL is fed into the grid connected converter. Since PLL’s invention, it has been broadly used in several fields, such as communication, motor servo control systems and power conversion systems [33]. Therefore, this chapter is devoted to PLL, where the next section discusses the main elements of PLL and an explanation is given to each element. Section 3.3 presents PLL application and literature review. Where in this section various PLL’s implementations in different fields are given, in addition, contributions in PLL’s design and modifications are also provided in this section. The basic transfer function of the PLL is derived in
Section 3.4, where the main elements of the PLL are only included in the developed model. The important parameters in PLL’s operation are explained in Section 3.5, mathematical relations and illustrated simulation results to each of the parameters is included. Finally, descriptions of the three types of PLL, namely, SRF-PLL, DF-PLL and IC-PLL are provided in Section 3.6.

3.2 PLL basic loop components

A basic structure of PLL consists of three components (Figure 3.1) [2]:
1. Phase detector (PD).
2. Loop filter.

![Figure 3.1 A general block diagram of the Phase-Locked Loop [2]](image)

The phase detector (PD)

PD is a nonlinear element that produces a voltage of $V_q$, which is related to the phase difference between the input signal and the VCO output signal. The waveform of the produced $V_q$ depends on the type of utilised PD. There are two types of PD, namely sinusoidal PD or digital PD. Figure 3.2 depicts the characteristics of these two types [33].
The sinusoidal PD operates as a multiplier and it is a zero memory device, generating a sinusoidal wave voltage. In the sinusoidal PD, the phase detection interval is \((-\pi/2, +\pi/2)\). Another type of PD is termed a digital PD. It is implemented by a sequential logic circuit, which contains a memory device to store the past values in order to achieve PD characteristic that is difficult to obtain by the multiplier PD. The characteristics of the digital PD are linear over a range of the phase difference interval, are linear over \((-\pi/2, \pi/2)\) of \(\theta_d\) for triangular PD, \((-\pi, \pi)\) for sawtooth PD and \((-2\pi, 2\pi)\) for sequential PD [33]. In Figure 3.2 all the curves have the same slope at \(\theta_d = 0\), which means the different types of PD have the same PD gain \(K_d\). The PD interval is a significant factor in the PLL operation, the larger the interval, the larger the tracking range of the PLL [33].

**Loop filter (LF)**

The loop filter is typically a linear component of a PLL which attenuates the noise and high frequency components of the PD output signal. In most of the cases, the loop filter (LF) is modelled as a cascade of the low pass filter and a PI controller,
3.2 PLL basic loop components

whose output is the control signal fed into the VCO. Designing the loop filter is the key underlying for tuning the PLL, this is where it has more degree of freedom in shaping the PLL characteristic than the other two elements. In the case of tracking a step in frequency, which is the typical case in the power system, the loop filter should contain an integrator. In this case, PLL is Type 2, as the VCO modelled as an integrator [34]. The linear analysis tools are typically used, such as frequency response and root locus, when designing this component of the PLL.

**Voltage-controlled oscillator (VCO)**

VCO is one of the main components of PLL which receives a control signal as an input from LF and generates an oscillatory output signal with a frequency proportional to the magnitude of its input signal. In order for the VCO to work properly, it needs to satisfy certain requirements such as phase stability, high range of output frequency, high modulation sensitivity and linearity of the relationship between output signal’s frequency and input control signal. There are four types of an oscillator which are commonly used, namely, voltage controlled crystal oscillators, resonator oscillators, RC multivibrators, and YIG-tuned oscillators [35].

PD detects the difference in the phases between the input signal and the output signal of the VCO, where the output voltage of the PD is proportionally related to this difference. The loop filter attenuates the high frequency components of the PD’s output and then the output signal is fed into the VCO. The output frequency of the VCO changes to reduce the frequency difference with the input signal’s one. When both frequencies are equal, the loop enters the locked mode. During this mode, the PD keeps its output value at a certain constant level to maintain the loop locked [2].
3.3 PLL applications and literature review

Since PLL was invented, researchers in several applications have paid attention to its significance. One of the earliest widespread applications of the PLL dates back to 1943, when a work by K. R. Wendt [36] was published to provide synchronisation in television receivers. Two PLLs (which are referred to in the paper as "automatic frequency and phase controlled synchronising system") are utilised for vertical and horizontal receiver circuits. For each circuit, the VCO (named in the paper as "scanning oscillator") generates saw-tooth wave to compare it by PD with the synchronising input signal, and then low pass filter attenuates noise and high-frequency components to generate control voltage for the VCO. Another prominent use of PLL is in the spaceflight, where the first utilising of PLL in the satellite communication backs to the first American artificial satellite. Due to the Doppler effect, the frequency of the transmitted signal from the spaceflight sources is shifted; therefore, PLL is utilised for recovering the error in the frequency of the received signal [2].

Several works have been done in the field of the analysis and design of the PLL, particularly when the PLL is used in sophisticated applications where the simple analysis tools are not applicable. One of these applications is when the PLL utilised to track a frequency ramp input signal. Doppler shift produces a frequency ramp input signal, and to deal with this signal, a Type 3 system is needed to have a zero steady state error [34]. For Type 1 and Type 2 PLLs, the parameters’ values that make the linear model stable also guarantee the stability of the nonlinear model, which is not the case for the Type 3 PLL. Therefore, Lyapunov Redesign was proposed to design a Type 3 PLL in [37]. The second method of Lyapunov is adopted, as this approach does not require a solution for the differential equation, it depends on the generalised energy in the system. The same technique is also adopted to examine the stability of the
3.3 PLL applications and literature review

classical digital PLL [38]. Further analysis on a Type 3 PLL has been done in [39]. The work started with analysing the system considering the signal is small enough to be examined as a linear system, then extending the analysis for the nonlinear region. The second method of Lyapunov and LaSalle’s Theorem are used as tools to analyse the nonlinear system[34]. The low order filter limits the performance of the PLL, therefore, in order to have a better performance, a high order filter is considered. It is difficult to design PLL with a high order filter through the aforementioned approach, therefore, the circle criterion and the Popov criterion are used for PLL design [40], [41].

For the high frequency PLL applications, a challenge emerges in simulating the system, as the system would work in two time scales. The first one is the fast time scale which includes the input signal and the output of the voltage controlled oscillator. The second one is the slow time scale which is often called modulation domain, which is the output of the loop filter [42]. It is therefore typical to break up the simulation of the PLL into two parts [43].

In the literature, PLL is also used as a part of the control scheme for various types of motor control. One of the earliest applications dates back to 1970 [44], where PLL is used to mimic the synchronous motor operation. In this work, the stator and rotor fields are considered to be analogue to the input signal and the VCO output signal of the PLL, respectively. The rotor’s and stator’s fields rotate at the same speed, which is analogues to the manner in which the VCO output signal tracks the input signal of the PLL. By this analogy, the synchronous motor can be viewed as a PLL. Therefore, the model of the PLL can be used to mathematically describe operation of the synchronous motor, particularly in the presence of torque disturbances.

Digital PLL is utilised in order to control the speed of the induction motor [45]. The speed control of the induction motor by a variable frequency is considered the most efficient method of the induction motor control. In this work, the speed of the rotor
measured by means of a digital optical encoder whose output frequency is proportional to the motor speed. The output signal of the digital encoder is compared using the phase detector with the desired motor’s speed signal. Therefore, instead of comparing the output of the VCO with the reference signal, the square wave output of the digital optical encoder is used to compare with the reference oscillator. The same methodology can be found in [46] and [47]. In the first work, stability and dynamic response are studied for a PLL based control induction motor, where the mathematical model of the induction motor is simply described as a first order differential equation. In the second work, a time domain state space model has been developed for PLL based speed control induction motor, where a detailed mathematical model of the induction motor is considered. Based on [48], most of the PLL based speed control of the induction motor exhibit some drawbacks, such as the unreliability of the acquisition process for large step-input speed changes, slow pull-in process and losing the synchronisation when the motor is subjected to a sudden load disturbance. It is therefore a microcomputer-based fuzzy logic controller is proposed based on PLL to enhance the pull-in process, where the fuzzy logic controller is utilised to pull the speed of the motor into the PLL lock-in range.

In [49], PLL-assisted internal-model (IM) controller is proposed to control brushless DC motor. In this work, PLL is added to internal model control to achieve a fast transient speed and an accurate steady state. Therefore, the original loop of IMC is combined with the PLL’s one so that the conventional PI control is responsible to provide a fast transient, and the PLL is responsible to improve the accuracy of the steady state. PLL is utilised for frequency tracking system for portable microelectromechanical piezoresistive cantilever mass sensors [50]. The VCO of PLL generates a frequency which synchronises with the signal comes from MEMS cantilever. The same technique is also used in [51] for cantilever array sensors.
The merit of PLL in terms of estimation the frequency and phase angle of the input signal acquires PLL importance for the power conversion utilisations. Therefore, it is attracted many researchers to consider PLL in this field. The PLL-based synchronisation for the single phase AC system works according to the modulation of the voltage controlled oscillator (VCO) to produce voltage whose frequency matches the grid’s one. The synchronisation occurs when the PLL is in a locked mode, during this mode, the frequency of the produced voltage by the VCO equals to the fundamental harmonic frequency of the grid with a certain value of phase shift [3]. Therefore, different types of PLLs are proposed in order to address various problems in the single-phase system, such as double frequency components and noise. In [52], [53] the enhanced PLL (E-PLL) is proposed, where in the PLL’s configuration an adaptive filter is involved in the PD. Hence, the E-PLL has the ability to extract the fundamental frequency components, amplitude and the phase shift of the input voltage. In [54], the second order generalized integrator PLL (SOGI-PLL) is proposed. In this method the PD involves a quadrature-signals generator, hence the single-phase is translated into an equivalent set of two-phase signals in order to achieve some form of internal cancellation of the high frequency components.

In the case of the three-phase grid connected converters, another challenging problem appears, which is the weak grid connection. Hence several modifications in the PLL are suggested to deal with this problem. In [55], [56] the voltage sensor-less technique has been proposed. In this method, a virtual flux concept is utilised to synchronise the converter with the grid at the point of synchronisation without any needing for the physical sensor. So that PLL utilities the flux instead of voltages to generate the phase angle of the point in the AC grid at which the converter is synchronised. However, this technique needs for advanced estimation method for providing the information of the grid impedance. In [57], [26] the same concept of the virtual flux is used, where the
voltage at the point of common coupling (PCC) is utilised by PLL and that voltage is subtracted by the voltage drop across the virtual impedance so that the converter is synchronised to a remote point in the stiff grid, where the SRF-PLL is modified to attach the virtual impedance. Another approach that is suggested to deal with a weak grid problem is modifying the SRF-PLL by attaching a damping factor term in order to suppress the oscillation that exhibits in the voltage at PCC due to the weak grid connections [25]. It has been shown that with a certain value of the damping factor the stability of the system is enhanced. However, this approach is limited to a weak grid with a $SCR > 1.83$.

Despite the fact that PLL has considerable properties which promote it to be utilised widely for different applications, PLL can cause significant stability and dynamic performance challenges. In the power conversion applications, PLL has a significant role in the stability issue. It is reported in [19] that the PLL gains affect the maximum power transfer capability of the VSC-HVDC converter, in particular weak grid connections. In addition, the system can transfer power equals to the theoretical power in the case of decreasing the values of the PLL gains [19]. For closed-loop synchronous reference frame PLL (SRF-PLL) based system, positive feedback emerges in the loop, where its voltage output is positive [58], [59]. This voltage has a negative impact on the synchronisation, as it drives the estimated angle by the PLL away from the grid input angle. The value of this voltage is determined by the value of the injected current into the convert (the transmitted power), and the value of the grid impedance. The larger the value of the current and the grid impedance, the larger the value of the voltage of the positive feedback. The interaction between the bandwidth of the PLL and the bandwidth of the controllers (DC-link voltage and the current controllers) is considered in [60] [61]. It shows that when the PLL bandwidth is close to the bandwidth of the controllers, it causes dynamic interaction, and as a result provoking instability in the
3.4 The basic transfer function of the PLL

system. However, applying a large reduction in the PLL bandwidth causes slower PLL response and as results slower PLL tracking for the phase angle.

Hence, from the reviewed papers, it can be concluded that PLL is an essential element in many applications. However, for the power conversion application, despite the importance of the PLL in the function of the power converters, it can induce some challenges in terms of stability and dynamic performance. Therefore, a new PLL called "adaptive impedance conditioned PLL (AIC-PLL)" is proposed in chapter 6 to overcome the drawbacks of the PLL in power conversion applications.

3.4 The basic transfer function of the PLL

In this section, the basic transfer function of the PLL is derived. Firstly, for each of the three components of PLL, the simplified linear model is derived. Following this, the overall linear model, given in the form of a transfer function, for PLL is obtained by combining individual components’ models. Figure 3.3 shows the detailed PLL’s block diagram.

\[ v_i = A_i \sin(\theta_i), \]  

(3.1)
\[ v_o = \cos(\theta_g). \quad (3.2) \]

Where \( \omega_c \) is the central angular frequency of the PLL, which is equal to the nominal frequency of the input signal. For the general sinusoidal wave, the phase angles \( \theta_i \) and \( \theta_g \) can be rewritten as \( \theta_i = \omega_i t + \theta_1, \theta_g = \omega_g t + \theta_2 \) [34]. Therefore, the input and the output signals can be rewritten as

\[ v_i = A_i \sin(\omega_i t + \theta_1), \quad (3.3) \]
\[ v_o = \cos(\omega_g t + \theta_2). \quad (3.4) \]

If the phase detector has a sinusoidal characteristic, the output signal of PD element \( V_q \) is given by multiplication of the two signals \( v_i \) and \( v_o \) as

\[ V_q = A_i K_d \sin(\omega_i t + \theta_1) \cos(\omega_g t + \theta_2), \quad (3.5) \]

where \( K_d \) is the gain of the PD.

Equation (3.5) can be simplified by using the trigonometric properties to get

\[ A_i K_d \sin(\omega_i t + \theta_1) \cos(\omega_g t + \theta_2) = \frac{A_i K_d}{2} \sin((\omega_i + \omega_g)t + \theta_1 + \theta_2) + \frac{A_i K_d}{2} \sin((\omega_i - \omega_g)t + \theta_1 - \theta_2). \quad (3.6) \]

Equation (3.6) contains two terms, the first one is adding the frequencies of the input and output signals to produce a high-frequency component, while the second term is the difference between them to produce a low-frequency component. To acquire a locked mode, the low-frequency component is allowed to propagate through the system. Hence, the controller generates a control signal which is proportional to
3.4 The basic transfer function of the PLL

the low-frequency component. This signal, as mentioned earlier, is fed into VCO to generate a signal with a frequency of \( \omega_g \approx \omega_i \), as a result, PLL is in locked mode. The high-frequency low pass filter in the PLL is designed for this purpose so that the low-frequency component propagates through the system. Whereas the high-frequency components are suppressed, as it may cause the system to be unstable. As a result, the first term in equation (3.6) is cancelled out, hence equation(3.6) is finally defined as 

\[
V_q = \frac{A_i K_d}{2} \sin \theta_d, \text{ where } \theta_d = (\theta_1 - \theta_2).
\]

If the phase shift between the input signal and the output signal is very small \( \theta_d \approx 0 \), the mathematical model 3.5 can be linearised. To linearise the nonlinear model, the first term in Taylor series \( \sin \theta_d = \theta_d - \frac{\theta_d^3}{3!} + \frac{\theta_d^5}{5!} - \cdots \) is chosen so that \( \sin \theta_d = \theta_d \). Hence, the system shown in Figure 3.3 can be represented by the block diagram shown in Figure 3.4.

The linearised mathematical model of PLL is derived assuming that the system is initially locked

\[
\begin{align*}
\theta_1 &\quad \rightarrow \theta_d \quad \rightarrow \quad H_L(s) \quad \rightarrow \quad \frac{1}{s} \quad \rightarrow \quad \theta_2 \\
\end{align*}
\]

Fig. 3.4 Linearized closed-loop PLL

The error signal \( \theta_d(s) = \theta_1(s) - \theta_2(s) \),
and \( \theta_2(s) = \theta_d(s)H_L(s)\frac{1}{s} \),
therefore, \( \theta_2(s) = (\theta_1(s) - \theta_2(s))H_L(s)\frac{1}{s} \Rightarrow \theta_2(s) = \frac{H_L(s)\frac{1}{s}}{1 + H_L(s)\frac{1}{s}}\theta_1(s) \).
If the loop transfer function \( L(s) = H_L(s)\frac{1}{s} \),
then, \( \theta_2(s) = \frac{L(s)}{1 + L(s)}\theta_1(s) \).
The sensitivity transfer function can be defined as \( S(s) = \frac{\theta_d(s)}{\theta_1(s)} = \frac{1}{1 + L(s)} \), and the complementary sensitivity as \( T(s) = \frac{\theta_2(s)}{\theta_1(s)} = \frac{L(s)}{1 + L(s)}, \) therefore, \( \theta_2(s) = T(s)\theta_1(s) \).
In the case the loop filter is chosen to be the PI controller with transfer function
\[ C(s) = \frac{K_p(T_i s + 1)}{T_i s}, \]
the overall linearised model of the PLL is
\[ \theta_2 = \frac{K_p s + K_p/T_i}{s^2 + K_p s + K_p/T_i} \theta_1. \]  
(3.7)

### 3.5 Key parameters of PLL

The mathematical model that is derived in the Section 3.4 is based on the assumption that PLL is initially locked, in this case, the system is considered linear. When PLL is out of lock, the model becomes very complicated and nonlinear. In order to understand under which conditions the PLL gets locked and under which conditions the PLL loses lock, the following parameters are needed to be discussed.

Firstly, the parameters that are responsible for maintaining PLL locked are [63] [64]:

**The hold-in range \( \Delta \omega_H \):**

It is the range of the input frequency in which PLL can statically maintain lock. Therefore, the system locks out if the input frequency of \( \omega_i \) is larger than \( \Delta \omega_H \). To calculate this value, the final value theorem is calculated for \( \theta_d \) [63]

\[
\lim_{t \to \infty} \theta_d(t) = \lim_{s \to 0} s \theta_d(s) = \lim_{s \to 0} s \frac{\Delta \omega_H}{s^2 + \frac{1}{C(s)}\frac{s}{1 + C(s)}} = \frac{\Delta \omega_H}{C(0)}
\]  
(3.8)

where \( \omega_i = \omega_c + \Delta \omega_H \). However, for a greater value of \( \theta_d \) where \( \sin \theta_d \neq \theta_d \), the true expression should be [2], [63]

\[
\sin \theta_d = \frac{\Delta \omega_H}{C(0)}.
\]  
(3.9)
To find a solution for equation 3.9, the following relation should be satisfied which is \( \Delta \omega_H \leq C(0) \). Therefore, if the changing in the frequency \( \Delta \omega_H \) is larger than the value \( C(0) \) the PLL gets unlocked. In the case of the PI controller where \( C(0) = \infty \), the hold range depends on the other parameters such as the frequency range that the VCO can cover [63]. Equation 3.9 indicates the importance of the characteristics of the phase detector for the operation of the PLL in terms of the stability of the system. To demonstrate how PLL becomes unlocked under the changing of the input frequency, the PI controller is replaced by a gain \( K_p = 5 \), so that the variation in the frequency of the input signal has a finite limit which is the value of the \( K_p \). For a nonlinear PLL, equation 3.9 becomes

\[
\sin \theta_d = \frac{\Delta \omega_H}{K_p} = \frac{\Delta \omega_H}{5},
\]

(3.10)

In this case, the step change in the input frequency should not exceed the value of \( K_p = 5 \) rad/s. If \( \Delta \omega_H > K_p \) for a nonlinear system, it falls out of lock and \( V_q \), which is the output of the PD, becomes beat in note rather than a DC level. Figure 3.5 depicts the block diagram of the linear and nonlinear model for PLL system that is utilised to conduct this experiment.
In Figure 3.5 the block diagram for the nonlinear model is chosen to be the SRF-PLL (as it is explained in the next section). This is because the value of the output voltage of the Park transformation (which represents the phase detector in PLL) is $V_q = V \sin(\theta_i - \theta_g)$, as was shown in the previous chapter. Figures 3.6 shows a comparison in the estimation of the frequency between linear and nonlinear PLL when $\Delta \omega_H < K_p$. Figures 3.7-3.9 illustrate the difference between the time domain responses of the linear and nonlinear PLL when $\Delta \omega_H > K_p$ for $\theta_g$, $\omega_g$ and $V_q$, respectively, where the value of $\omega_c = 0$ rad/s.
3.5 Key parameters of PLL

(a) $\omega_i = 2.5$ rad/sec 

(b) $\omega_i = 5$ rad/sec

Fig. 3.6 Comparison of the estimated frequency for the linear and nonlinear PLL when $\Delta \omega_H < K_p$

Fig. 3.7 Comparison of the estimated phase angle for the linear and nonlinear PLL when $\Delta \omega_H > K_p$
Fig. 3.8 Time-domain response of the estimated frequency of the nonlinear PLL when $\Delta \omega_H > K_p$

Fig. 3.9 Time-domain response of $V_q$

Figure 3.6 shows that both linear and nonlinear PLL are able to estimate the input frequency, where $\Delta \omega_H < K_p$. In this figure, two values of frequency input are applied, $\omega_i = 2.5$ rad/sec and $\omega_i = 5$ rad/sec. It is clear that as the value of the $\omega_i$ increases, the discrepancy between the nonlinear and linear system increases, which is clear from the error signals. This is because as the value of $\omega_i$ increases, the term $(\theta_i - \theta_g)$ in the equation $V_q = V_m \sin(\theta_i - \theta_g) = V_m \sin(\omega_i - \omega_g)t$ in the nonlinear system relatively becomes larger, as a results $\sin(\theta_i - \theta_g) \neq (\theta_i - \theta_g)$. Figures 3.7-3.9 show that the linear PLL is locked while nonlinear PLL fall out of lock when $\Delta \omega_H > K_p$, which based on
equation 3.10. It is clear from Figure 3.7 that the estimated phase angle $\theta_g$ for the linear model is synchronised with the input phase angle $\theta_i$ which is not the case for the nonlinear model. It is also obvious from Figure 3.7 that there is a phase shift between the input angle and the output angle for the linear model, which is due to the fact that the value of the phase error $\theta_d \neq 0$ in the steady state. In addition, Figures 3.8 and 3.9 show that the output frequency and the voltage of the PD of the nonlinear model is the beat in note rather than DC level, which is due to the unlock of the PLL.

The pull-out range $\Delta \omega_{po}$:

It is the frequency offset that if it is applied to the system as a step, it causes the PLL to be unlocked. $\Delta \omega_{po}$ can be considered the dynamic limit of stability. It is not possible to calculate the exact value of $\Delta \omega_{po}$, however, the approximation value of $\Delta \omega_{po}$ is calculated by simulation can be given as [63]

$$\Delta \omega_{po} = 1.8 \omega_n (\zeta + 1) \quad (3.11)$$

If the value of the step change of the input frequency is larger than the value of $\Delta \omega_{po}$, the PLL loses the lock state temporary, and the system will lock again after a certain period of time. To demonstrate how the PLL becomes temporary unlocked, a step change of a frequency input is applied, when $K_P = 10$ and $K_i/T_i = 5$, $\Delta \omega_{po} = 13.02$ rad/sec. Two cases are shown in Figures 3.10-3.15, when a 13 rad/sec is applied and 16 rad/sec is applied.
Fig. 3.10 $\theta_g$ with a 13 rad/sec step change

Fig. 3.11 $\omega_g$ with a 13 rad/sec step change

Fig. 3.12 $V_\psi$ with a 13 rad/sec step change
3.5 Key parameters of PLL

Fig. 3.13 $\theta_g$ with a 16 rad/sec step change

Fig. 3.14 $\omega_g$ with a 16 rad/sec step change

Fig. 3.15 $V_q$ with a 16 rad/sec step change
Figures 3.10-3.12 show that the system stays in a locked mode after applying at $t = 10$ sec a 13 rad/sec frequency step change which is less than the calculated value of $\Delta \omega_{po} = 13.02$ rad/sec. Whereas, Figure 3.13 and 3.15 illustrate how PLL unlocked temporarily, when a 16 rad/sec is applied at $t = 10$ sec, which is clear from the beat in note responses in the output frequency $\omega_g$ and voltage $V_q$ in Figures 3.14 and 3.15. Where the applied frequency step change exceeds the value of $\Delta \omega_{po} = 13.02$ rad/sec.

**A step of acceleration:**

When the frequency input signal changes linearly with time $\Delta \omega = \frac{\Delta \omega}{t}$ is applied to the PLL. The maximum value of $\dot{\Delta} \omega$ can be calculated by taking the final value for $\theta_d(t)$ with input signal $\theta_i(s) = \frac{\Delta \omega}{s^3}$ [63]

$$\lim_{t \to \infty} \theta_d(t) = \lim_{s \to 0} s \theta_d(s) = \lim_{s \to 0} \frac{s^2 + K_p s + K_p/T_i}{s s^3} = \frac{\Delta \omega}{K_p/T_i}.$$  

(3.12)

However, for a greater value of $\theta_d$ where $\sin \theta_d \neq \theta_d$, the true expression should be [2], [63]

$$\sin \theta_d = \frac{\dot{\Delta} \omega}{K_p/T_i}.$$  

(3.13)

To find a solution for equation 3.13, the following relation should be satisfied which is $\Delta \dot{\omega}_H \leq K_p/T_i$. In this case, the rate of change of the input frequency should always be smaller than the value $K_p/T_i$, otherwise the system would be unlocked. Figures 3.16-3.18 show two cases, for $\dot{\Delta} \omega < K_p/T_i$ and $\dot{\Delta} \omega > K_p/T_i$. 

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3.5 Key parameters of PLL

Fig. 3.16 Comparison of the estimated frequency for $\dot{\Delta}\omega < K_p/T_i$

Fig. 3.17 Comparison of the estimated frequency for $\dot{\Delta}\omega > K_p/T_i$

Fig. 3.18 Comparison of $V_q$ for $\Delta\omega > K_p/T_i$
Phase-Locked Loop

Figure 3.16 shows that the estimated frequency by linear and nonlinear PLL are identical for $\dot{\Delta}\omega < K_p/T_i$. For $\dot{\Delta}\omega > K_p/T_i$, Figures 3.17 and 3.18 show that the nonlinear PLL loses the tracking for the ramping input frequency. It also clear from Figures 3.17 and 3.18 that the deviation between linear and nonlinear responses of the models starts at the moment when $\frac{\Delta \omega}{K_p/T_i} = 1$, which is clear from Figure 3.18.

In the case that the system is unlocked, it can be locked by the following process [33]:

The lock-in process:

In this process, the PLL locks within one single-beat note between the input and output frequencies, and the locking process takes place within a frequency range called the lock range $\Delta \omega_L$. The approximation value of the $\Delta \omega_L$ is given by equation 3.14 [33][63]

$$\Delta \omega_L \approx \pm K_d K_v C(\infty).$$

(3.14)

Where $K_v$ is the VCO sensitivity. When $K_d = K_v = 1$, and in the case of the PI controller, $\Delta \omega_L = K_p$, $K_p = 5$ rad/s. Figure 3.19 shows the process of the locking-in,

![Fig. 3.19 The estimated frequency during the locking-in process](image)

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3.6 PLL for three-phase synchronisation

Figure 3.19 shows that at \( t = 10 \text{ sec} \) PLL is locked, where the system is initially unlocked and by reducing the input frequency to be equal to \( \Delta \omega_L = K_p \), PLL locks in within one cycle.

3.6 PLL for three-phase synchronisation

In this section, the types of PLL that are utilised in converters for the three-phase AC system are considered, which are SRF-PLL, DF-PLL and IC-PLL. In Chapters four and six the three types of PLL are considered in deriving the mathematical models of the HVDC-VSC converters and for studying the stability limits and the dynamic performance of the systems, respectively.

3.6.1 Synchronous reference frame PLL (SRF-PLL)

For the three-phase applications, the SRF-PLL is considered the most utilised PLL in the industry [28]. The early description of the SRF-PLL can be found in [65] and [66], as it is shown in Figure 3.20,

![Schematic diagram of the SRF-PLL system](image)

Fig. 3.20 Schematic diagram of the SRF-PLL system

As it is shown in Figure 3.20 the three-phase voltage is utilised by the Park transformation, as discussed in the previous chapter, the voltages \( u_d \) and \( u_q \) can be
mathematically described as

\[ u_d = U \cos(\theta_u - \theta_{PLL}), \] (3.15)
\[ u_q = U \sin(\theta_u - \theta_{PLL}), \] (3.16)

where the phase angle \( \theta_u \) is the phase angle at which the space vector of the voltage \( u_{abc} \) rotates. In Figure 3.20, the voltage \( u_q \) is fed into a PI controller, therefore, when the system is stable and in the steady-state, i.e. when the PLL is locked, \( u_q \rightarrow 0 \). The output of the PI controller is the estimated angular frequency, which is integrated to obtain the angle \( \theta_{PLL} \). Hence, in the steady-state, the phase angle \( \theta_{PLL} = \theta_g \), and \( u_d = U \). This is the state where the produced voltage by the converter that utilises SRF-PLL is synchronised to the measured voltage \( u_{abc} \).

The topology of the SRF-PLL in Figure 3.20 is considered the simplest form, another topology of the SRF-PLL can be demonstrated in Figure 3.21,

In Figure 3.21 the function \( \text{atan2} \) is used to generate the signal that is fed into the controller \( C(s) \) instead of the using the signal \( u_q \) only. This allows a higher linear range for the phase detector, as \( e_{\theta} = \text{atan2}(\frac{u_q}{u_d}) = \text{atan2}\left(\frac{\sin(\theta_u - \theta_{PLL})}{\cos(\theta_u - \theta_{PLL})}\right) = \theta_u - \theta_{PLL} \), as a results, increasing the hold range for the SRF-PLL.
3.6.2 Damping factor PLL (DF-PLL)

The voltage at the point of common coupling usually exhibits high-frequency oscillations for the high transferred power when the VSC converter connected to a weak grid system. Therefore, the transferred power is required to be reduced in order to minimise the oscillation of the voltage to maintain the stability in the system. The high oscillation of the voltage is caused by the high value of the inductance, which in turn reduces the value of the damping characteristic of the AC grid circuit. Consequently, a voltage with a high oscillation is fed into PLL causes the VSC-HVDC to be unstable. One of the proposed solutions is to append the damping factor $D$ into the existing PLL, so that the damping characteristics of the VSC system is enhanced [25]. In DF-PLL a parameter $D$ is multiplied by the error of the $d$ component of the converter current $c_i_{cd}$ (Figure 3.22). The parameter $D$ in DF-PLL functions as a dissipative element in the circuit, where the increasing the value of the resistive element in the circuit enhances the damping coefficient of the AC circuit [67] [68]. The structure of DF-PLL is similar to the structure of the SRF-PLL (the upper part in Figure 3.22) with the only difference that the attached damping factor (the lower part in Figure 3.22). The DF-PLL mathematical model is defined by equation 3.17, where '+' is for rectifying operation, and '-' is for the inverting operation.
Fig. 3.22 Schematic diagram of the Damping Factor PLL

\[
\frac{d\theta_{PLL}}{dt} = C(s)u_q \pm D(i_{cd}^* - i_{cd}) + \omega_c \tag{3.17}
\]

Where \(\theta_{PLL} = \int \omega_u dt\), in order to have appropriate comparisons in Chapter 5, the structure of the DF-PLL shown in Figure 3.22 is modified as to be represented as in Figure 3.23
And the mathematical model of the alternative topology of the DF-PLL is given as in equation 3.18

\[
\frac{d\theta_{PLL}}{dt} = K_{pPLL}\tan^{-1}\frac{c_{uq}}{c_{ud}} + K_{iPLL}\int\tan^{-1}\frac{c_{uq}}{c_{ud}}dt \pm D(c_{i*d} - c_{i*q}), \quad (3.18)
\]

where the sign “+” is for rectifying operation and “-” is for inverting operation.

The mathematical model of the low pass filter of the PLL is defined as

\[
\begin{align*}
\frac{c_{ud}}{dt} &= -\omega_{FLPLL}c_{ud} + \omega_{FLPLL}c_{u_d}, \\
\frac{c_{uq}}{dt} &= -\omega_{FLPLL}c_{uq} + \omega_{FLPLL}c_{u_q}.
\end{align*}
\]

where \(\omega_{FLPLL}\) is the bandwidth of the low pass filter of the PLL.
3.6.3 Impedance conditioned PLL (IC-PLL)

In this section, impedance conditioned PLL (IC-PLL) based system is considered, where in this technique the converter is not synchronised to the voltage at the point of common coupling (PCC), it is instead synchronised to the virtual remote point in the stiff grid. Hence, this provides better synchronisation (as a result better stability) as the converter is synchronised to a virtual point near to the infinite bus. So that the PLL receives a signal with lower fluctuations than the signal that is received by PLL in the case of the synchronising to the weak grid point.

The IC-PLL consists of SRF-PLL which is the upper part in Figure 3.24, and the virtual impedance as indicated in the lower part in the figure. In the IC-PLL, the \(dq\) components of the voltage at the virtual point is obtained by subtracting the \(dq\) components of the voltage \(u\) at PCC from the voltage drop across the virtual impedance.

The virtual impedance can be defined as

\[
Z_v = R_v + j\omega_{PLL}L_v,
\]

and the virtual voltage which are indicated in Figure 3.24 by its \(dq\) components as \(u_d\) \(u_q\) can be defined as

\[
\begin{align*}
u_d &= c u_d - c_i g_i g d R_v + \omega_{PLL} L_v^{vc} i g q, \\
u_q &= c u_q - c_i g q g d R_v - \omega_{PLL} L_v^{vc} i g d.
\end{align*}
\]

(3.20)

where the additional inputs to the PLL is the grid side current \(i_g\) in the \(dq\) frame [57],
Fig. 3.24 Block Diagram of the Impedance conditioned PLL

The mathematical model of the IC-PLL is defined as

\[
\frac{d\theta_{PLL}}{dt} = K_{pPLL} \tan^{-1} \frac{c_{uq}}{c_{udf}} + K_{iPLL} \int \tan^{-1} \frac{c_{uqf}}{c_{udf}} dt, \quad (3.21)
\]

and the mathematical model of the low pass filter of the IC-PLL is defined as in equation 3.19.

### 3.7 Conclusion

Phase-locked loop (PLL) was discussed in this chapter. An explanation for each main element of the PLL was provided. A literature review of the PLL and its applications are also given in this chapter. In the literature review, the earliest researches in the applications of the PLL are explained. The theoretical contributions in the PLL, PLL in control system and PLL in power conversion system are also considered in this
section. The mathematical model of the PLL is derived in this chapter. The derivation starts with considering the nonlinear system and then the linearised model is finally obtained. The key parameters of the PLL that governs the PLL’s locking state are provided with simulation results. Finally, different types of PLL that are utilised in the power conversion application are discussed, where the topology and the mathematical description of each one are explained.
Chapter 4

Modelling and Validation of VSC-HVDC Converter Utilising Various Types of PLLs

4.1 Introduction

In order to analyse the dynamic response of VSC-HVDC utilises any type of PLL, a nonlinear mathematical model is developed, and this model is validated by comparing its time-domain responses with the simulation of the overall system realised using MATLAB’s SimPowerSystem toolbox. This mathematical model is then linearised around an operating point so that the linear state space model is obtained. The linearised model is then validated by applying a small step change for the reference inputs and comparing the time-domain response with nonlinear one. In this chapter, the detailed mathematical model of the SRF-PLL based converter is provided. For DF-PLL and IC-PLL the result state space models are provided in Appendix A, and the results of the validations are provided in Appendix B. Note that in the developing
the mathematical model of the system, the converter, measurement equipment and PWM dynamics are neglected.

4.2 Developing the nonlinear mathematical model of the converter utilises SRF-PLL

In this section, the nonlinear mathematical model of the VSC-HVDC converter utilises SRF-PLL is derived and validated. Due to the fact that the PLL is a pivotal element in the control, modelling of VSC-HVDC, it is re-explained in this section, to make it more apparent to the reader. The topology of the SRF-PLL is chosen in this chapter to be as in Figure 4.1, which is the simplified model of the SRF-PLL in Figure 3.20. For the second configuration (Figure 3.21), the SRF-PLL is considered as a part of the IC-PLL with virtual impedance $Z_v = 0$.

![Fig. 4.1 The basic structure of the SRF-PLL](image)

Figure 4.1 illustrates the basic structure of the SRF-PLL. The phase angle $\theta_{PLL} = \frac{1}{s}\omega_u$ is generated by setting the $q$ component of the voltage $u$ to zero by feeding it into a PI controller, (the pre-superscript 'c' refer to the $q$ component in converter side as will be explained later).

Referring to Figure 2.1 the system consists of the two main parts; the first one is the main circuit model which represents the AC circuit system, and another part is the feedback which represents the PLL, the Park and inverse Park Transformations and the outer and inner loop controllers.
4.2 Developing the nonlinear mathematical model of the converter utilises SRF-PLL

Based on the literature, there are two approaches to derive the mathematical model of VSC-HVDC converter utilises any type of PLL, and that is based on how the produced angle by the PLL is mathematically coupled with the main circuit model. The methods of developing mathematical models are as follow.

The first method:

In the first method, the mathematical model that is derived in Chapter 2 for the AC circuit (2.7)-(2.12) are reconsidered in this section [31] [57] [25], where the SRF-PLL is utilised to estimate the phase angle $\omega t$ to synchronise the converter to the voltage $u$ at PCC. Due to the fact that the converter does not have any access to the voltage $e$ at the infinite bus, the relation $E^* = E e^{-j\omega t}$ in (2.6) is not valid. Therefore, the mathematical model for the voltage across the grid inductance $L_g$, which are (2.11)-(2.12) in Chapter 2 is rewritten as follow, the voltage across the grid inductance $L_g$ is

$$L_g \frac{di_g}{dt} = u - E^* e^{-j\omega t} - R_g i_g. \quad (4.1)$$

In (4.1) the term $E^* e^{-j\omega t}$ can be simplified as

$$E^* e^{-j\omega t} = E^* e^{-j(\omega t + \theta_{PLL})} = E e^{-j\theta_{PLL}}.$$

Where the vector $E = -E_d + j \cdot E_q$ is the voltage $e$ represented in a $dq$ frame defined with respect to the voltage $e$. Therefore, (4.1) can be rewritten as

$$L_g \frac{di_g}{dt} = u - E e^{-j\theta_{PLL}} - R_g i_g. \quad (4.2)$$

Equations 2.7, 2.10 and 4.2 show the system is represented by a mathematical model in which the voltage $u$ is chosen as a reference voltage, and the voltage $e$ in a $dq$ frame
rotates by phase shift $-\theta_{PLL}$ to be aligned with voltage $u$. The mathematical model of the outer and inner loop controllers are given as in 2.24-2.34 Chapter two, with considering not to include the pre-superscript $c$, as there is only one reference frame.

However, referring to Figure 2.1, and as it is stated before, the converter does not have any access to the voltage $e$, i.e. the voltage $E$ does not rotate by any angle. In addition, the derived mathematical model of the AC circuit, [2.7],[2.10] and [4.2] becomes dependent on the variable $\theta_{PLL}$, which estimated by SRF-PLL. However, the estimated angle of $\theta_{PLL}$ is not one of the main variables of the AC circuit power system. In addition, this method does not include any mathematical modelling for the Park and inverse Park transformation, i.e. the dynamics of these two main parts are neglected. It is therefore that this procedure of developing the mathematical model is not accurately valid for the VSC-HVDC system presented in Figure 2.1.

The second method

The second approach of modelling the VSC-HVDC system with including PLL is that by having two reference frames, as it is demonstrated in Section 2.1, to which the $dq$ components of the voltages and currents are referred. In the first reference frame, the voltages and the currents of the AC power circuit are represented by $dq$ components, which are synchronised to the voltage $e$ at the infinite bus, where the phase shift of this voltage is 0 degree. In another reference frame, the $dq$ components of the voltage and the currents are synchronised to the voltage $u$ at PCC, which represent the voltage and the current of the converter side. The rotation between the two frames occurs by the rotation matrices by the angle $\theta_{PLL}$ which is fed from the PLL [24] [23]. To distinguish between the two frames, pre-superscript $e$ refers to the voltages and the currents of the main circuit model, and pre-superscript $c$ is for the $dq$ components in a frame that is synchronised to the voltage $u$ at PCC. Figure 4.2 is the block diagram
4.2 Developing the nonlinear mathematical model of the converter utilises SRF-PLL that illustrates the second approach of modelling the SRF-PLL based VSC-HVDC system that is shown in Figure 2.1,

![Diagram](image)

**Fig. 4.2 Block diagram for the nonlinear mathematical model considering the dynamic of the PLL**

The mathematical model of the system can be represented as follow, the main circuit model is

\[
\dot{x} = f(x, u), \quad y = h(x) \tag{4.3}
\]
where

\[
\begin{bmatrix}
\frac{1}{L_c} V_d^e - \frac{1}{L_c} u_d - \frac{R_c}{L_c} i_{cd} + \omega^e i_{cq} \\
\frac{1}{L_c} V_q^e - \frac{1}{L_c} u_q - \frac{R_c}{L_c} i_{cq} - \omega^e i_{cd} \\
\frac{1}{C_f} e^{i_{cd}} - \frac{1}{C_f} e^{i_{gd}} + \omega^e u_q \\
\frac{1}{C_f} e^{i_{cq}} - \frac{1}{C_f} e^{i_{gq}} - \omega^e u_d \\
\frac{1}{L_g} u_d - \frac{1}{L_g} E - \frac{R_g}{L_g} i_{gd} + \omega^e i_{gq} \\
\frac{1}{L_g} u_q - \frac{R_g}{L_g} i_{gq} - \omega^e i_{gd}
\end{bmatrix},
\]

\[h(x) = \begin{bmatrix} P \\ U \end{bmatrix}^T.\]

And

\[P = \sqrt{u_d^2 + u_q^2}. \]

The rotation matrices are

\[e^{M_e^{-1}} = e^{M_e} = \begin{bmatrix} \cos \theta_{PLL} & \sin \theta_{PLL} \\ -\sin \theta_{PLL} & \cos \theta_{PLL} \end{bmatrix}.\]

The mathematical models of the inner and outer controllers are given as in 2.24-2.34.

The mathematical model of the SRF-PLL is given as

\[\frac{d\theta_{PLL}}{dt} = K_{PLL} e^{u_q} + K_{PLL} \gamma_{PLL}, \quad (4.4)\]
4.2 Developing the nonlinear mathematical model of the converter utilises SRF-PLL

where

\[ \gamma_{pll} = \int_0^t c_u q d\tau. \]

The states vector of the system is given as

\[ x = [e_{i_{cd}} e_{i_{cq}} e_{u_d} e_{u_q} e_{i_{gd}} e_{i_{gq}} \gamma_d \gamma_q \theta_{PLL} \gamma_{PLL} \gamma_P \gamma_U \phi_d \phi_q P_m U_m]. \]

In the case of only the inner-loop controller included

\[ u = [e_{i_{*cd}} e_{i_{*cq}} E]. \]

Figures 4.3 and 4.4, and the attached Figures B.1-B.4 in Appendix B show comparisons between the time-domain responses of the mathematical models that were derived based on the two approaches with the simulation of the overall system realised using MATLAB’s SimPowerSystem toolbox. The simulation experiment is conducted by applying a step change into the reference input signals (10% in \( e_{i_{cd}} \) and \( e_{i_{cq}} \)).
Fig. 4.3 Comparison of $u_d$ for the two mathematical models with MATLAB’s SimPowerSystem toolbox model for the SRF-PLL based converter

Fig. 4.4 Comparison of $u_q$ for the two mathematical models with MATLAB’s SimPowerSystem toolbox model for the SRF-PLL based converter

Where the Nonlinear Math. 1 refers to the nonlinear mathematical model that is derived based on the first approach and the Nonlinear Math. 2 refers to the model of the second approach. Figures 4.3-4.4 and Figures B.1-B.4 in Appendix B reveal that the nonlinear mathematical model that is derived based on the second approach provides very similar results to the MATLAB’s SimPowerSystem toolbox model. It is
4.3 Developing the small-signal model of the SRF-PLL based system

The small-signal model is obtained by linearising the nonlinear mathematical model around an operating point, so that the linear state-space model is eventually developed. The state-space mathematical model is utilised to evaluate the stability and dynamic performance of the system. The outer loop controller is considered at this step, and Figure 4.5 shows the block diagram of the linearised mathematical model, where the symbol \( \Delta \) refers to the small signal of the voltages and currents [23].

Fig. 4.5 Block diagram for the linearised mathematical model considering the dynamic of the PLL
The linearisation of the main circuit model which is represented by (4.3) produces the following linear state-space model

\[
\dot{\tilde{x}} = \begin{bmatrix}
\frac{R_c}{L_c} & \omega & -\frac{1}{L_c} & 0 & 0 & 0 \\
-\omega & -\frac{R_c}{L_c} & 0 & -\frac{1}{L_c} & 0 & 0 \\
\frac{1}{C_f} & 0 & 0 & \omega & -\frac{1}{C_f} & 0 \\
0 & \frac{1}{C_f} & -\omega & 0 & 0 & -\frac{1}{C_f} \\
0 & 0 & \frac{1}{L_g} & 0 & -\frac{R_g}{L_g} & \omega \\
0 & 0 & 0 & \frac{1}{L_g} & -\omega & -\frac{R_g}{L_g}
\end{bmatrix} \tilde{x} + \begin{bmatrix}
\frac{1}{L_c} & 0 & 0 & 0 & 0 \\
0 & \frac{1}{L_c} & 0 & 0 & 0
\end{bmatrix}^T \tilde{u},
\tag{4.5}
\]

\[
y = \begin{bmatrix}
0 & 0 & e_{i_{gd}} & e_{i_{gq}} & e_{u_{d0}} & e_{u_{q0}} \\
0 & 0 & -e_{i_{gq}} & e_{i_{gd}} & e_{u_{gq}} & -e_{u_{d0}}
\end{bmatrix} \tilde{x} + \begin{bmatrix}
0 & 0 \\
0 & 0
\end{bmatrix} \tilde{u}.
\tag{4.6}
\]

Where

\[
\dot{x} = \begin{bmatrix}
\Delta^e i_{cd} & \Delta^e i_{cq} & \Delta^e u_d & \Delta^e u_q & \Delta^e i_{gd} & \Delta^e i_{gq}
\end{bmatrix}^T,
\]

\[
\tilde{u} = \begin{bmatrix}
\Delta^e V_d^* & \Delta^e V_q^*
\end{bmatrix}^T,
\]

\[
y = \begin{bmatrix}
\Delta P & \Delta Q
\end{bmatrix}^T.
\]

The small-signal model of the inner loop current controllers are

\[
\Delta^e V_d^* = \Delta^e u_d - \omega L_c \Delta^e i_{cq} + k_{pd}(\Delta^e i_{cd} - \Delta^e i_{ca}) + k_{id}\Delta \gamma_d - \Delta v_{AD,d},
\tag{4.7}
\]

\[
\Delta^e V_q^* = \Delta^e u_q + \omega L_c \Delta^e i_{cd} + k_{pg}(\Delta^e i_{gq} - \Delta^e i_{cq}) + k_{iq}\Delta \gamma_q - \Delta v_{AD,q}.
\tag{4.8}
\]
4.3 Developing the small-signal model of the SRF-PLL based system

where

\[ \Delta \gamma_d = \int_0^t (\Delta^c i_{cd}^* - \Delta^c i_{cd})d\tau. \]

And the small-signal model of the active damping part is defined as

\[ \Delta v_{AD,d} = K_{AD}(\Delta^c u_d - \Delta \phi_d), \]

\[ \frac{d\Delta \phi_d}{dt} = \omega_{AD} \cdot \Delta^c u_d - \omega_{AD} \cdot \Delta \phi_d. \]

The small-signal model of the \( q \) component of the inner loop controller can be defined as

\[ \Delta^c V_q^* = \Delta^c u_q + \omega L_c \Delta^c i_{cd} + k_{pq}(\Delta^c i_{cq}^* - \Delta^c i_{cq}) + k_{iq} \Delta \gamma_q - \Delta v_{AD,q}, \quad (4.8) \]

where

\[ \Delta \gamma_q = \int_0^t (\Delta^c i_{cq}^* - \Delta^c i_{cq})d\tau. \]

And the small-signal model of the active damping part is defined as

\[ \Delta v_{AD,q} = K_{AD}(\Delta^c u_q - \Delta \phi_q), \]

\[ \frac{d\Delta \phi_q}{dt} = \omega_{AD} \cdot \Delta^c u_q - \omega_{AD} \cdot \Delta \phi_q. \]
The outer loop controllers are defined as

\[
\Delta^c i_d^* = K_{Pp}(\Delta P^* - \Delta P_m) + K_{Pq}\Delta\gamma_P, \tag{4.9}
\]

where

\[
\Delta\gamma_P = \int_0^t (\Delta P^* - \Delta P_m) d\tau.
\]

\[
\frac{d\Delta P_m}{dt} = \omega_p \cdot \Delta P - \omega_p \cdot \Delta P_m = \omega_p(\epsilon_{gd0}\Delta^c u_d + \epsilon_{gq0}\Delta^c u_q + \epsilon u_{d0}\Delta^c i_gd + \epsilon u_{q0}\Delta^c i_gq) - \omega_p \cdot \Delta P_m.
\]

The mathematical model of the \( q \) component of the outer loop controller which controls the magnitude of the voltage \( u \) at the point of common coupling (PCC) can be defined as

\[
\Delta^c i_q^* = K_{Up}(\Delta U^* - \Delta U_m) + K_{Uq}\Delta\gamma_U, \tag{4.10}
\]

where

\[
\Delta\gamma_U = \int_0^t (\Delta U^* - \Delta U_m) d\tau.
\]

The mathematical model of the applied low-pass filter on the voltage magnitude is

\[
\frac{d\Delta U_m}{dt} = \omega_U \cdot \Delta U - \omega_U \cdot \Delta U_m = \frac{\omega_U}{U_0}(\Delta^c u_d \cdot \epsilon u_{d0} + \Delta^c u_q \cdot \epsilon u_{q0}) - \omega_U \cdot U_m
\]
4.3 Developing the small-signal model of the SRF-PLL based system

and the SRF-PLL model is

\[
\frac{d\Delta \theta_{PLL}}{dt} = K_{pPLL}\Delta c_{u_q} + K_{iPLL}\Delta \gamma_{ PLL},
\]

(4.11)

where

\[
\Delta \gamma_{ PLL} = \int_0^t \Delta c_{u_q} \, d\tau.
\]

And the rotation matrices are

\[
\Delta^e M_e = \begin{bmatrix}
\cos \theta_{PLL} & -\sin \theta_{PLL} & (-c^*V_{do} \sin \theta_{PLL} - c^*V_{qo} \cos \theta_{PLL}) \\
\sin \theta_{PLL} & \cos \theta_{PLL} & (c^*V_{do} \cos \theta_{PLL} - c^*V_{qo} \sin \theta_{PLL})
\end{bmatrix}
\]

\[
\Delta^e M_{eu} = \begin{bmatrix}
\cos \theta_{PLL} & \sin \theta_{PLL} & (-e^u_{d0} \sin \theta_{PLL} + e^u_{q0} \cos \theta_{PLL}) \\
-e^u_{d0} \cos \theta_{PLL} & -e^u_{q0} \sin \theta_{PLL}
\end{bmatrix}
\]

\[
\Delta^e M_{ei} = \begin{bmatrix}
\cos \theta_{PLL} & \sin \theta_{PLL} & (-e^i_{d0} \sin \theta_{PLL} + e^i_{q0} \cos \theta_{PLL}) \\
-e^i_{d0} \cos \theta_{PLL} & -e^i_{q0} \sin \theta_{PLL}
\end{bmatrix}
\]

where

\[
\begin{bmatrix}
\Delta^e V^e_d \\
\Delta^e V^e_q
\end{bmatrix} = \Delta^e M_e \begin{bmatrix}
\Delta^e V^*_d \\
\Delta^e V^*_q \\
\Delta^e \theta_{PLL}
\end{bmatrix}, \quad \begin{bmatrix}
\Delta^e c_{u_d} \\
\Delta^e c_{u_q}
\end{bmatrix} = \Delta^e M_{eu} \begin{bmatrix}
\Delta^e c_{u_d} \\
\Delta^e c_{u_q}
\end{bmatrix}, \quad \begin{bmatrix}
\Delta^e \theta_{PLL}
\end{bmatrix}
\]
The state-space model of the main circuit, the inner loop controllers, the outer loop controllers and the rotation matrices are all combined in an overall linearised state-space matrix form as

\[
\Delta \dot{x} = A \cdot \Delta x + B \cdot \Delta u, \\
\Delta y = C \cdot \Delta x + D \cdot \Delta u.
\]

where

\[
A = \begin{bmatrix}
\alpha_{11} & \alpha_{12} & -\frac{R_c}{L_c} & 0 & 0 & 0 & 0 & 0 \\
\alpha_{21} & \alpha_{22} & 0 & -\frac{R_c}{L_c} & 0 & 0 & 0 & 0 \\
0 & 0 & \omega & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & \omega & 0 & 0 & 0 & 0 \\
\frac{1}{\tau_f} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
\frac{1}{\tau_f} & 0 & -\frac{1}{\tau_f} & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & -\frac{1}{\tau_f} & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & \frac{1}{\tau_f} & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
\end{bmatrix}
\]

\[
a_{1,1} = \alpha_1 \cos \theta_{PLL0} - \alpha_2 \sin \theta_{PLL0} - \frac{R_c}{L_c},
\]

\[
a_{1,2} = \alpha_3 \cos \theta_{PLL0} - \alpha_4 \sin \theta_{PLL0} + \omega,
\]

\[
a_{2,1} = \alpha_1 \sin \theta_{PLL0} + \alpha_2 \cos \theta_{PLL0} - \omega,
\]

\[
a_{2,2} = \alpha_3 \sin \theta_{PLL0} + \alpha_4 \cos \theta_{PLL0} - \frac{R_c}{L_c},
\]

\[
a_{7,9} = \epsilon_i_{cd0} \sin \theta_{PLL0} - \epsilon_i_{cq0} \cos \theta_{PLL0},
\]

\[
a_{8,9} = \epsilon_i_{cq0} \sin \theta_{PLL0} + \epsilon_i_{cd0} \cos \theta_{PLL0},
\]
4.3 Developing the small-signal model of the SRF-PLL based system

\[ \alpha_1 = \omega \sin \theta_{PLL0} - \frac{1}{L_c} k_{pd} \cos \theta_{PLL0}, \]
\[ \alpha_2 = \frac{1}{L_c} (\omega L_c \cos \theta_{PLL0} + k_{pq} \sin \theta_{PLL0}), \]
\[ \alpha_3 = -\omega \cos \theta_{PLL0} - \frac{1}{L_c} k_{pd} \sin \theta_{PLL0}, \]
\[ \alpha_4 = \frac{1}{L_c} (\omega L_c \sin \theta_{PLL0} - k_{pq} \cos \theta_{PLL0}), \]
\[ \alpha_5 = k_{id} \frac{1}{L_c} \cos \theta_{PLL0}, \]
\[ \alpha_6 = k_{iq} \frac{1}{L_c} \sin \theta_{PLL0}, \]
\[ \alpha_7 = \frac{1}{L_c} (\cos \theta_{PLL0} (\partial V_{dref}^c / \partial \theta |_{x=x_0}) - (V_{dref}^c |_{x=x_0}) \sin \theta_{PLL0} - \sin \theta_{PLL0} (\partial V_{qref}^c / \partial \theta |_{x=x_0}) - (V_{qref}^c |_{x=x_0}) \cos \theta_{PLL0}), \]
\[ \alpha_8 = \frac{1}{L_c} (\sin \theta_{PLL0} (\partial V_{dref}^c / \partial \theta |_{x=x_0}) + (V_{dref}^c |_{x=x_0}) \cos \theta_{PLL0} + \cos \theta_{PLL0} (\partial V_{qref}^c / \partial \theta |_{x=x_0}) - (V_{qref}^c |_{x=x_0}) \sin \theta_{PLL0}), \]
\[ \alpha_9 = K_{pPLL} \sin \theta_{PLL0}, \]
\[ \alpha_{10} = K_{pPLL} \cos \theta_{PLL0}, \]
\[ \alpha_{11} = -e_{uq0} K_{pPLL} \sin \theta_{PLL0} - e_{ud0} K_{pPLL} \cos \theta_{PLL0}, \]
\[ \alpha_{12} = \omega_{AD} (-e_{uq0} \sin \theta_{PLL0} + e_{ud0} \cos \theta_{PLL0}), \]
\[ \alpha_{13} = \omega_{AD} (-e_{uq0} \cos \theta_{PLL0} - e_{ud0} \sin \theta_{PLL0}), \]
\[ \alpha_{14} = \frac{\omega_{AD}}{K_{pPLL}}. \]

\[
B = \begin{bmatrix}
\frac{1}{L_c} k_{pd} K_{pP} \cos \theta_{PLL0} & \frac{1}{L_c} k_{pd} K_{UP} \sin \theta_{PLL0} & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\
\frac{1}{L_c} k_{pq} K_{pP} \sin \theta_{PLL0} & -\frac{1}{L_c} k_{pq} K_{UP} \cos \theta_{PLL0} & 0 & 0 & 0 & 0 & 0 & -K_{UP} & 0 & 0 & 0 & 1 & 0 & 0
\end{bmatrix}^T,
\]

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The developed small-signal model is validated by comparing its time-domain response with the nonlinear model’s one, where the experiment is conducted by applying a step change into the reference input signal $\Delta P^* = 0.2$ p.u at time=1 sec. Figures 4.6-4.8 and Figures B.5-B.10 in Appendix B are the results experiment.

![Comparison of $e_{u_d}$ for linear and nonlinear mathematical models for the SRF-PLL based converter](image)

**Fig. 4.6** Comparison of $e_{u_d}$ for linear and nonlinear mathematical models for the SRF-PLL based converter
4.3 Developing the small-signal model of the SRF-PLL based system

Fig. 4.7 Comparison of $\epsilon_{u_q}$ for linear and nonlinear mathematical models for the SRF-PLL based converter

Fig. 4.8 Comparison of $\theta_{PLL}$ for linear and nonlinear mathematical models for the SRF-PLL based converter
Figures 4.6-4.8 and Figures B.5-B.10 in Appendix B show that the small signal state space model is satisfactorily validated, where the responses for both linearised state space model and nonlinear model are identical.

The nonlinear mathematical model of the DF-PLL and IC-PLL based converters are also derived by using the same procedure that is used for the derivation of the mathematical model of the converter that uses SRF-PLL, with considering the mathematical model of the DF-PLL as given in equations 3.18-3.19, and for the IC-PLL as given in equations 3.20-3.21 in Chapter 3. Therefore, the detailed derivation procedures for the DF-PLL and IC-PLL are not presented in the chapter. The final state-space models for the DF-PLL and IC-PLL based systems are attached in Appendix A. The time-domain responses results for the validations of the nonlinear models are attached in Appendix B, Figures B.11-B.22 for the IC-PLL based system nonlinear model, and Figures B.29-B.33 for the DF-PLL based system nonlinear model. The validations of the linearised models are attached in Appendix B, Figures B.23-B.28 for the IC-PLL, and Figure B.34-B.41 for DF-PLL. All the results show that the nonlinear models and the linearised models are valid, as the compared time-domain responses are very similar.

4.4 Conclusion

This chapter describes the methods that are used to develop the analytical model for the VSC-HVDC utilises any type of PLL. The nonlinear mathematical model of the SRF-PLL based system is derived based on two approaches. The nonlinear mathematical models are validated by comparing their time-domain responses with the simulation of the overall system realised using MATLAB’s SimPowerSystem toolbox. The method that is corresponded to the validated mathematical model is chosen as an approach to develop the model of any type of PLL based system. The small-signal
model is then obtained and validated by linearising the nonlinear mathematical model around an operating point so that this model is used to study the static stability and the dynamic response of the system. The results show that all the nonlinear mathematical models and the linearised models are valid, as the compared time-domain responses are very similar.
Chapter 5

Static Stability and Dynamic Performance Studies for VSC-HVDC Converter Utilising Various Types of PLLs

5.1 Introduction

In this chapter, the static power transfer capability and the dynamic performance of the different converters utilise different types of PLL, SRF-PLL, DF-PLL and IC-PLL are considered. The design parameters for different types of PLLs, namely, virtual impedance value $Z_v$ for IC-PLL, damping factor $D$ for DF-PLL and PLL low pass filter $\omega_{FL,PLL}$ for IC-PLL, DF-PLL and SRF-PLL, determine the dynamic characteristics of the utilised PLL. Hence, these parameters have a considerable impact on the operation of the VSC-HVDC system, consequentially, reflecting on the static stability and dynamic performance of the system. Therefore, the effect of each parameter on the power
transfer capability and the dynamic performance is investigated in this chapter. Section 5.2 provides a general explanation about the operation limits of the VSC-HVDC system. Section 5.3 is devoted to a general comparison between different converters utilise different types of PLLs in terms of stability limits. The impacts of PLLs’ parameters on the stability limits for different types of PLLs are given in Section 5.4. The dynamic performance study of the system utilises IC-PLL is considered in Section 5.5, and finally, Section 5.6 is the conclusion of the chapter.

5.2 Operation limits of the VSC-HVDC System

The operation limit is defined in terms of the maximum power that the VSC converter can transfer in steady-state while maintaining the stability of the system. For a general power system consisting of two voltage sources $u$ and $e$, interconnected via impedance $Z_g = R_g + jX_g$, as shown in Figure 5.1, there is a theoretical maximum power that is considered the theoretical operation limit that cannot be exceeded [69]. This theoretical maximum power is given by

$$P_{\text{max}}(\text{p.u.}) = \frac{U \cdot E}{|Z_g|} \pm U^2 \frac{R_g}{|Z_g|^2},$$

(5.1)

where all the values of the voltages and the AC circuit parameters are in per-unit quantities, and the sign ‘+’ is for the inverter operation and ‘-’ is for the rectifier operation.

However, the VSC-HVDC system may not be able to transfer power equals to the theoretical maximum power $P_{\text{max}}$, which is due to the presence of the feedback element, where the dynamic of this element may affect on the stability of the system. Therefore,
in the case of the VSC-HVDC system shown in Figure 2.1, $P_{\text{max}}$ represents the maximum power that is transferred between the voltage $u$ at PCC and the voltage $e$ at the infinite bus and $P_{\text{max}} \leq P_{\text{max}}$.

\[ L_g R_g i_g + u \]

Fig. 5.1 Simplified AC circuit model

5.3 Stability limits of the VSC-HVDC System

In order to study the stability of the system for various types of PLLs, the operating points of the system are obtained first. The operating points are calculated by setting $f(x_0) = 0$, which are solved numerically to find solutions, where the $f(x)$ is the set of the nonlinear equations 4.3 that were derived in Chapter 4. The maximum theoretical power that is calculated by equation 5.1 for a certain value of the grid impedance is approximately equal to the maximum power by which the nonlinear equations return real solution. However, the system may not be able to operate according to the calculated operating points, i.e. these operating points are unstable. The operating points $x_0$ are considered stable if all the eigenvalues of the matrix $A$, which is obtained based on $x_0$ from Chapter 4, has negative real parts, where this method is referred as the first method of Lyapunov [70].

The first method of Lyapunov is a small signal stability analysis which identifies the maximum active power that the system can transfer with retaining the stability of the system. The results of the small signal stability analysis for different types of PLLs are shown in Figure 5.2, where $U^* = 1$ p.u. for $Z_g = [0.1, 1]$ p.u. and $\omega_{FL,PLL} = 400$ rad/sec.
5.3 Stability limits of the VSC-HVDC System

![Graph showing stability limits for SRF-PLL, DF-PLL and IC-PLL based system.](image)

Fig. 5.2 Small signal stability limits for SRF-PLL, DF-PLL and IC-PLL based system.

Figure 5.2 shows the stability limits for SRF-PLL, DF-PLL and IC-PLL for different values of grid impedance $Z_g$. Note that the VSC converter that relies on SRF-PLL or DF-PLL is not able to reach the maximum theoretical power for the inverter and rectifier operation and for any value of the grid impedance $Z_g$. Conversely, the VSC converter that utilises IC-PLL is capable of almost reaching the theoretical maximum power transfer given in Equation (5.1). This is because the VSC converter that utilises IC-PLL is synchronised to the infinite bus voltage $e$, since $Z^e_g = Z_g$, whose frequency is fixed and, therefore, whose phase angle is independent of the phase angle perturbations of other voltages in the power system. Therefore, the interaction between the grid synchronisation and power flow control is minimised. In addition, for the inverter and rectifier operations, the maximum transferred power for the converter that relies on DF-PLL does not improve as it delivers approximately the same amount of power that the SRF-PLL based converter does.
5.4  Impact of tuning the PLLs’ parameters on the transferred power capability

The impacts of the tuning the parameters of SRF, DF-PLL and IC-PLL on the transferred maximum power are presented in this section. These parameters are the virtual impedance value $Z^v_g$ for the IC-PLL, D for the damping factor PLL, and PLL low pass filter $\omega_{FL,PLL}$ for the IC-PLL, DF-PLL and SRF-PLL (which is IC-PLL with $Z^v_g = 0$). When the value of the low pass filter bandwidth $\omega_{FL,PLL}$ changes, the values of the PI controller gains change accordingly. The value of the low pass filter $\omega_{FL,PLL}$ is related to the bandwidth of the PLL PI controller $\omega_{co} = 0.55\omega_{FL,PLL}$; $\omega_{co}$ is the bandwidth of the PLL PI controller, and this is due to the symmetrical optimum tuning method (which is presented in Appendix C)[26].

5.4.1  The impact of tuning the values of $D$ and $\omega_{FL,PLL}$ on the transferred power capability for the DF-PLL based system

In this section the effects of tuning the values of $D$ and $\omega_{FL,PLL}$ for the DF-PLL on the transferred power are considered. The small signal stability analysis is conducted for each value in a range of $Z^v_g = 0.2, 0.4, 0.8, 2$ p.u., $\omega_{FL,PLL} = 100, 200, 400, 800, 1000$ rad/sec and for $D = [0, 500]$ for the inverter operation and $D = -[0, 500]$ for the rectifier operation. The results are plotted in Figures 5.3-5.6.
5.4 Impact of tuning the PLLs’ parameters on the transferred power capability

Fig. 5.3 Maximum power transfer for DF-PLL for different values of $\omega_{FL,PLL}$, for a range of $D$ and for $Z_g = 0.2$ p.u.

In Figure 5.3 a range of the damping factor $|D| = [0 \quad 500]$ is considered and for the range of PLL low pass filter $\omega_{FL,PLL} = 100, 200, 400, 800$ and $1000$ rad/sec for the case of $Z_g = 0.2$ p.u. It is clear that the converter that utilises DF-PLL is not able to reach the theoretical maximum power for that of the value of $Z_g = 0.2$ p.u. In addition, for the inverter and rectifier operations, and for the value of $\omega_{FL,PLL} = 100, 200$ and $400$ rad/sec the results show that as the value of $D$ increases the maximum power decreases. The results also show that for the inverter operation, and as the value of $\omega_{FL,PLL}$ increases, the maximum power increases for the same range of the damping factor $D$. In comparison between inverter operation and rectifier operation for the case of $\omega_{FL,PLL} = 800, 1000$ rad/sec, the results show that the effect of increasing the value of $D$ on the maximum power transfer is insignificant for the case of inverter operations. On the contrary, for the case of the rectifier operation, the increase in the value of $D$ has a significant impact on the maximum power transfer, where the value of maximum power increases as the value of $D$ increases.
Static Stability and Dynamic Performance Studies for VSC-HVDC Converter Utilising Various Types of PLLs

Fig. 5.4 Maximum power transfer for DF-PLL for different values of $\omega_{FL,PLL}$, for a range of $D$ and for $Z_g = 0.4$ p.u.

The results in Figure 5.4 are for the case of $Z_g = 0.4$ p.u. and for the inverter and rectifier operations for the range of $|D| = [0 \ 500]$ and $\omega_{FL,PLL} = 100, 200, 400, 800$ and $1000$ rad/sec. The behaviour of the system to the changing in the value of $\omega_{FL,PLL}$ and $D$ is similar to that one for the case of $Z_g = 0.2$ p.u. which is presented in Figure 5.3. However, the only difference is that in the case of the rectifier operation for $Z_g = 0.4$ and for frequency $\omega_{FL,PLL} = 800$ rad/sec the results in Figure 5.4 (b) show that the maximum power slightly decreases when $|D| = 200$.

Fig. 5.5 Maximum power transfer for DF-PLL for different values of $\omega_{FL,PLL}$, for a range of $D$ and for $Z_g = 0.8$ p.u.

For the case of $Z_g = 0.8$ p.u. the results are represented in Figure 5.5 and for the same ranges of $D$ and $\omega_{FL,PLL}$ that used to produce the results in Figure 5.3-5.4. For
5.4 Impact of tuning the PLLs’ parameters on the transferred power capability

the inverter and rectifier operations, the results show that as the value of D increases the maximum power decreases for the case of $\omega_{FL,PLL} = 100$ and 200 rad/sec. In the case of $\omega_{FL,PLL} = 400$ rad/sec and for the inverter operation, the results in Figure 5.5 (a) shows that there is an insignificant increase in the maximum power transfer in the range of $D= [100 \ 400]$. On the contrary, for the rectifier operation and when the value of $|D|= 200$ and $\omega_{FL,PLL} = 400$ rad/sec, the results in Figure 5.5 (b) shows that the transferred power slightly reduces below $P= -0.85$ p.u. For the high frequency PLL low pass filter $\omega_{FL,PLL} = 1000$ rad/sec the results in Figure 5.5 (a) shows that the maximum power is increasing almost linearly as the value of D increases to reach the maximum power which is slightly above $P= 1$ p.u. when $D= 500$. However, for the rectifier operation, the results in Figure 5.5 (b) shows that the increase in the value of D has no effect on the maximum power transfer for $\omega_{FL,PLL} = 1000$ rad/sec, which the same case of $\omega_{FL,PLL} = 800$ rad/sec for the inverter and rectifier operations.

![Fig. 5.6 Maximum power transfer for DF-PLL for different values of $\omega_{FL,PLL}$, for a range of $D$ and for $Z_g = 2$ p.u.](image)

(a) Inverter operation  
(b) Rectifier operation

For the case of $Z_g = 2$ p.u. which is represented in Figure 5.6, the results show that the maximum power reduces as the value of D increases for $\omega_{FL,PLL} = 100$, and 200 rad/sec and for the inverter and rectifier operations. For $\omega_{FL,PLL} = 400$ rad/sec and for the inverter and rectifier operations, the results show that there is no significant changing in the maximum power transfer as the value of D increases. For the case
of $\omega_{FL,PLL} = 800$ rad/sec the results in Figure 5.6(a) show that there is a significant increase in the value of the maximum power from $P = 0.15 \rightarrow 0.4$ p.u., which is slightly larger than the SRF-PLL based system can transfer, as the value of damping factor increase for $D = 0 \rightarrow 270$. However, for $\omega_{FL,PLL} = 800$ rad/sec, there is no changing in the maximum power as the value of $D$ increases in the case of rectifier operation, which is the same case of $\omega_{FL,PLL} = 1000$ rad/sec. Where both frequencies are transferring the same amount of power which is equal to the SRF-PLL can transfer. For the $\omega_{FL,PLL} = 1000$ rad/sec and for the inverter operation and for the whole range of $D$, the results in Figure 5.6 (a) show the transferred power is far less than the power that SRF-PLL with $\omega_{FL,PLL} = 400$ rad/sec can transfer, it is $P = 0.13$ p.u. for the DF-PLL compared to $P = 0.38$ p.u. for SRF-PLL.

5.4.2 The impact of selecting the values of $Z^v_g$ and $\omega_{FL,PLL}$ on the power transfer capability for the IC-PLL based system

To further illustrate how the value of the compensated grid impedance, namely the virtual impedance, is influencing the power transfer capability for different values of the grid impedance, the stability limits for three selecting values of the virtual impedance are chosen 50 %, 70% and 200% of the grid impedance, and the result are presented in Figure 5.7-5.9.
5.4 Impact of tuning the PLLs’ parameters on the transferred power capability

Fig. 5.7 Maximum power for SRF-PLL and IC-PLL ($Z_g^v = 0.5Z_g$), and for $\omega_{FL,PLL} = 400$ rad/sec.

Fig. 5.8 Maximum power for SRF-PLL and IC-PLL ($Z_g^v = 0.7Z_g$), and for $\omega_{FL,PLL} = 400$ rad/sec.
In general, for the rectifier operation, the transfer power capability is improved when the converter utilises IC-PLL, and this is true for each selected value of the $Z^v_g$, where the power transfer is approximately equal to the maximum theoretical power. For the three values of the virtual impedance and for the inverter operation, the power transfer capability is also improved. When $Z^v_g = 0.5Z_g$ (Figure 5.7) and for the entire range of the grid impedance $Z_g = [0.2 \, 2]$ p.u., for the inverter operation the converter that relies on the IC-PLL has the ability to transfer power larger than the SRF-PLL does, however, the transferred power is less than the maximum theoretical one. For the inverter operation, as the value of the virtual impedance increases, i.e. in the case of $Z^v_g = 0.7Z_g$ (Figure 5.8), the power transfer capability is enhanced in the case of $Z_g \leq 1.2$ p.u. to be equal to the maximum theoretical power, and it is not exhibiting a significant improvement for the value of the grid impedance $Z_g > 1.2$ p.u. When the value of the virtual impedance is twice times the value of the grid impedance $Z^v_g = 2Z_g$ (Figure 5.9) the power transfer capability for the IC-PLL increases to be

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Fig. 5.9 Maximum power for SRF-PLL and IC-PLL ($Z^v_g = 2Z_g$), and for $\omega_{FL,PLL} = 400$ rad/sec.
5.4 Impact of tuning the PLLs’ parameters on the transferred power capability

equal to the value of the theoretical one for most of the range of the grid impedance, except for the value of the grid impedance $Z_g < 0.4$ p.u., where the maximum power capability decreases. Therefore, from the presented results in Figure 5.7-5.9, it can be concluded that increasing the value of the power transfer capability when the value of the virtual impedance increases does not have a certain characteristic for the entire range of the grid impedance, and this is particularly challenging in the case of the variable grid impedance. In addition, the dynamic performance of the system depends on the selection of the virtual impedance, and this is will be considered in Section 5.5.

The main requirement in the converter operation that utilises IC-PLL is to have prior knowledge about the value of the grid impedance, and that requires, as will be explained in the next chapter, estimation techniques to measure the value of the grid impedance. The task of the grid estimation becomes more challenging in the case of the variation in the value of the grid impedance. Therefore, a study on stability limits are considered for the converter utilises IC-PLL in the case of the inaccurate estimation for the value of the grid impedance, which might be a particular case of changing in the value of the grid impedance. While the value of the grid impedance is varying, there is no updating in the value of virtual impedance, accordingly. In addition, the PLL parameters, namely PLL low pass filter $\omega_{FL,PLL}$, as it is mentioned before it is related to the PI bandwidth, also have an impact on the static stability limits of the IC-PLL. Therefore, the effects of these parameters on the stability are evaluated for different values of grid impedance. Figure 5.10-5.13 represent the stability limits, which are determined based on the small signal stability, for values of the grid impedance $Z_g = 0.2, 0.4, 0.8$ and 2 p.u., respectively, and for inverter and rectifier operations. Each curve in these figures are plotted as a function of the ratio $Z_v/Z_g = 0 \rightarrow 3$. 

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where each curve represents one value of $\omega_{FL,PLL}$ and these values are 100, 200, 400, 800 and 1000 rad/sec.

![Graph](image-url)

(a) Inverter operation  
(b) Rectifier operation

Fig. 5.10 Maximum power for IC-PLL for different values of $\omega_{FL,PLL}$ for a range of $Z_g^v$ and for $Z_g = 0.2$ p.u.

The curves in Figure 5.10 show the stability limits for the value of the grid impedance $Z_g = 0.2$ p.u., and for the rectifier and inverter operations. In general, the results in Figure 5.10 show that for all values of $\omega_{FL,PLL}$ and as the value of the virtual impedance increases, the stability limits of the system in the inverter and rectifier operation are enhanced to reach the highest value of the transferred power at a certain range of value of the virtual impedance. Then, as this value increases the value of the transferred power decreases. In addition, for the inverter operation and for the SRF-PLL (IC-PLL with $Z_g^v/Z_g = 0$), the stability limits for the value of $\omega_{FL,PLL} = 1000$ rad/sec is lower than the other values of $\omega_{FL,PLL}$ which are approximately equal. For the rectifier operation, the results in Figure 5.10 (b) show that for the high value of the PLL bandwidth $\omega_{FL,PLL} = 800, 1000$ rad/sec, the converter provides the lowest stability limits in the case of SRF-PLL.

The curves also show how the value of the stability limits increases linearly for the low values of the $\omega_{FL,PLL} = 100, 200, 400$ rad/sec to reach the highest value which is equal to the theoretical power for the range of ratio of $0.5 \leq Z_g^v/Z_g \leq 1.2$. However, in the case of the high frequency $\omega_{FL,PLL} = 800, 1000$ rad/sec the converter can transfer power
5.4 Impact of tuning the PLLs’ parameters on the transferred power capability

equal to the theoretical power in a range of the virtual impedance ratio $1 \leq \frac{Z_v}{Z_g} < 1.8$ for the inverter operation. For the rectifier operation, the results in Figure 5.10 (b) show that the converter with a high frequency of $\omega_{FL,PLL}$ is not able to reach the theoretical power value for any value of the virtual impedance.

![Graph](image)

Fig. 5.11 Maximum power for IC-PLL for different values of $\omega_{FL,PLL}$ for a range of $Z_v$ and for $Z_g = 0.4$ p.u.

Figure 5.11 show the results of the stability limits for the case of the grid impedance $Z_g = 0.4$ p.u. For the converter with a low value of the low pass filter $\omega_{FL,PLL} = 100, 200, 400$ rad/sec, the stability limits increase steadily as the value of the virtual impedance increases, to reach the theoretical maximum power at the value of $Z_v/Z_g = 0.5$ for both cases of inverter and rectifier operations. For the high value of the low pass filter $\omega_{FL,PLL} = 800, 1000$ rad/sec, the curves in Figure 5.11 show that the transferred power is changing nonlinearly when the value of the virtual impedance increases. Where the value of the stability limits decrease in the inverter operation, then the curves increase to reach the maximum theoretical power when $Z_v/Z_g \geq 1$, and $Z_v/Z_g > 2.4$ for the rectifier operation.
The curves in Figure 5.12 represent the stability limits for the case of the grid impedance $Z_g = 0.8$ p.u., i.e. very weak grid connection with SCR = $1/0.8 = 1.25$. For the inverter operation and for the high values of the low pass filter $\omega_{FL.PLL} = 800, 1000$ rad/sec, the curves in Figure 5.12 (a) show that the system has similar trends for their stability limits to their equivalences of the case of $Z_g = 0.4$ p.u. In the case of the value of $\omega_{FL.PLL} = 100, 200, 400$ rad/sec, the curves show that the stability limits increase linearly as the value of the virtual impedance increases to reach the maximum theoretical power when $Z_v^g/Z_g \geq 0.4$ for $\omega_{FL.PLL} = 200$ rad/sec, $Z_v^g/Z_g \geq 0.5$ for $\omega_{FL.PLL} = 100$ rad/sec and $Z_v^g/Z_g = 0.6$ for $\omega_{FL.PLL} = 400$ rad/sec.

For the rectifier operation, the curves in Figure 5.12 (b) show that in the case of SRF-PLL (IC-PLL with $Z_v^g/Z_g = 0$) all the values of the PLL low pass filter have the approximately same value of the stability limits $P \simeq -0.85$ p.u. When the value of the virtual impedance increases, the value of the maximum power transfer is increasing linearly for the low value of the low pass filter $\omega_{FL.PLL} = 100, 200, 400$ rad/sec to reach the theoretical maximum power at $Z_v^g/Z_g \simeq 0.5$. However, for the case of the high value of the low pass filter $\omega_{FL.PLL} = 800$ rad/sec, the results in Figure 5.12 (b) show that the stability limit reaches the maximum theoretical power in two points of $Z_v^g/Z_g$. The first point, the system critically reaches the theoretical maximum power
5.4 Impact of tuning the PLLs’ parameters on the transferred power capability

at a single value of $Z_g^v/Z_g = 0.7$, then the value of the maximum power reduces again when the value of the virtual impedance increases, and the second point is for the value of $Z_g^v/Z_g \geq 1.9$. However, for the value of PLL low pass filter $\omega_{FL,PLL} = 1000$ rad/sec, the stability limit reaches the maximum theoretical power for the value of $Z_g^v/Z_g \geq 2.1$.

![Fig. 5.13 Maximum power for IC-PLL for different values of $\omega_{FL,PLL}$ for a range of $Z_g$ and for $Z_g = 2$ p.u.](image)

The curves in Figure 5.13 represent the stability limits for the value of the grid impedance $Z_g = 2$ p.u., which is the case of the very weak grid connections with $SCR = 1/2 = 0.5$ for the inverter and rectifier operations. For the low value of the PLL low pass filter $\omega_{FL,PLL} = 100, 200$ rad/sec the trends of the curves show that the stability limits increase linearly as the value of the virtual impedance increases, to reach the maximum theoretical power when $Z_g^v/Z_g \geq 0.5$ for both inverter and rectifier operations. In the case of $\omega_{FL,PLL} = 400, 800, 1000$ rad/sec, the results show that the increasing in the values stability limits occur nonlinearly, to reach the maximum theoretical power when $Z_g^v/Z_g \geq 0.9$ for $\omega_{FL,PLL} = 400$ rad/sec, $Z_g^v/Z_g \geq 1.7$ for $\omega_{FL,PLL} = 800$ rad/sec and $Z_g^v/Z_g \geq 1.9$ for $\omega_{FL,PLL} = 1000$ rad/sec for the inverter operation. For the rectifier operation, the system with different values of the $\omega_{FL,PLL}$ can reach the maximum theoretical power at different points of the ratio $Z_g^v/Z_g$. For the value of $\omega_{FL,PLL} = 400$ rad/sec, it approaches the maxi-
mum power at two different regions $Z^v_g/Z_g = [0.5, 0.7] \cup Z^v_g/Z_g \geq 1.2$ as it shown in Figure 5.13 (b). And for the value of $\omega_{FL,PLL} = 800$ rad/sec it attains the maximum power at $Z^v_g/Z_g = [0.5, 0.7] \cup Z^v_g/Z_g \geq 1.7$, and for $\omega_{FL,PLL} = 1000$ rad/sec is $Z^v_g/Z_g = [0.6, 0.8] \cup Z^v_g/Z_g \geq 1.8$.

Figures 5.10-5.13 reveal how increasing the value of the PLL low pass filter, which increasing the bandwidth of the PI controller accordingly, can provoke the instability of the system. However, this effect is less noticeable for the large value of the virtual impedance, in which the converter can reach the maximum theoretical power, even the value of the PLL low pass filter is very large. In order to understand this behaviour, the eigenvalues trajectories for the value of $Z_g = 0.8$ p.u. and two values of virtual impedance $Z^v_g = Z_g$ and $Z^v_g = 2Z_g$ are considered, for the range of $\omega_{FL,PLL} = 50 \rightarrow 2000$ rad/sec, and the results are presented in Figure 5.14

![Fig. 5.14 Loci of the closed-loop system's poles for the range of $\omega_{FL,PLL}$](image)

In Figure 5.14 two pairs of trajectories, each pair represent complex conjugate poles $\lambda_{3,16}$ and $\lambda_{2,17}$. The reason that only these eigenvalues are chosen is that they have more rapidly changed locations in the s-plane compared to other closed loop poles. It is clear from Figure 5.14 that dominant poles are different for different values of the virtual impedance $Z^v_g$. They are $\lambda_{3,16}$ for the value of $Z^v_g = Z_g$, and it is clear the
system becomes unstable when $\omega_{FL,PLL} > 750$ rad/sec, and in the case of $Z_g^v = 2Z_g$ the dominant poles are $\lambda_{2,17}$ which become unstable for $\omega_{FL,PLL} > 1400$ rad/sec. Based on participation matrix (the details about the participation matrix is included in Appendix C) the eigenvalues $\lambda_{3,16}$ have a highest participation factors with the states $\theta_{PLL}$ and the virtual voltage $u_{vqf}$, i.e. the stability of the system is more sensitive to the states that is associated to the IC-PLL. Unlike the case of the $Z_g^v = 200\%Z_g$, where the dominant poles are $\lambda_{2,17}$, which is based on the participation factor is more related to the states $e_{iq}$ and $e_{uq}$, i.e. as the value of the virtual impedance increases the dominant poles migrate from poles’ related PLL to non-related PLL’s ones. Therefore, the effect of increasing the value of $\omega_{FL,PLL}$ on the stability of the system for the high value of the virtual impedance IC-PLL is reduced.

5.5 Dynamic performance study of VSC-HVDC system that utilises IC-PLL

It has been shown in the previous section that IC-PLL has the ability to extend the stability limits of the VSC-HVDC system so that the transferred power can meet its theoretical maximum for certain range of virtual impedance $Z_g^v$ and PLL low pass filter bandwidth $\omega_{FL,PLL}$. In this section, the dynamic performance of the VSC-HVDC system that utilises IC-PLL is considered. In particular, the effect of selecting the value of the PLL low pass filter $\omega_{FL,PLL}$ and the virtual impedance $Z_g^v$ on the dynamic performance of the system. From Section 5.4.1 it has been shown that introducing DF-PLL does not improve the maximum power transfer, and the DF-PLL based system has approximately the same amount of the transferred power to the SRF-PLL based system. Therefore, the dynamic performance study only considers the IC-PLL based converter in this section.
5.5.1 The effect of selecting the value of $\omega_{FL,PLL}$ on the dynamic performance of IC-PLL based system

In this subsection, the effect of selecting the value of PLL low pass filter bandwidth on dynamic performance is investigated. Figure 5.14 shows how increasing the value of the $\omega_{FL,PLL}$ has an effect on the dynamic performance of the system. It is clear that as the value of the bandwidth increases, IC-PLL provides a faster tracking performance for the phase angle at the point of synchronisation, and this can be demonstrated from the shifting all the eigenvalues to the left of the imaginary axis. However, the increase in the bandwidth should be restricted, as it causes higher controller gains that, in turn, causes noise amplification, which provokes system instability. In order to understand the effect of the value of low pass filter $\omega_{FL,PLL}$ on the dynamic performance of the overall system, the sum of squares of errors (SSE) for the tracking of the active power is calculated for the value of $Z_g = [0.5 \ 0.9]$ p.u., where $Z_g^v = Z_g$ and for the range of $\omega_{FL,PLL} = [100 \ 700]$ rad/sec and the results is presented in Figure 5.15.

![Graph showing SSE for different values of PLL bandwidth](image)

**Fig. 5.15** SSE for the active power tracking for different values of PLL bandwidth, and for a range of $Z_g$.

The results in Figure 5.15 show that generally the SSE for different values of $Z_g$ decreases as the value of $\omega_{FL,PLL}$ increases, which indicates that the dynamic...
5.5 Dynamic performance study of VSC-HVDC system that utilises IC-PLL

performance is enhanced for the larger value of $\omega_{FL,PLL}$. However, for a different value of $Z_g$, the system has an optimal value of $\omega_{FL,PLL}$ at which the converter provides the optimal dynamic response. The larger the value of $Z_g$ the lower the optimal value of $\omega_{FL,PLL}$, for instant, for the value of $Z_g = 0.7$ p.u. the lowest value of SSE is when the value of $\omega_{FL,PLL} = 650$ rad/sec, and for $Z_g = 0.9$ p.u. the lowest value of SSE is when $\omega_{FL,PLL} = 550$ rad/sec. The extended plot of SSE for the value of $Z_g = 0.5$ p.u. is plotted in Figure 5.16 (a), where the minimum value of SSE is when the value of $\omega_{FL,PLL} = 750$ rad/sec, and the time response for selected values of $\omega_{FL,PLL}$ is plotted in Figure 5.16 (b).

![Fig. 5.16 SSE and time domain response for different values of $\omega_{FL,PLL}$, and for $Z_g = 0.5$ p.u.](image)

The time domain response in Figure 5.16 (b) shows how selecting the value of $\omega_{FL,PLL}$ affects the dynamic performance of the system. It is clear that time domain response in the case of $\omega_{FL,PLL} = 750$ rad/sec is far better than the case of $\omega_{FL,PLL} = 200$ rad/sec, which is less oscillatory in the case of $\omega_{FL,PLL} = 750$ rad/sec. It is worth mentioning that the results are presented in Figure 5.16 may not reflect the real operating point on which the convert is feasibly operating. This is because the value of the active power for the results presented in Figure 5.16 is $P > 1$ p.u., where the convert is not able to transfer power larger than the rated power of the system,
i.e. power of more than 1 p.u. Therefore, another result is presented in Figure 5.17 showing the time domain response of the active power, where the value of the grid impedance $Z_g = 1$ p.u., $Z_v = Z_g$

![Figure 5.17 Time domain response of the active power tracking for system with $Z_g = 1$ p.u.](image)

It is clear from Figure 5.17 that the time domain response in the case of $\omega_{FL,PLL} = 500$ rad/sec is better than the case of $\omega_{FL,PLL} = 200$ rad/sec, which is less oscillatory in the case of $\omega_{FL,PLL} = 500$ rad/sec.

### 5.5.2 The effect of selecting the value of $Z_v$ on the dynamic performance of IC-PLL based system

In this subsection, the effect of changing the value of $Z_v$ on the dynamic performance of the VSC converter that utilises IC-PLL is considered. A system with a value of $Z_g = 0.8$ p.u. is selected for the study as an example of the system with a very low SCR (very weak grid). The loci of the closed-loop system’s poles are plotted in Figure 5.18 for varying $Z_v$ from 0 p.u to 1.5 p.u., and the reference power equals to its theoretical maximum value which is equal to $P^* = 1.46$ p.u. The plotted eigenvalues are considered because they are more affected by varying the value of $Z_v$, as they have more shifting in their locations in the s-plane compared to the other closed-loop poles.
5.5 Dynamic performance study of VSC-HVDC system that utilises IC-PLL

Fig. 5.18 Loci of the closed-loop system’s poles for the range of $Z'_g$ from 0 p.u. to 1.5 p.u.

Figure 5.18 shows that as the value of the $Z'_g$ increases (the arrows indicate the direction of the poles’ loci as the $Z'_g$ increases) $\lambda_{3,7,8,16}$ shifts towards left, having negative real value for $Z'_g \geq 0.6$ p.u., which is consistent with the results in Figure 5.12(a) that shows VSC-HVDC system which utilises IC-PLL with $\omega_{FL,PLL} = 400$ rad/sec having the ability to transmit the power equal to its theoretical maximum value of $P_{max} = 1.46$ p.u. for $Z'_g \geq 0.6$ p.u. Results also show how the increase in the value of $Z'_g$ has a considerable shifting in the closed-loop poles. To investigate the dynamic response of the VSC-HVDC system in time-domain, the sum of squares of error (SSE) of the active power tracking is calculated for the range of values of $Z'_g/Z_g = [0.75, 3]$, and the results shown in Figure 5.19.
Static Stability and Dynamic Performance Studies for VSC-HVDC Converter Utilising Various Types of PLLs

Fig. 5.19 SSE and time domain response for different values of $Z_g^v$, and for $Z_g = 0.8$ p.u.

It is clear from the presented results in Figure 5.19 that the optimal dynamic performance in terms of SSE is achieved when $Z_g^v = Z_g$. In other words, the converter has the ability to transmit power with the optimal dynamic performance defined in terms of SSE provided that it is synchronised to the infinite bus voltage $e$, which represents stiff grid. The results also show that as the value of the virtual impedance exceeds the value of the grid impedance, the dynamic performance of the system starts to deteriorate. This is due to a high reactive power injection when using a value of the virtual impedance greater than the actual grid impedance, which results in longer closed-loop system’s settling time [26].

The dynamic performance of the system for a range of values of grid impedance $Z_g$ is also considered in this section for the inverter operation. For each value of $Z_g$ the SSE is calculated for the range of $Z_g^v$. The experiments are conducted with the value of the reference active power $P^*$ chosen to be equal to the maximum power that SRF-PLL can provide for each grid impedance value (shown as a red trend in Figure 5.2), and the value of the corresponding step change in reference power signal equal to $\Delta P^* = 0.01 \cdot P^*$. The result for the SSE is presented in Figure 5.20 for the
range of normalized values of $Z_{vg}^v$ for different values of $Z_g$.

Figure 5.20 shows the results of evaluating dynamic performance defined in terms of SSE of the VSC-HVDC system that employs IC-PLL for different values of grid impedance. These results show that for all values of $Z_g$ the SSEs have the same pattern, namely the best performance can be achieved for the range $Z_{vg}^v/Z_g = [0.9 \ 1.0]$. In addition, the highest value of SSE is reached when $Z_{vg}^v/Z_g = 0$, i.e. by replacing IC-PLL with SRF-PLL. Therefore, by introducing the virtual impedance term to the conventional SRF-PLL the dynamic performance of the closed-loop system begins to improve in addition to the improvements in the static power transfer stability. Due to the fact that the reference active power $P^*$ for each value of grid impedance is chosen to be equal to the highest power transfer capability that the SRF-PLL system can transfer, the calculated SSE is high for the small values of the grid impedance as the corresponding values of reference active power $P^*$ are high in these cases.
5.6 Conclusion

This chapter studies the maximum power transfer capability, and the dynamic performance of the converters utilise different types of PLLs. The PLLs parameters are chosen to investigate the maximum power transfer capability and the dynamic performance of the systems. These parameters are, \( \omega_{FL,PLL} \), \( D \) and \( Z_{vg} \). The results reveal that the converter that employs IC-PLL has the ability to transfer power equals to the theoretical maximum. In addition, introducing the DF-PLL does not improve the static stability, because the converter that utilises DF-PLL transfers approximately the same amount of the power that the SRF-PLL based converter does. The results in this chapter also show that for each value of \( Z_g \) there is a certain range of \( Z_{vg} \) that the converter can transfer power the same amount of the theoretical one. For the dynamic performance, the results show that for any value of \( Z_g \), the optimal dynamic performance can be achieved by IC-PLL with \( Z_{vg} = Z_g \).
Chapter 6

Adaptive IC-PLL (AIC-PLL) Based System

This chapter discusses the adaptive impedance conditioned phase-locked loop (AIC-PLL) utilised by VSC-HVDC system connected to a weak AC grid. As it was shown in Chapter 5, the impedance conditioned phase-locked loop (IC-PLL) has recently been proposed to address the issue of synchronisation with weak AC grid by supplementing the conventional synchronous reference frame phase-locked loop (SRF-PLL) with additional virtual impedance term. As a result, increasing the upper bound on the achievable power transfer achieved by the VSC converter connected to the weak grid [26]. However, the approach mentioned above is required for the grid impedance to be estimated accurately so that the virtual impedance branch compensates the high-value grid impedance. Hence, the VSC converter is synchronised to the point at the infinite bus voltage, where the voltage operates in a relatively robust manner concerning the perturbations that happen in the voltage at PCC. The task of grid synchronisation becomes particularly challenging in the cases where the grid impedance is varied, which is the case that IC-PLL needs for adapting the value of the virtual impedance so that the VSC converter maintains the synchronization with the infinite
Adaptive IC-PLL (AIC-PLL) Based System

bus voltage.
In the literature, the approaches that are used to estimate the value of the grid impedance are based on the deliberate creation of a disturbance at the PCC, and the value of impedance is calculated based on the grid response to this distortion. These disturbances can be based on power variation in both active and reactive power at the PCC [71], current spike at PCC [72]. However, the accuracy of the estimation depends on the size of the disturbances, which may become challenging in the case of a weak grid system. In addition, these approaches require for additional signal processing method to deal with the influence of the nonlinear loads connected close to PCC. Therefore, the proposed AIC-PLL has the ability to estimate the value of the grid impedance so that the VSC converter maintains the synchronisation with the infinite bus voltage, without any requirements for the sophisticated methods of the impedance value estimation. Furthermore, this method does not require any source of disturbance, which is essential in the other methods, for the estimation of the accurate value of the grid impedance. Therefore, the VSC converter utilities the AIC-PLL provides the maximum achievable theoretical power in the case of the grid variation with satisfactory dynamic performance.

6.1 Adaptive Impedance-Conditioned PLL (AIC-PLL) configuration

The exiting IC-PLL is modified so that another closed loop is included in order to adapt the value of the virtual resistance and inductance of the virtual impedance part. As it is shown in Figure 6.1 the value of $\theta_{PLL}$ is fed into two compensators $H_L(s)$ and $H_R(s)$, in order to generate the virtual inductance and resistance values $\hat{L}_v$ and $\hat{R}_v$, respectively. To understand how the AIC-PLL functions in terms of the phase angles
of the voltages, the block diagram in Figure 6.1 is simplified to be represented as in Figure 6.2.

![Fig. 6.1 Schematic diagram of the AIC-PLL system.](image)

![Fig. 6.2 Simplified model of the AIC-PLL.](image)
In Figure 6.2 two feedback closed loops simplify the AIC-PLL in Figure 6.1 where;

- The inner loop represents the linearised version of the conventional SRF-PLL, in which the transfer function $H_{PLL}(s) \simeq H_{FL,PLL}(s) \cdot H_C(s)$, where $H_{FL,PLL}(s)$ and $H_C(s)$ are the transfer functions of the PLL low pass filter and PLL compensator, respectively, providing that the angle $\arctan\left(\frac{v^u}{v_{id}}\right) \simeq 0$.

- The outer loop depicts the virtual impedance part, where $\hat{L}_v = \theta_{PLL} \cdot H_L(s)$ and $\hat{R}_v = \theta_{PLL} \cdot H_R(s)$.

- The value of $\theta_{uv}$ is the phase angle of the virtual voltage, which is the voltage across the virtual impedance.

Initially, it is assumed that the value of the voltage amplitude of $E$ is known, and $\theta_E = 0^\circ$. In the outer loop, the value of the $\theta_{uv} \rightarrow \theta_u$ through manipulating the values of $\hat{L}_v$ and $\hat{R}_v$, where $\hat{L}_v \rightarrow L_g$, $\hat{R}_v \rightarrow R_g$. The angle $(\theta_u - \theta_{uv})$ is the phase angle of the voltage at the point of synchronisation, which is $(\theta_u - \theta_{uv} = 0)$ when the converter is synchronised to the infinite bus voltage. By the inner loop, which represents the traditional SRF-PLL, the estimated angle value $\theta_{PLL}$ converges to the point of synchronisation angle, where $\theta_{PLL} \rightarrow (\theta_u - \theta_{uv})$. As a result of this and in the steady-state, the VSC converter is synchronised to the infinite bus voltage, where $\theta_{uv} = \theta_a$ and $\theta_{PLL} = 0$. In order to demonstrate how the voltages and currents are manipulated in the AIC-PLL, the vector diagram is plotted in Figure 6.3,
In Figure 6.3, the voltage magnitude $U^v$ is the magnitude of the voltage across the virtual impedance $u^v$ with its phase angle $\theta_{uv}$, and this angle is measured with respect to the voltage $u$ at PCC. The voltage $u^v$ is aligned with the voltage $u$ when the value of the virtual impedance is equal to zero ($\hat{R}_v = 0$, $\hat{L}_v = 0$). In this case, the value of the angle $\theta_{uv} = 0$, i.e., the converter is synchronised to the voltage at PCC. Hence, the value of $\theta_{PLL} = \theta_u$ which is fed into compensators $H_L(s)$ and $H_R(s)$ to generate $\hat{L}_v$ and $\hat{R}_v$, respectively. As these values increase the voltage $u_v$ shifts away from voltage $u$ towards voltage $E$ (as shown in Figure 6.3), and as result of this $\theta_{uv} \rightarrow \theta_u$ and $\theta_{PLL} \rightarrow 0$.

The modelling of the VSC-HVDC system utilises AIC-PLL is the same as that one utilises IC-PLL with considering the following model of the AIC-PLL
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\[ u_d^v = c u_d - c_{igd} \hat{R}_v + \omega_{PLL} \hat{L}_v c_{igd}, \]  
\[ u_q^v = c u_q - c_{igq} \hat{R}_v - \omega_{PLL} \hat{L}_v c_{igd}, \]  
(6.1)

where

\[ \hat{L}_v = \pm (H_L(s) \cdot \theta_{PLL} s), \]
\[ \hat{R}_v = \pm (H_R(s) \cdot \theta_{PLL} s). \]
\[ H_L(s) = \frac{K_{Lvi}}{s} + K_{Lvp}, \quad H_R(s) = \frac{K_{Rvi}}{s} + K_{Rvp}. \]

Where the sign (+) is for the inverter operation and (-) is for the rectifier operation.

The reason for that is the voltage \( u \) at the PCC leads the voltage \( E \) at the infinite bus in the case of the inverter operation, i.e. the phase angle \( \theta_{PLL} \) is positive. Whilst in the case of the rectifier operation, the voltage \( u \) lags the voltage \( E \), which results in the phase angle \( \theta_{PLL} \) to be negative.

By trial and error, the parameters of \( H_L(s) \) and \( H_R(s) \) are chosen to be \( K_{Lvi} = 10, \)
\( K_{Rvi} = 500, \) \( K_{Lvp} = 100 \) and \( K_{Rvp} = 100. \) In order to investigate the validity of these values, the sums of squares of errors for the time-domain responses of the active power are calculated for different selected values of the gains, and the results of this experiment are plotted in Figure 6.4
6.2 Stability limits of AIC-PLL based VSC converter

In Figure 6.4 different values of the gains are selected, 0.1, 1 and 10 times of the nominal value of the virtual impedance compensator gains. It is clear from the result that the highest value of SSE is when the gains is smaller than the nominal value by 90% and the values of the SSE are approximately equal in the case of the 1 and 10 times of the nominal value. This indicates that as the values of the gains increase, there will not have an effect on the dynamic performance of the system. This is due to the fact that the small improvement in the dynamic response of the phase angle $\theta_{PLL}$ is within an inconsiderable range that will have no impact on the overall system.

6.2 Stability limits of AIC-PLL based VSC converter

In this section, the stability limit is defined in terms of the maximum power that the AIC-PLL based VSC converter can transfer in a steady-state while maintaining the
stability of the system, which is determined by conducted the small signal stability analysis as it is explained in Chapter 5. The results are shown in Figure 6.5.

![Fig. 6.5 Steady-state power transfer stability limits of VSC-HVDC system](image)

Figure 6.5 shows the maximum transferred power in per unit for two VSC converters utilise two types of PLLs, IC-PLL with $Z_v^g = Z_g$ and AIC-PLL, for a range of values of grid impedance $Z_g$ and for the inverter and rectifier operations. It can be observed that the values of the maximum active power at which the system maintains stable for both types of the IC-PLL and AIC-PLL based converters are equal, and they are approximately equal to the theoretical maximum power. Therefore, the converter that utilises AIC-PLL is capable of reaching the maximum theoretical power transfer in the same way that the IC-PLL does, in spite of the fact that the AIC-PLL does not require any information about the value of the grid impedance. Moreover, It can be concluded from this result that the AIC-PLL is able to imitate the IC-PLL with $Z_v^g = Z_g$ in terms of the power transfer capability, as the converter that utilises AIC-PLL is also synchronised to the infinite bus voltage $E$. Therefore, the AIC-PLL possibly replaces the IC-PLL in the case that the maximum power transfer is demanded,
6.3 Dynamic performance study for AIC-PLL based VSC converter

and the estimation of the value of the grid impedance is challenging, in particular, the
grid strength changes, as it will be shown in this chapter.

6.3 Dynamic performance study for AIC-PLL based VSC converter

In this section, the dynamic performance of the AIC-PLL based converter is investigated
for different points in the grid strength. The performance of the AIC-PLL based system
is studied by examining the dynamic response of the system to the changing in the
value of the grid impedance and the value of the active power. For each point of the
grid impedance, an experiment is conducted, and two step changes are applied. The
first step is on the grid impedance, and this is to simulate the variation that may occur
in the grid impedance value in the real system, and how the AIC-PLL has the ability
to recover the changing in this value. The second step change is for the active power,
and this is to examine the effectiveness of the AIC-PLL based converter in terms of
dealing with variation in active power. In order to demonstrate the effectiveness of
the proposed method, the response of the AIC-PLL based converter’s active power
is compared with the two cases of the IC-PLL based converters. The first one is the
IC-PLL with a constant value of the virtual impedance, i.e. the value of $Z_g^v$ does not
change according to the changing in the grid impedance. The second case is when the
value of the $Z_g^v$ is changing according to the changing in the grid impedance, hence the
relation $Z_g^v = Z_g$ is maintained during the system’s operation.

The first experiment is when the value of the grid impedance changes from $Z_g = 1 \rightarrow 1.1$
p.u. in the inverter operation, then another step change in active power is applied
which is $P = 0.9 \rightarrow 1$ p.u. Figures 6.6, 6.7 and 6.8 show the responses of active power
and $\theta_{PLL}$, respectively.
Adaptive IC-PLL (AIC-PLL) Based System

Fig. 6.6 Time-domain response of the active power for different types of PLLs for step change in $Z_g = 1 \rightarrow 1.1$ p.u. and for $\omega_{PLL} = 400$ rad/sec (inverter operation)

Figure 6.6 shows the result of the time-domain response of the active power for different converters utilise different types of PLLs. It is clear from the figure the converter that utilises the IC-PLL with $Z_v^v = Z_g$ has the optimal response as it shows less oscillation than the other two approaches with less settling time. However, for the system that relays on the IC-PLL without updating the value of the virtual impedance, the result shows that the time-domain response exhibits the highest oscillatory response. In the case that the system uses the proposed method AIC-PLL, the result shows that the time-domain response of the active power suffers far less oscillation than the IC-PLL with $Z^v_g = 1$ p.u., and it has slightly more oscillation amplitude than the case of IC-PLL with $Z^v_g = Z_g$. Therefore, from this result, it can be concluded that the proposed AIC-PLL has the ability to recover the changing that occurs in the grid impedance in the case of the strong system.

Figure 6.7 shows the time-domain response of the active power for the applied step change in the active power for the VSC converters with different types of PLLs for the same above experiment at a different time where the value of the grid impedance $Z_g = 1.1$ p.u.,
6.3 Dynamic performance study for AIC-PLL based VSC converter

It can be seen from Figure 6.7 that the dynamic response for the case of IC-PLL with \( Z_g^v = 1 \) exhibits higher overshoot than the other two cases. However, for the case of the converter that utilises AIC-PLL the results in Figure 6.7 show that the response exhibits relatively higher oscillation amplitude than the other two cases. It can be concluded from the results in Figures 6.6 and 6.7 that the proposed AIC-PLL has the ability to deliver the maximum power with satisfactory dynamic performance. Figure 6.8 is the time domain response for the phase angle of the different types of PLL in the case of the step changing in the value of the grid impedance,
Adaptive IC-PLL (AIC-PLL) Based System

Fig. 6.8 Time-domain response of the $\theta_{PLL}$ for different types of PLLs for step change in $Z_g = 1 \rightarrow 1.1$ p.u. and for $\omega_{FL,PLL} = 400$ rad/sec (inverter operation)

Figure 6.8 shows the response of the phase angle $\theta_{PLL}$ that is generated by different types of PLLs. In this figure two y-axes for the phase angle $\theta_{PLL}$ are included, the left y-axis is for the IC-PLL ($Z^u_g = 1$ p.u.), as it generates a larger phase angle scale than the other two cases. For the other two cases of the PLLs, the right y-axis is devoted. It is clear from the figure that the time domain response that is generated by IC-PLL ($Z^u_g = 1$ p.u.) exhibits higher oscillatory with higher settling time than the other two cases. In addition, the value of $\theta_{PLL}$ in the case of IC-PLL ($Z^u_g = 1$ p.u.) does not converge to zero. However, the result shows that the response of the $\theta_{PLL}$ for the IC-PLL with ($Z^u_g = Z_g$) has more oscillatory than the case of AIC-PLL. This is because in the second case another closed loop is involved in the AIC-PLL (Figure 6.1) where the $\theta_{PLL}$ is considered as the control signal in this loop, and this is not the case for IC-PLL.

The experiment is re-conducted for the different step change where the value of the grid impedance change is $Z_g = 1.7 \rightarrow 2$ p.u., and the results are provided in Figures 6.9, 6.10 and Figure 6.11,
6.3 Dynamic performance study for AIC-PLL based VSC converter

Fig. 6.9 Time-domain response of the active power for different types of PLLs for step change in $Z_g = 1.7 \rightarrow 2$ p.u. and for $\omega_{FL,PLL} = 400$ rad/sec (inverter operation)

Fig. 6.10 Time-domain response of the active power for different types of PLLs for step change in active power and for $\omega_{FL,PLL} = 400$ rad/sec, $Z_g = 2$ p.u. (inverter operation)

Figures 6.9 and 6.10 show the response of the active power for the step change in the grid impedance ($Z_g = 1.7 \rightarrow 2$ p.u.), and the step change in the value of the active power, respectively. It can be observed that the responses of the active power for the cases of IC-PLL with ($Z_g^v = Z_g$) and the AIC-PLL have far better responses
than the case of IC-PLL with \( Z_g^v = 1.7 \) p.u., as the first two cases provide lower oscillatory and settling time than the second case. Figures 6.9 and 6.10 also show that the response of the active power in the case of AIC-PLL is slightly better than the case of IC-PLL with \( Z_g^v = Z_g \), as the former case provides less oscillatory and settling time than the latter case. Therefore, it can be concluded that in the case of the very weak grid the converter that utilises AIC-PLL has the ability to replace the ideal IC-PLL in the case of the grid variation where the estimation of the grid is very complicated.

Figure 6.11 is the time domain response for the produced angle of the three types of PLL,

![Time-domain response of the \( \theta_{PLL} \) for different types of PLLs for step change in \( Z_g = 1.7 \to 2 \) p.u. and for \( \omega_{FL,PLL} = 400 \) rad/sec (inverter operation).](image)

From the result in Figure 6.11, it can be concluded that the response of the phase angles for different types of PLLs have the same indication as for the result in Figure 6.8. In addition, By comparing two Figures 6.8 and 6.11 it is clear that the dynamic response of the angle in the case of IC-PLL with \( Z_g^v = Z_g \) has a higher oscillatory amplitude in the case of the second experiment than the first experiment. It reaches 2 degrees for the second experiment while it reaches about 0.5 degree in the first case,
6.3 Dynamic performance study for AIC-PLL based VSC converter

which is due to the larger value of the grid impedance in the second case. The dynamic response of the angle $\theta_{PLL}$ has an impact on the dynamic response of the active power, and the larger the value of the angle, the higher impact on the response of the active power. As a result of this, the response of the active power in the case of the AIC-PLL is relatively better than the case of the IC-PLL ($Z^v = Z_g$) for the larger value of the grid impedance, which is evident in Figures 6.9 and 6.10.

For further validation and reliability of the proposed AIC-PLL, experiments of different values of operating points and different values of the changing in the value of the grid impedance are conducted and the values of the SSE are calculated. Two different operating points are chosen, 50% and 100% of the maximum transferred power of different values of the grid impedance. A step change in the active power is applied which is 1% of the selected operating point. Other experiments are also conducted, where the value of the active power is the maximum and the step change in the grid impedance is applied. Different step change percentages are applied and they depend on the value of the grid impedance, the larger the value of the grid impedance the smaller the value of the step change. The results of this experiment are presented in Figures 6.12, 6.14 and 6.16 for the inverter operation, and Figures 6.13, 6.15, and 6.17 for the rectifier operation.
Fig. 6.12 SSE for the active power tracking for the IC-PLL and AIC-PLL based system for half value of the maximum power (inverter operation).

Fig. 6.13 SSE for the active power tracking for the IC-PLL and AIC-PLL based system for half value of the maximum power (rectifier operation).
6.3 Dynamic performance study for AIC-PLL based VSC converter

Fig. 6.14 SSE for the active power tracking for the IC-PLL and AIC-PLL based system for the maximum power (inverter operation).

Fig. 6.15 SSE for the active power tracking for the IC-PLL and AIC-PLL based system for the maximum power (rectifier operation).

In Figures 6.12, 6.13, 6.14 and 6.15 the value the operating points are 50% and 100% of the maximum transferred power, for the inverter and rectifier operation, respectively, and for a range of the value of the grid impedance. In these figures, bar charts represent the values of the SSE. A line graph represents the relative errors between the value of
SSE of IC-PLL and SSE of AIC-PLL. It is clear from the results that both methods are approximate equals in terms of the dynamic responses, which indicates by the inconsiderable value of the relative error. In the case of the inverter operation, it can be concluded from the results in Figures 6.12 and 6.14 that the dynamic response of the IC-PLL base converter is better than the AIC-PLL based one for the strong grid. This difference in the dynamic response is reduced as the value of the grid impedance increases to become positive for the value of the $Z_g \geq 1.8$ p.u. However, in the case of the rectifier operation, the results in Figure 6.13 and 6.15 show that the converter that relies on the AIC-PLL provides better dynamic response than the case of the IC-PLL based converter for the whole range of the grid impedance. This is indicated by the value of the relative error, which is positive. In addition, the value of SSE for both types of PLLs is higher in the case of the higher value of the operating points, which indicates the impact of the increasing the value of the operating points on the dynamic performance of the system.

Figures 6.16 and 6.17 represent the results of the value of SSE for both types of PLLs based converters when the value of the grid impedance is changing for the inverter and rectifier operations, respectively. The values of these changes are $\Delta Z_g = [0.5 \ 0.5 \ 0.3 \ 0.3 \ 0.3 \ 0.25 \ 0.25 \ 0.2 \ 0.2] \cdot Z_g$, where $Z_g = [0.2 \ 0.4 \ 0.6 \ 0.8 \ 1 \ 1.2 \ 1.4 \ 1.6 \ 1.8 \ 2]$ p.u. The value of the relative errors are also presented as a graph line in order to show the difference between the SSE values of the IC-PLL and AIC-PLL for the range of the grid impedance.
6.3 Dynamic performance study for AIC-PLL based VSC converter

Fig. 6.16 SSE for the active power tracking for the IC-PLL and AIC-PLL based system for different change in the values of the grid impedance (inverter operation).

In the case of the inverter operation, Figure 6.16 shows that the values of SSE for IC-PLL based converter is less than the value of SSE for the case of the AIC-PLL based converter for $Z_g \leq 1.6$ p.u., which is indicated by the value of the error. The results also show that the error is positive for $Z_g \geq 1.8$ p.u., which indicates that the

Fig. 6.17 SSE for the active power tracking for the IC-PLL and AIC-PLL based system for different change in the values of the grid impedance (rectifier operation).
proposed method has the ability to provide better dynamic performance as the value of the grid impedance increases. In the case of the rectifier operation, Figure 6.17 shows that the converter that utilises AIC-PLL has the ability to provide better dynamic performance than the case of the system that uses IC-PLL for the whole range of the grid impedance. This is clear from the relative error line graph, which is positive for the whole range of the grid impedance value.

6.3.1 The impact of changing the value of PLL bandwidth on the AIC-PLL dynamic performance

In this section, the effect of changing the value of the PLL bandwidth $\omega_{FL,PLL}$, which is related to the PLL compensator bandwidth, on the dynamic performance of the converter is considered. The compensator bandwidth is 55% of the bandwidth of the PLL low pass filter. Therefore, when the value of the $\omega_{FL,PLL}$ changes, the controller parameters change accordingly. In order to understand how the impact of changing the value of the $\omega_{FL,PLL}$ on the dynamic performance of the system, the root locus of the closed-loop system’s poles in the s-domain is examined by sweeping the $\omega_{FL,PLL} = 50 \rightarrow 2000$ rad/sec, and the results are plotted in Figure 6.18. This is to discover which eigenvalues are affected by changing the value of the $\omega_{FL,PLL}$, and by calculating the participation matrix, the states that have the highest participation factors to the plotted eigenvalues are revealed.
6.3 Dynamic performance study for AIC-PLL based VSC converter

In Figure 6.18, the only eigenvalues $\lambda_{1,20,6}$ are included, since they have the highest rates of change in their positions than other eigenvalues. From the participation matrix (the participation matrix are provided in Appendix C), these eigenvalues have the highest participation factors to the states that are related to the PLL. These states are the phase angle $\theta_{PLL}$, the augmented state of the PLL’s PI controller $\gamma_{PLL}$ and the virtual voltage $u_{dv}$. It is clear from the result that all the positions of the eigenvalues are shifted towards left as the value of the PLL bandwidth increases. This indicates that for the case of the AIC-PLL the value of the PLL bandwidth does not have an impact on the stability and the dynamic performance of the system. This is because the value of the states is minimal, which is due to the included estimation closed-loop. Therefore, this will not have an obvious impact on the dynamic performance of the active power. In order to understand this effect, the time-domain responses of the active power and the phase angle $\theta_{PLL}$ for different values of $\omega_{FL,PLL}$ are plotted in Figures 6.19, 6.20,
Adaptive IC-PLL (AIC-PLL) Based System

Fig. 6.19 Time domain response of the active power for AIC-PLL for step change in $Z_g = 1.7 \rightarrow 2$ p.u. and for different values of the $\omega_{FL,PLL}$

Fig. 6.20 Time domain response of the $\theta_{PLL}$ for AIC-PLL for step change in $Z_g = 1.7 \rightarrow 2$ p.u. and for different values of the $\omega_{FL,PLL}$

It is clear from Figures 6.19 that the dynamic response of the active power for the converter that utilises AIC-PLL with different values of $\omega_{FL,PLL}$ are approximately identical, which indicates the fact that the changing the value of the PLL bandwidth does not have any impact on the response of the active power. Figure 6.20 shows the
time domain response of the phase angle $\theta_{PLL}$ for different value of $\omega_{FL,PLL}$, and it is clear that as the value of the bandwidth increases the system has a better response in terms of the oscillatory and the settling time. This is due to the increase in the value of the PI compensator parameters, which, in turn, increases the speed of the PI controller. In addition, the result in Figure 6.20 shows that the range of the variation is inconsiderable to have an impact on the response of the active power.

6.4 Conclusion

In this chapter, a description of the proposed AIC-PLL is provided. The steady-state power transfer capability and the dynamic performance of the AIC-PLL based converter are also considered in this chapter. The results show that the converter that relies on AIC-PLL is capable of transferring power which is approximately equal to the theoretical maximum power. In terms of the dynamic performance, the results demonstrate that the AIC-PLL based VSC converter provides a satisfactory dynamic response for different value of the grid impedance. Therefore, the AIC-PLL has the ability to replace the traditional IC-PLL in the case of the grid variation.
Chapter 7

Conclusions and Future Work

7.1 Conclusions

This thesis investigates the impact that different grid synchronisation techniques, which all employ PLL technique, have on the power transfer capability and the dynamic performance of the VSC-HVDC system interconnected to AC grid. Three types of PLLs are considered, namely, Synchronous Reference Frame PLL (SRF-PLL), Damping Factor PLL (DF-PLL) and Impedance-Conditioned PLL (IC-PLL). Extensive studies were carried out to investigate the VSC-HVDC system that utilises each of these three types of PLL in terms of its power transfer capability and dynamic performance. In order to perform these tasks, the mathematical models of the VSC-HVDC system that utilises each of the three considered types of PLL are derived. Because of the fact that there is no unified approach in the literature that can be followed to develop the mathematical model, the two approaches are used to derive the models, and then they are validated by comparing their time-domain responses against the simulation of the overall system realised using MATLAB’s SimPowerSystem toolbox. The approach that provides a validated mathematical model is used as the design procedure to develop the mathematical models for each of the different types of PLL based converters considered.
in this thesis.

The maximum power transfer capability is determined by conducting a small signal stability analysis, and the maximum value of the active power for which the system maintains stability, i.e. for which the real part of each of the eigenvalues is located in the left half side of the s-plane, is considered the stability limit of the system. It was found that the converter that utilises the IC-PLL has the ability to transfer power approximately equal to the theoretical maximum power for a certain range of virtual impedance and PLL bandwidth. However, the transferred power by the converter that utilises either SRF-PLL or DF-PLL was found to be considerably smaller than its theoretical maximum value. Furthermore, it was observed that converters that utilise either SRF-PLL or DF-PLL result in a similar value of maximum power transfer. In addition, the results demonstrate that selecting the values of PLL bandwidth, virtual impedance and damping factor, have an impact on the transferred power. This reflects the fact that PLL parameters which affect the dynamic performance of the system also have a significant impact on the maximum power transfer capability. Also, the dynamic performance of the system is considered in the thesis and the results show that for the IC-PLL based system the value of the PLL bandwidth and the virtual impedance have a considerable impact on the dynamic response of the control system to track the required active power. It is shown that for any value of the grid impedance, the optimal dynamic performance can be achieved for the case where the assumed grid impedance is equal to its actual value.

This thesis also considers a realistic scenario of changing grid impedance as a result of varying system configuration or loading conditions. In order to address this scenario the IC-PLL is modified by augmenting it with additional closed loop so that the internally generated angle is utilised to estimate the value of the virtual impedance. In order to imitate the changing that may happen in the value of the grid impedance, step changes
are applied in the value of the grid impedance during the running of the simulation, and for different value of the grid impedance. In addition, the effectiveness of the system is also examined in terms of the different operating conditions, i.e. different nominal value of the transferred power. The results reveal that the converter that utilises the proposed AIC-PLL has the ability to transfer power approximately equal to the theoretical maximum power even in the presence of grid impedance variation with satisfactory dynamic performance. Therefore, the issue of variation in SCR is no longer a limiting factor in the case of the VSC converter that utilises AIC-PLL.

### 7.2 Future work

The possible future work is listed below:

- The VSC valves losses, the PWM technique and the DC side voltage control are neglected in the modelling and studying the VSC-HVDC system in the thesis. Therefore, these could be considered in future studies.

- The locations of the zeros of the overall system could be examined. The right half-plane (RHP) zeros, or non-minimum phase, imposes some limitations, such as inverse response and high gain instability [73]. Therefore, it is important to be taken into account, in particular, the effect of proposing AIC-PLL on the locations of the zeros.

- Investigating the effectiveness of the converters that utilise different types of PLL when is subjected to various distortions, such as harmonics, frequency changes and unbalanced input conditions should be considered in future studies.

- In this thesis, the weak grid connections are characterised by the high value of the grid impedance. Another problem is determined by a low-inertia AC system,
7.2 Future work

i.e. a limited number of rotating machines in the system. This scenario should also be considered for converters that utilise various types of PLLs.
References


References


References


Appendix A

State space models of the DF-PLL and IC-PLL based converters

In this appendix, the state space model of the DF-PLL and IC-PLL are presented, where these models are obtained in the same procedure that is used in Chapter 4.

A.0.1 State space model of the converter utilises DF-PLL

The state space model of the main circuit, the inner loop controllers, the outer loop controllers and the rotation matrices are all combined in an overall linearised state-space matrix form as

\[
\Delta \dot{x} = A \cdot \Delta x + B \cdot \Delta u, \\
\Delta y = C \cdot \Delta x + D \cdot \Delta u.
\]

where
\[
\begin{align*}
\alpha_{1,1} &= \alpha_1 \cos \theta_{PLL} - \alpha_2 \sin \theta_{PLL} - \frac{B_e}{L_e}, \\
\alpha_{1,2} &= \alpha_3 \cos \theta_{PLL} - \alpha_4 \sin \theta_{PLL} + \omega, \\
\alpha_{2,1} &= \alpha_1 \sin \theta_{PLL} + \alpha_2 \cos \theta_{PLL} - \omega, \\
\alpha_{2,2} &= \alpha_3 \sin \theta_{PLL} + \alpha_4 \cos \theta_{PLL} - \frac{B_e}{L_e}, \\
\alpha_{7,9} &= \varepsilon_{i_{q0}} \sin \theta_{PLL} - \varepsilon_{i_{d0}} \cos \theta_{PLL}, \\
\alpha_{8,9} &= \varepsilon_{i_{q0}} \sin \theta_{PLL} + \varepsilon_{i_{d0}} \cos \theta_{PLL}, \\
\alpha_1 &= \omega \sin \theta_{PLL} - \frac{1}{L_c} k_{pd} \cos \theta_{PLL}, \\
\alpha_2 &= \frac{1}{L_c} (\omega L_c \cos \theta_{PLL} + k_{pd} \sin \theta_{PLL}), \\
\alpha_3 &= -\omega \cos \theta_{PLL} - \frac{1}{L_c} k_{pd} \sin \theta_{PLL}, \\
\alpha_4 &= \frac{1}{L_e} (\omega L_e \sin \theta_{PLL} - k_{pd} \cos \theta_{PLL}), \\
\alpha_5 &= k_{id} \frac{1}{L_c} \cos \theta_{PLL}, \\
\alpha_6 &= k_{iq} \frac{1}{L_e} \sin \theta_{PLL}, \\
\alpha_7 &= \frac{1}{L_c} (\cos \theta_{PLL} (\partial V_{dref}^c / \partial \theta) |_{\theta=x_0}) - (V_{dref}^c |_{\theta=x_0}) \sin \theta_{PLL} - \sin \theta_{PLL} (\partial V_{qref}^c / \partial \theta) |_{\theta=x_0}) - (V_{qref}^c |_{\theta=x_0}) \cos \theta_{PLL}, \\
\alpha_8 &= \frac{1}{L_c} (\sin \theta_{PLL} (\partial V_{dref}^c / \partial \theta) |_{\theta=x_0}) + (V_{dref}^c |_{\theta=x_0}) \cos \theta_{PLL} + \cos \theta_{PLL} (\partial V_{qref}^c / \partial \theta) |_{\theta=x_0}) - (V_{qref}^c |_{\theta=x_0}) \sin \theta_{PLL}, \\
\alpha_9 &= \sin \theta_{PLL}, \\
\alpha_{10} &= \cos \theta_{PLL}, \\
\alpha_{11} &= D(\varepsilon_{i_{d0}} \sin \theta_{PLL} - \varepsilon_{i_{q0}} \cos \theta_{PLL}), \\
\alpha_{12} &= \omega \Delta D(\varepsilon_{u_d} \sin \theta_{PLL} + \varepsilon_{u_d} \cos \theta_{PLL}), \\
\alpha_{13} &= \omega \Delta D(\varepsilon_{u_q} \sin \theta_{PLL} - \varepsilon_{u_q} \cos \theta_{PLL}),
\end{align*}
\]
State space models of the DF-PLL and IC-PLL based converters

\[ \alpha_{14} = K_{pPLL} \omega_b \frac{u_{v0}^2}{u_{d0}^2 (\frac{u_{d0}}{u_{v0}} + 1)} \]

\[ \alpha_{15} = K_{pPLL} \omega_b \frac{u_{v0}^2}{u_{d0}^2 (\frac{u_{d0}}{u_{v0}} + 1)} \]

\[ \alpha_{16} = \omega_{PLL} (-c u_{d0} \sin \theta_{PLL0} + c u_{q0} \cos \theta_{PLL0}) \]

\[ \alpha_{17} = \omega_{PLL} (-c u_{q0} \sin \theta_{PLL0} - c u_{d0} \cos \theta_{PLL0}) \]

\[ \alpha_{18} = \frac{\omega_{AD}}{K_{pPLL}} \]

\[
B = \begin{bmatrix}
\frac{1}{L_c} k_{pd} K_p \cos \theta_{PLL0} & - \frac{1}{L_c} k_{pd} K_p \sin \theta_{PLL0} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
\frac{1}{L_c} k_{pq} K_p \sin \theta_{PLL0} & - \frac{1}{L_c} k_{pq} K_p \cos \theta_{PLL0} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
\end{bmatrix}
\]

\[
C = \begin{bmatrix}
0 & 0 & i_{g0} & 0 & u_{d0} & u_{q0} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & i_{g0} & 0 & u_{d0} & u_{q0} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
\end{bmatrix}
\]

\[ D = \tilde{D}. \]

A.0.2 State space model of the converter utilises IC-PLL

The state space model of the main circuit, the inner loop controllers, the outer loop controllers and
the rotation matrices are all combined in an overall linearised state-space matrix form as:

\[ \Delta \dot{x} = A \cdot \Delta x + B \cdot \Delta u, \]

\[ \Delta y = C \cdot \Delta x + D \cdot \Delta u. \]
where

\[ \begin{align*}
\alpha_1, \alpha_2 & \quad \frac{K_{pi}}{s} \quad 0 \quad 0 \quad 0 \quad 0 \quad n_i \quad n_0 \quad n_0 \quad 0 \quad 0 \quad 0 \\
\alpha_3, \alpha_4 & \quad 0 \quad -\frac{K_{pi}}{s} \quad 0 \quad 0 \quad n_i \quad n_0 \quad n_0 \quad 0 \quad 0 \quad 0 \\
\alpha_5, \alpha_6 & \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \\
\alpha_7 & \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \\
0 & \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \\
0 & \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \\
0 & \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \\
0 & \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \\
0 & \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \\
\end{align*} \]

\[ A = \begin{pmatrix}
\omega_0 & \omega_0 & \omega_0 & \omega_0 & \omega_0 & \omega_0 & \omega_0 & \omega_0 & \omega_0 & \omega_0 \\
\omega_0 & \omega_0 & \omega_0 & \omega_0 & \omega_0 & \omega_0 & \omega_0 & \omega_0 & \omega_0 & \omega_0 \\
\omega_0 & \omega_0 & \omega_0 & \omega_0 & \omega_0 & \omega_0 & \omega_0 & \omega_0 & \omega_0 & \omega_0 \\
\omega_0 & \omega_0 & \omega_0 & \omega_0 & \omega_0 & \omega_0 & \omega_0 & \omega_0 & \omega_0 & \omega_0 \\
\omega_0 & \omega_0 & \omega_0 & \omega_0 & \omega_0 & \omega_0 & \omega_0 & \omega_0 & \omega_0 & \omega_0 \\
\omega_0 & \omega_0 & \omega_0 & \omega_0 & \omega_0 & \omega_0 & \omega_0 & \omega_0 & \omega_0 & \omega_0 \\
\omega_0 & \omega_0 & \omega_0 & \omega_0 & \omega_0 & \omega_0 & \omega_0 & \omega_0 & \omega_0 & \omega_0 \\
\omega_0 & \omega_0 & \omega_0 & \omega_0 & \omega_0 & \omega_0 & \omega_0 & \omega_0 & \omega_0 & \omega_0 \\
\omega_0 & \omega_0 & \omega_0 & \omega_0 & \omega_0 & \omega_0 & \omega_0 & \omega_0 & \omega_0 & \omega_0 \\
\omega_0 & \omega_0 & \omega_0 & \omega_0 & \omega_0 & \omega_0 & \omega_0 & \omega_0 & \omega_0 & \omega_0 \\
\end{pmatrix} \]

and

\[ a_{11} = a_1 \cos \theta_{PLL0} - a_2 \sin \theta_{PLL0} - \frac{R_0}{L_c}, \]
\[ a_{12} = a_3 \cos \theta_{PLL0} - a_4 \sin \theta_{PLL0} + \omega, \]
\[ a_{21} = a_3 \sin \theta_{PLL0} + a_2 \cos \theta_{PLL0} - \omega, \]
\[ a_{22} = a_3 \sin \theta_{PLL0} + a_4 \cos \theta_{PLL0} - \frac{R_0}{L_c}, \]
\[ a_{77} = -i_{d0} \sin \theta_{PLL0} - i_{q0}^c \cos \theta_{PLL0}, \]
\[ a_{87} = -i_{q0} \sin \theta_{PLL0} + i_{d0} \cos \theta_{PLL0}, \]
\[ a_{1} = \omega \sin \theta_{PLL0} - \frac{1}{L_c} k_{pd} \cos \theta_{PLL0}, \]
\[ a_{2} = \frac{1}{L_c} (\omega L_c \sin \theta_{PLL0} + k_{pq} \sin \theta_{PLL0}), \]
\[ a_{3} = -\omega \cos \theta_{PLL0} - \frac{1}{L_c} k_{pd} \sin \theta_{PLL0}, \]
\[ a_{4} = \frac{1}{L_c} (\omega L_c \sin \theta_{PLL0} - k_{pq} \cos \theta_{PLL0}), \]
\[ a_{5} = k_{pd} \cos \theta_{PLL0}, \]
\[ a_{6} = k_{pq} \frac{1}{L_c} \sin \theta_{PLL0}, \]
\[ a_{7} = \frac{1}{L_c} \left( (\cos \theta_{PLL0} (V_{c,dref} / \partial \theta) \mid x=x_0) - (V_{c,dref} / \partial \theta) \mid x=x_0 \right) \sin \theta_{PLL0} - \sin \theta_{PLL0} (V_{c,qref} / \partial \theta) \mid x=x_0 - (V_{c,qref} / \partial \theta) \mid x=x_0 \right) \sin \theta_{PLL0}, \]
\[ a_{8} = \frac{1}{L_c} \left( (\sin \theta_{PLL0} (V_{c,dref} / \partial \theta) \mid x=x_0) + (V_{c,dref} / \partial \theta) \mid x=x_0 \right) \cos \theta_{PLL0} + \cos \theta_{PLL0} (V_{c,qref} / \partial \theta) \mid x=x_0 - (V_{c,qref} / \partial \theta) \mid x=x_0 \right) \sin \theta_{PLL0}, \]
\[ a_{9} = \sin \theta_{PLL0}, \]
\[ a_{10} = \cos \theta_{PLL0}, \]
\[ a_{12} = \omega \AD (\omega u_0 \sin \theta_{PLL0} + \omega u_0 \cos \theta_{PLL0}), \]
\[ a_{13} = \omega \AD (\omega u_0 \sin \theta_{PLL0} + \omega u_0 \cos \theta_{PLL0}), \]
\[ a_{14} = K_p \PLL \omega \omega_0, \]
\[ a_{15} = K_p \PLL \omega \omega_0, \]
\[ a_{16} = \omega \PLL L_d (u_0 - R_{gq} q_{q0} - \omega \PLL L_d \omega_{pq}), \]
\[ a_{17} = \omega \PLL L_d (u_0 - R_{q0} q_{q0} - \omega \PLL L_d \omega_{pq}), \]
\[ a_{18} = \omega \PLL L_d (R_{q0} \cos \theta_{PLL0} - \omega \PLL L_d \omega_{pq} \sin \theta_{PLL0}). \]
State space models of the DF-PLL and IC-PLL based converters

\[ \alpha_{19} = \omega_{PLL}(-R_y \sin \theta_{PLL} + \omega_{PLL} L_y \cos \theta_{PLL}) \]

\[ B = \begin{bmatrix} \frac{1}{L_c} k_{pd} K_p \cos \theta_{PLL} & \frac{1}{L_c} k_{pd} K_p \sin \theta_{PLL} & 0 & 0 & 0 & 0 & 0 & K_p & 0 & DK_p & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ \frac{1}{L_c} k_{pq} K_u \sin \theta_{PLL} & -\frac{1}{L_c} k_{pq} K_u \cos \theta_{PLL} & 0 & 0 & 0 & -K_u & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & \end{bmatrix}^T \]

\[ C = \begin{bmatrix} 0 & 0 & i_{gq} & i_{dq} & u_{d0} & u_{q0} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}, \]

\[ D = \tilde{D}. \]
Appendix B

Figures of the mathematical models’ validations of the VSC-HVDC converters utilise three types of PLLs

This appendix presents the results that are related to the validation of the mathematical models that are derived in Chapter 4.
Figures of the mathematical models’ validations of the VSC-HVDC converters utilise three types of PLLs

B.0.1 Figures of the validation of the nonlinear mathematical model of the SRF-PLL

Fig. B.1 Comparison of $\mathcal{C}i_{cd}$ for the two mathematical models with MATLAB’s SimPowerSystem toolbox model for the SRF-PLL based converter

Fig. B.2 Comparison of $\mathcal{C}i_{cq}$ for the two mathematical models with MATLAB’s SimPowerSystem toolbox model for the SRF-PLL based converter
Fig. B.3 Comparison of $i_{gd}$ for the two mathematical models with MATLAB’s SimPowerSystem toolbox model for the SRF-PLL based converter.

Fig. B.4 Comparison of $i_{gq}$ for the two mathematical models with MATLAB’s SimPowerSystem toolbox model for the SRF-PLL based converter.

### B.0.2 Figures of the validation of the linearised mathematical model of the SRF-PLL

Figures B.5-B.10 show comparisons in the time domain responses between the nonlinear mathematical model and the small signal model of the SRF-PLL based system that were developed in Chapter 4.
Figures of the mathematical models’ validations of the VSC-HVDC converters utilise three types of PLLs

Fig. B.5 Comparison of $e_{i_{cd}}$ for linear and nonlinear mathematical models for the SRF-PLL based converter

Fig. B.6 Comparison of $e_{i_{cq}}$ for linear and nonlinear mathematical models for the SRF-PLL based converter

Fig. B.7 Comparison of $e_{i_{gd}}$ for linear and nonlinear mathematical models for the SRF-PLL based converter
Fig. B.8 Comparison of $i_q$ for linear and nonlinear mathematical models for the SRF-PLL based converter

Fig. B.9 Comparison of $P$ for linear and nonlinear mathematical models for the SRF-PLL based converter

Fig. B.10 Comparison of $Q$ for linear and nonlinear mathematical models for the SRF-PLL based converter
Figures of the mathematical models’ validations of the VSC-HVDC converters utilise three types of PLLs

B.0.3 Figures of the validation of the nonlinear mathematical model of the IC-PLL

Figures B.11-B.22 show comparisons in the time domain responses between the nonlinear mathematical model of the IC-PLL based system and the MATLAB’s SimPowerSystem toolbox model, and for $Z_g = Z_v$, where $Z_g = 0.8$ p.u.

![Figure B.11](image1.png)

Fig. B.11 Comparison of $c_i_{cd}$ for nonlinear mathematical model and MATLAB’s SimPowerSystem toolbox model for IC-PLL, the step change $c_i^*_{cd} = 0.5$ p.u.

![Figure B.12](image2.png)

Fig. B.12 Comparison of $c_i_{cq}$ for nonlinear mathematical model and MATLAB’s SimPowerSystem toolbox model for IC-PLL, the step change $c_i^*_{cd} = 0.5$ p.u.
Fig. B.13 Comparison of $u_d$ for nonlinear mathematical model and MATLAB’s SimPowerSystem toolbox model for IC-PLL, the step change $i_{cd}^* = 0.5$ p.u.

Fig. B.14 Comparison of $u_q$ for nonlinear mathematical model and MATLAB’s SimPowerSystem toolbox model for IC-PLL, the step change $i_{cd}^* = 0.5$ p.u.

Fig. B.15 Comparison of $i_{gd}$ for nonlinear mathematical model and MATLAB’s SimPowerSystem toolbox model for IC-PLL, the step change $i_{cd}^* = 0.5$ p.u.
Figures of the mathematical models’ validations of the VSC-HVDC converters utilise three types of PLLs.

Fig. B.16 Comparison of $c_i_{gq}$ for nonlinear mathematical model and MATLAB’s SimPowerSystem toolbox model for IC-PLL, the step change $c_i_{cd}^* = 0.5$ p.u.

Fig. B.17 Comparison of $c_i_{cd}$ for nonlinear mathematical model and MATLAB’s SimPowerSystem toolbox model for IC-PLL, the step change $c_i_{cq}^* = -0.5$ p.u.

Fig. B.18 Comparison of $c_i_{cq}$ for nonlinear mathematical model and MATLAB’s SimPowerSystem toolbox model, the step change $c_i_{cq}^* = -0.5$ p.u.
Fig. B.19 Comparison of $\hat{u}_d$ for nonlinear mathematical model and MATLAB’s SimPowerSystem toolbox model for IC-PLL, the step change $\hat{i}_{cq}^* = -0.5$ p.u.

Fig. B.20 Comparison of $\hat{u}_q$ for nonlinear mathematical model and MATLAB’s SimPowerSystem toolbox model for IC-PLL, the step change $\hat{i}_{cq}^* = -0.5$ p.u.

Fig. B.21 Comparison of $\hat{i}_{gd}$ for nonlinear mathematical model and MATLAB’s SimPowerSystem toolbox model for IC-PLL, the step change $\hat{i}_{cq}^* = -0.5$ p.u.
Figures of the mathematical models’ validations of the VSC-HVDC converters utilise three types of PLLs

Fig. B.22 Comparison of \(c_{iq}^*\) for nonlinear mathematical model and MATLAB’s SimPowerSystem toolbox model for IC-PLL, the step change \(c_{iq}^* = -0.5\) p.u.

B.0.4 Figures of the validation of the linearized mathematical model of the IC-PLL

Figures B.23-B.28 show comparisons in the time domain responses between the nonlinear mathematical models and the small signal model of the IC-PLL based system that were derived in Chapter 4,

Fig. B.23 Comparison of \(c_{id}^*\) for IC-PLL based system, the step change \(\Delta P^* = 0.2\) p.u., \(Z_{v}^* = 0.1Z_g\)
Fig. B.24 Comparison of $e_{iq}$ for IC-PLL based system, the step change $\Delta P^* = 0.2$ p.u., $Z_g = 0.1Z_g$ and $Z_g = 0.8$ p.u.

Fig. B.25 Comparison of $e_{ud}$ for IC-PLL based system, the step change $\Delta P^* = 0.2$ p.u., $Z_g = 0.1Z_g$ and $Z_g = 0.8$ p.u.

Fig. B.26 Comparison of $e_{uq}$ for IC-PLL based system, the step change $\Delta P^* = 0.2$ p.u., $Z_g = 0.1Z_g$ and $Z_g = 0.8$ p.u.
Figures of the mathematical models’ validations of the VSC-HVDC converters utilise three types of PLLs.

Fig. B.27 Comparison of $e_{i_{gd}}$ for IC-PLL based system, the step change $\Delta P^* = 0.2$ p.u., $Z^v_g = 0.1 Z_g$ and $Z_g = 0.8$ p.u.

Fig. B.28 Comparison of $e_{i_{gq}}$ for IC-PLL based system, the step change $\Delta P^* = 0.2$ p.u., $Z^v_g = 0.1 Z_g$ and $Z_g = 0.8$ p.u.

**B.0.5 Figures of the validation of the nonlinear mathematical model of the DF-PLL**

Figures B.29-B.33 show comparisons in the time domain responses between the nonlinear mathematical model of the DF-PLL based system that were developed Chapter 4 and the MATLAB's SimPowerSystem toolbox model.
Fig. B.29 Comparison of $c_{i_{cd}}$ for DF-PLL, the step change $\Delta c_{i_{cd}} = 0.3$ p.u., $D=10$.

Fig. B.30 Comparison of $c_{i_{cq}}$ for DF-PLL, the step change $\Delta c_{i_{cd}} = 0.3$ p.u., $D=10$.

Fig. B.31 Comparison of $c_{i_{gd}}$ for DF-PLL, the step change $\Delta c_{i_{cd}} = 0.3$ p.u., $D=10$. 

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Figures of the mathematical models’ validations of the VSC-HVDC converters utilise three types of PLLs.

Fig. B.32 Comparison of $c_{ig}$ for DF-PLL, the step change $\Delta c_{id}^* = 0.3$ p.u., $D=10$.

Fig. B.33 Comparison of $\theta_{PLL}$ for DF-PLL, the step change $\Delta c_{id}^* = 0.3$ p.u., $D=10$.

**B.0.6 Figures of the validation of the linearised mathematical model of the DF-PLL**

Figures B.34-B.41 show comparisons in the time domain responses between the nonlinear mathematical model and the small signal model of the DF-PLL based system that were derived in Chapter 4.
Fig. B.34 Comparison of $e_{icd}$ for DF-PLL, the step change $\Delta P^* = 0.2$ p.u., $D= 10$.

Fig. B.35 Comparison of $e_{icq}$ for DF-PLL, the step change $\Delta P^* = 0.2$ p.u., $D= 10$.

Fig. B.36 Comparison of $e_{ud}$ for DF-PLL, the step change $\Delta P^* = 0.2$ p.u., $D= 10$. 

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Figures of the mathematical models’ validations of the VSC-HVDC converters utilise three types of PLLs.

Fig. B.37 Comparison of $e_{u_q}$ for DF-PLL, the step change $\Delta P^* = 0.2$ p.u., $D = 10$.

Fig. B.38 Comparison of $e_{i_{q_d}}$ for DF-PLL, the step change $\Delta P^* = 0.2$ p.u., $D = 10$.

Fig. B.39 Comparison of $e_{i_{q_q}}$ for DF-PLL, the step change $\Delta P^* = 0.2$ p.u., $D = 10$. 
Fig. B.40 Comparison of $P$ for DF-PLL, the step change $\Delta P^* = 0.2$ p.u., $D = 10$.

Fig. B.41 Comparison of $Q$ for DF-PLL, the step change $\Delta P^* = 0.2$ p.u., $D = 10$. 
Appendix C

C.1 Tuning Parameters of the PLL controller

The parameters of the PLL have been tuned according to the symmetrical optimum (SO) that is suggested in [26], it states that the closed loop bandwidth of PLL transfer function will be 0.55 times of $\omega_{FLPLL}$, and the formulas of PLL controller gains are given as follow;

$$K_{pPLL} = \frac{1}{aT_{FLPLL}} = \frac{\omega_{FLPLL}}{a}, \quad a = 2\zeta + 1, \quad \text{where} \quad T_{FLPLL} = \frac{1}{\omega_{FLPLL}},$$

$$K_{iPLL} = \frac{K_{pPLL}}{T_{iPLL}}, \quad \text{where} \quad T_{iPLL} = a^2 \cdot T_{FLPLL}$$

where $a$ is a design parameter that can be selected in order to find a desired trade-off between damping and bandwidth of PLL, in this case $a = 3$.

C.2 Participation Factor

Participation Factor for the interaction between the eigenvalues and the states

The study of the impact of $Z_q^\nu$ and the IC-PLL bandwidth on the dynamic response of the VSC-HVDC system is carried out by demonstrating the eigenvalues migration of the A matrix of the closed loop system. The contribution of each eigenvalue on each state of the closed loop system can be demonstrated by calculating the Participation Matrix which can be given by [8]

$$P = [p_1p_2...p_n], \quad \text{(C.1)}$$
C.2 Participation Factor

with

\[
\mathbf{p}_i = \begin{bmatrix} p_{i1} \\ p_{i2} \\ \vdots \\ p_{in} \end{bmatrix} = \begin{bmatrix} \phi_{i1}\psi_{i1} \\ \phi_{i2}\psi_{i2} \\ \vdots \\ \phi_{in}\psi_{in} \end{bmatrix}
\]  \hspace{1cm} (C.2)

and

\[
\Phi = \begin{bmatrix} \phi_1 & \phi_2 & \ldots & \phi_n \end{bmatrix},
\] \hspace{1cm} (C.3)

\[
\Psi = \begin{bmatrix} \psi_1 & \psi_2 & \ldots & \psi_n \end{bmatrix}
\] \hspace{1cm} (C.4)

where \( \phi_i \in \mathbb{R}^{n \times 1} \) and \( \psi_i \in \mathbb{R}^{n \times 1} \) are the right and left eigenvector for the matrix \( A \). The element \( p_{ik} = \phi_i\psi_{ik} \) is called participation factor, it shows how the \( k \)th state variable is related to the \( i \)th eigenvalue, and vice versa. The participation matrices for the closed loop systems for IC-PLL and AIC-PLL are provided below;

## Participation matrix for the IC-PLL based system,

\( \omega_{FL,PLL} = 400 \) rad/sec, \( Z_g^v = Z_g \) and \( Z_g = 0.8 \) p.u.
## Participation matrix for the IC-PLL based system, \(\omega_{FL,PLL} = 400 \text{ rad/sec}, Z_v = 2 \cdot Z_g \text{ and } Z_g = 0.8 \text{ p.u.}\)

### Participation matrix

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## Participation matrix for the AIC-PLL based system, \(\omega_{FL,PLL} = 400 \text{ rad/sec and } Z_g = 2 \text{ p.u.}\)

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### C.3 The Electrical and Control Parameters of the Studied System

This appendix gives the technical data of the studied VSC-HVDC system,
C.3 The Electrical and Control Parameters of the Studied System

C.3.1 The Electrical System Parameters:

Rated Power: 1200 MVA.
Rated voltage $U$: 220 kV.
Angular frequency $\omega$: $2\pi$50 Hz.
Converter inductance $L_c$: 0.08 p.u.
Converter resistance $R_c$: 0.003 p.u.
Filter capacitance $c_f$: 0.074 p.u.
Grid voltage $E$: 1 p.u.
Grid impedance angle: 80°

C.3.2 The control system and PLL parameters

Power controller gains $K_{Pp}, K_{Pi}$: 1, 50.
Voltage controller gains $K_{Up}, K_{Ui}$: 0.1, 5.
Current controller gains $k_{pd} = k_{pq}, k_{id} = k_{iq}$: 1.27, 14.25.
Power measurement filter $\omega_P$: 200 rad/sec.
Ac voltage filter $\omega_U$: 10 rad/sec. The active damping gain $K_{AD}$: 10.
The active damping cut-off frequency $\omega_{AD}$: 200 rad/sec.