Cost Modeling and Analysis of TSV and Contactless 3D-ICs

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ABSTRACT

Contactless three-dimensional (3-D) interconnects have been proposed as an alternative to through-silicon via (TSV) due to its manufacturing compatibility with two-dimensional (2-D) processes. Typically, contactless 3-D circuits are thought to require considerable silicon resources compared to TSV. However, recent manufacturing options, such as extreme wafer thinning, provide new opportunities for this approach. This paper, therefore, explores these opportunities for producing 3-D systems of lower cost. The presented cost analysis and models usefully combine fabrication cost with performance requirements for inter-tier communication as a critical component of 3-D systems. Thus, benchmark circuits are simulated for a two-tier system using a commercial 65 *nm* technology and communicating at a data rate of 1 *Gbps* per link, although the model is directly applicable to any technology or design specifications. Interestingly, inductive links can be a useful alternative to TSV for specific and expected manufacturing capabilities. Furthermore, the effectiveness of different multiplexing schemes and their effect on system cost is also evaluated.

CCS CONCEPTS

• **Hardware → 3D integrated circuits**; **Radio frequency and wireless interconnect**.

KEYWORDS

Three-dimensional integrated circuits; wireless 3-D ICs; cost modeling; TSV; inductive links; extreme wafer thinning

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1 INTRODUCTION

To improve the performance of integrated circuits and overcome the physical scaling barrier, industry explores other ways to improve integration including the third dimension. Multiple dies or wafers are stacked vertically to form a 3-D IC through, for instance, wire bonding, microbump, TSV or wireless inductive/capacitive link [1]. 3-D circuits can offer lower power, heterogeneous integration [1], smaller footprint [2], higher bandwidth [3], and increased security [4]. But cost remains a challenge for the mass production of 3-D IC.

Among these methods, TSV offers substantially high interconnection density, especially when the diameter and pitch of TSV is reduced to 1 μm and 2 μm, respectively, but its complex manufacturing can increase cost considerably [1]. Capacitive or inductive coupling is utilized for contactless communication between tiers. Both contactless approaches require fewer manufacturing steps and reduce the overall wirelength. Inductive coupling is suitable for face-to-face, face-to-back, back-to-back bonding, while capacitive coupling is only fit for face-to-face bonding [**?**]. Consequently, this paper emphasizes TSV and inductive link based 3-D ICs.

For the TSV based 3-D ICs, redundant TSVs can be added to improve yield and reduce the hardware cost [5]. For the inductive link based 3-D ICs, although Die-to-Wafer (D2W) stacking induces larger inductors occupying greater area, significant cost benefits can result for a multiple-die system due to the advantages of the pre-stacking test when facing a processing yield loss [6]. However, no cost comparison to date between the TSV and contactless 3-D communication schemes has been performed. Considering the recently available extreme thinning processes, a cost analysis for these 3-D integration approaches offers useful insight for the choice of the most appropriate 3-D scheme. The analysis and comparison, offered in this paper, explores the different tradeoffs between these two approaches and determines the most cost-effective approach based on specific performance requirements, given as input parameters to the proposed model.

The structure of this paper is as follows. A cost model for 3-D systems is discussed in Section 2. Preliminaries about extreme wafer thinning and a cost analysis for TSV based 3-D ICs is presented in Section 3. Similarly, the cost analysis for inductive link based 3-D ICs is described in Section 4. The proposed cost model for both 3-D IC structures is compared and analyzed in Section 5. Finally, some conclusions are drawn in Section 6.

2 COST MODELING FOR 3-D SYSTEM

3-D IC fabrication cost includes additional manufacturing and stacking cost, such as TSV-last etch, wafer thinning, and die bonding. The overall cost of a 3-D processing consists of four different parts: wafer-level cost, bonding cost, stacking cost and cooling cost, with emphasis on the cost of the first three steps discussed below. This cost model is used to analyze the cost efficiency of different 3-D interconnection. The last step is a strong function of the cooling materials and thermal management methods followed during design time and cannot be reasonably described by a cost model.

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(1) *Wafer cost* : The core factor that affects wafer-level cost is the die yield, which is closely related to both die area and defect density. Die cost is determined by die area, total length of interconnect wires and metal layers.
(2) *Bonding cost* : After the individual 2-D dies have been fabricated, the TSV fabrication follows. Then, TSVs with the bonding pads form the interconnections between dies. The additional fabrication steps and bonding process increase the cost.
(3) *Stacking cost* : In the case of D2W stacking, pre-stack testing of the stacked dices is regarded as a critical step for decreasing the fabrication cost [7]. Compound yield and interposer substrate are the most cost-adding factors for W2W and interposer-based system, respectively [7], [8].

The diameter of the TSVs and inductors affects the silicon area, the number of dies per wafer and, eventually, the cost. The goal is to predict the cost for an inductive link based 3-D system and compare it with a TSV based 3-D system when extreme wafer thinning is performed. Different TSV/coil diameters and TSV yield are considered, therefore, the cost of these options are compared and analyzed.

3 COST OF TSV BASED 3-D ICS

Preliminary information on extreme thinning is introduced in this section. Furthermore, the effect of TSV geometry on manufacturing cost, the silicon area overhead incurred by TSVs for circuits of different area, and the yield as well as the predicted cost for 3-D ICs are presented in this section. Different aspect ratios of TSV are considered for each analysis step.

3.1 Preliminaries

3-D system-on-chip (SoC) enhances interconnection density through Wafer-to-Wafer (W2W) bonding, extreme thinning combined with parallel front-end of line (FEOL) [9], as illustrated in Fig. 1. An example of W2W bonding with a thinned wafer for the upper tier is shown in this figure.

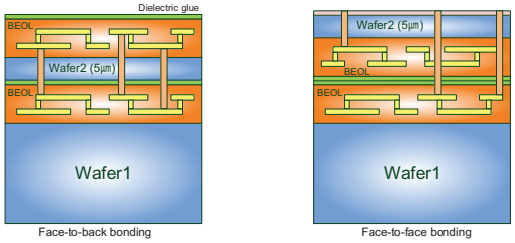


Figure 1: Illustration of face-to-back/face-to-face bonding with extremely thinned wafer.

During the extreme thinning process, the silicon thickness of the top wafer is thinned to 5 μm. Due to the very small diameter and pitch of TSV (diameter < 1 μm, pitch < 2 μm), which are approximately 10 times smaller than those of the typical substrate thickness (50 μm) [9], the scaling of TSVs can be significantly extended.

In this paper, the specific manufacturing approaches and optimization of the extreme thinning process are not considered. Rather emphasis is placed on how the extremely thinned wafer affects the diameter of TSVs and inductors required, respectively, in 3-D interconnection schemes, which further affects the overall chip area and cost.

3.2 TSV Manufacturing and Cost Implications

The TSV-last process can be adapted for extreme thinning [10]. The basic processing for TSV-last includes lithography, TSV etch, oxide liner deposition, bottom liner opening, barrier and seed deposition, Cu plating, and chemical mechanical planarization (CMP) [1]. In the case of TSVs with high aspect ratio (> 10:1) or narrow diameter (sub-micro meter), an additional embedded barrier layer is inserted before the bottom liner opening process to ensure better TSV reliability [11].

As the TSV geometry is considered to be closely related to the process complexity and cost, the cost of a TSV-last process for three different silicon thicknesses with disparate TSV dimensions is illustrated in Fig. 2 : thick silicon (50 μm) [7], moderately thinned silicon (20 μm) and extremely thinned silicon (5 μm), assuming Cu TSV filling for all scenarios. Note that all the processing costs are normalized to the cost of 5 μm × 50 μm TSV-last flow.

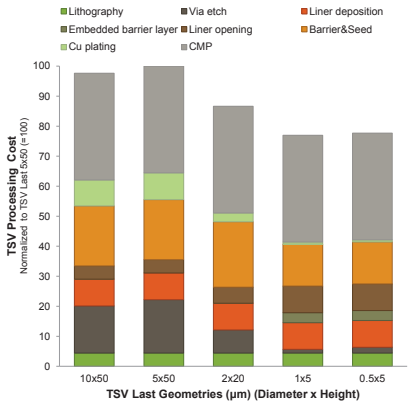


Figure 2: TSV processing cost of different geometries.

As shown in Fig. 2, TSVs, fabricated in thinner Si with a narrower diameter, cost approximately twice as that of thicker diameter due to the liner deposition step and incur an extra barrier step to prevent diffusion of re-sputtered copper to the side-wall of TSVs [11]. Alternatively, shorter TSVs require fewer etch cycles to complete the via etch step. Hence, the required etch time is reduced, which helps reduce the etch cost drastically. In addition, thinner TSV consumes less plating time and material cost for the Cu plating process. Moreover, the 1×5/0.5×5 (μm) TSV-last processing costs are approximately 22% lower than the typical TSV process cost.

3.3 Chip Area Overhead Comparison

The gate-limited 2-D die area A_{die} can be estimated as

$$A_{die} = A_G \times N_G, \tag{1}$$

where A_G is the single gate area and N_G is the total number of gates. Based on industrial empirical data, A_G is estimated to be $3,125n^2$,

where n is the half feature size of the technology node [12]. When these 2-D dies are partitioned and bonded for 3-D integration, an overhead in silicon area is added by the TSVs. To estimate this part of area, *Rent's rule* [13] can be used to determine the number of interconnect (N_{inter}) for the gate number (N_G), as follows [14]

$$N_{inter} = \alpha k N_G (1 - N_G^{p-1}), \tag{2}$$

where α is expressed by $\frac{N_{fan}}{N_{fan}+1}$ and N_{fan} is the average fanout of a gate. k and p are Rent's coefficient parameters which are determined empirically. Assuming the 2-D design is partitioned into two tiers, the TSV number (N_{TSV}) can be predicted by [14]

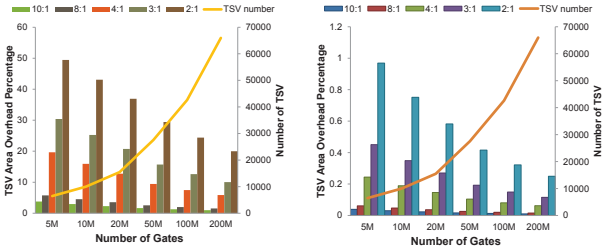
$$\begin{aligned} N_{TSV} = {} & \alpha k_{1,2}(N_{G1} + N_{G2})(1 - (N_{G1} + N_{G2})^{p_{1,2}-1}) \\ & - \alpha k_1 N_{G1}(1 - N_1^{p_1-1}) - \alpha k_2 N_{G2}(1 - N_2^{p_2-1}), \end{aligned} \tag{3}$$

where N_{G1} and N_{G2} are the respective gate numbers allocated in the two tiers. Therefore, the total silicon area including TSVs is

$$A_{total} = A_{die} + N_{TSV} \times A_{TSV}, \tag{4}$$

where A_{TSV} is the area of a single TSV, assumed to be $pitch^2$. $pitch$ is the distance of the center between two adjacent TSVs. The wire routing is assumed to avoid the interconnection area taken by the TSV arrays.

To estimate the overhead in area induced by TSVs, the gates are assumed to be uniformly partitioned within the two tiers. To explore the effect of the aspect ratio on the area, the aspect ratio is swept from 2:1 to 10:1. Using (1) to (4) and the same coefficients as in [15], [16], the TSV overhead in area related to the TSV geometry and the gate number is predicted in Fig. 3 for a 65 nm (=2n) technology.



(a) Typical wafer thickness (50 μm). (b) Extremely thinned wafer (5 μm).

Figure 3: Percentage of TSV area in different 3-D ICs.

The TSV area increases with the decrease of the TSV aspect ratio for both wafer thicknesses, as shown in Fig. 3. For the typical wafer thickness, when the aspect ratio is 2:1, the percentage of TSV area reaches approximate 50% for a small circuit (5M gates) and 20% for a large circuit (200M gates). However, if the aspect ratio increases from 2:1 to 10:1, the TSV area overhead decreases below 5% for both small and large circuits. For the extremely thinned wafer, for any selected aspect ratio, the TSV area overhead is always less than 1%. Especially when the aspect ratio is 10:1, the area overhead due to TSVs is below 0.05%. The effect of the TSV area overhead on the die yield and cost is discussed in the following subsection.

3.4 Approximate Yield and Cost Prediction

The percentage of the chips that are electrically functional on one wafer after all the processing steps is termed as the standard yield (Y_{std}). Major standard yield loss can occur during the photoresist and diffusion steps. Moreover, edge clustering of defects has been observed during the semiconductor manufacturing process. The yield of the interior of the wafer is different from that of edge and the radial yield degradation depends upon the chip area [17]. When incorporating the radial yield (Y_{radial}) with the standard yield, the total chip yield model is

$$Y_{die_{total}} = Y_{std} Y_{radial}. \tag{5}$$

Defects on a wafer are considered to be distributed in clusters based on silicon data [18]. The negative binomial distribution is commonly used to predict the relationship between the total die area (A_{total}) as (4) and Y_{std} [19],

$$\begin{aligned} Y_{std} &= \frac{1}{(1 + D_0 A_{total}/\alpha)^\alpha} \\ &= \frac{1}{(1 + D_0 (A_{die} + N_{TSV} A_{TSV})/\alpha)^\alpha}, \end{aligned} \tag{6}$$

where D_0 is the defect density, α is the clustering parameter that generally depends on the complexity of the manufacturing process.

Assume that the radial yield is a systematic component because it differs in different regions. Assuming the number of chips of a specific region is n_i, the corresponding estimated die yield of this area is Y_i, and R is the radius of the wafer, the radial yield is predicted by [18]

$$Y_{radial} = \sum_{i=1}^{R} n_i Y_i / \sum_{i=1}^{R} n_i. \tag{7}$$

Assuming the average yield for all the dies on the wafer is the same, the stacking yield for a N-layer 3-D stacking process, which uses the W2W stacking method, is

$$Y_{stacking} = \prod_{j=1}^{N-1} Y_{stacking,j} Y_{die_{total}}. \tag{8}$$

When the 3-D circuits are interconnected through TSVs, the TSV yield is incorporated into (8) to determine the stacking yield, replacing $Y_{stacking}$ with $Y_{bonding} Y_{TSV}$ and substituting (6) and (7) into (8) and integrating gives

$$\begin{aligned} Y_{stacking} = {} & \prod_{i=1}^{N-1} Y_{bonding} Y_{TSV} \\ & \times \frac{\sum_{i=1}^{R} n_i Y_i}{(1 + D_0 (A_{die} + N_{TSV} A_{TSV})/\alpha)^\alpha \sum_{i=1}^{R} n_i}. \end{aligned} \tag{9}$$

The total cost C_{total} incurred once these circuits have been packaged is

$$C_{total} = C_w \gamma + \frac{C_s N Y_{die_{total}}}{Y_{stacking}}, \tag{10}$$

where C_w is the wafer-level cost, C_s is the individual die stacking cost, N is the gross number of dice per wafer. γ denotes the complexity of the extreme thinning process, which is roughly proportional to the aspect ratio of TSV and increases inversely proportionally with the pitch of TSV.

4 COST OF INDUCTIVE LINK BASED 3-D ICS

In this section, the cost for inductive link based 3-D ICs is analyzed. The overhead in silicon area is estimated when the coil diameter decreases with the substrate thinning. Then the area and performance is traded off to preserve the electrical performance when the area is reduced.

4.1 Inductor Area and Cost Prediction

Inductor manufacturing is compatible with conventional CMOS processes, therefore, no additional manufacturing steps are added to implement inductors in the metal layers [20]. Typically, spiral inductors occupy considerable silicon area compared to that of the active devices [20]. The area and cost expressions for TSV based 3-D circuits are also suitable for inductive link based 3-D circuits. The total silicon area including coils in (4) is altered to

$$A_{total} = A_{die} + N_{coil} \times A_{coil}, \tag{11}$$

where N_{coil} is the number of spiral pairs required for a specific bandwidth, the overhead in area incurred by a coil A_{coil} is $dout^2$, where $dout$ is the outer diameter of the coil. The active devices are assumed to not occupy the silicon area under and between the coils. Although this assumption is rather excessive, allows for worst case analysis. This assumption is removed later where signal multiplexing is considered and the related circuits are assumed to occupy this area. The stacking yield $Y_{stacking}$ and the total cost C_{total} for N-layer inductive link based 3-D ICs is the same as (8) and (10), respectively.

4.2 Tradeoff Between Performance and Area

To minimize cost, the relationship between the inductive link performance and area should be considered. To investigate the effect of line width (W) and outer diameter (D_{out}) on the link performance, typical substrate thickness (50 μm) and extremely thinned substrate (5 μm) are simulated when W and D_{out} are varied keeping the other parameters fixed. The line spacing and line thickness are constrained by the fabrication process [1]. Furthermore, the dielectric layers and the substrate are defined as per the technology parameters of an eleven-layer metal process to make the inductive link as realistic as possible. The layout parameters of the coils based on 65 nm technology, which is the state-of-the-art technology for this scheme [20], [21], are listed in Table 1.

Table 1: Layout parameters of the inductor.

Metrics	Case 1	Case 2
Substrate thickness (μm)	50	5
ILD thickness (μm)	6.13	6.13
Line spacing (μm)	0.4	0.4
Line thickness (μm)	0.9	0.9
Line Width (μm)	0.4~1.8	0.4~1.8
Turns	5	5
Diameter (μm)	20~80	80~250
Communication distance (X) (μm)	60	12
Resonant frequency (GHz)	1	1

As a minimum coupling efficiency (k) of 0.1 is required for inter-inter communication [20], k is assumed to be 0.2 and the quality factor (Q) is set to 1.3 for the wireless communication scheme. Both structures are simulated using ANSYS Electronic Desktop. The relationship among k, Q, W, and D_{out} is listed in Table 2.

As reported in Table 2, for the 50 μm substrate, the optimal coil structure with W = 1.2 μm and D_{out} = 200 μm, in terms of coil area, can be adopted to reach the required k, which results in Q = 1.32. Alternatively, for the 5 μm substrate, a coil structure combined with W = 1.8 μm and D_{out} = 30 μm maintains the same k, but yields Q = 0.76, which is almost halved. Hence, the inductor area is reduced by 97.8% using the extreme thinning process where k is constant but Q drops by 42%. Assuming the acceptable deviation of Q is 10%, the outer diameter needs to be enlarged to 80 μm to reach the lowest Q requirement. In that case, the area savings drop to 84%, which, nonetheless, is still significant.

Table 2: Tradeoff analysis between inductor area and performance for different D_{out} and X.

X (μm)	D_{out} (μm)	W (μm)	Q	k	area savings (%)
60	200	1.2	1.32	0.2	–
12	30	1.8	0.76	0.2	97.8
12	80	1.8	1.2	0.41	84
24	80	1.8	1.36	0.24	84
36	80	1.8	1.43	0.15	84

Also, as listed in Table 2, when D_{out} remains 80 μm and assuming Q > 1.3, the communication distance can reach as far as 24 μm and exhibits a sufficient k (0.24), which is, effectively, the communication distance between Tier1 and Tier3 for a three tier 3-D circuit. In other words, for a substrate thickness of only 5 μm, a signal can be transmitted from an inductor in Tier1 to Tier3 using one hop for an inductive link based 3-D system. Therefore, cost can be saved for inductive interconnects as two stacked TSVs are needed for a signal to be propagated to Tier3 in a TSV based 3-D system.

5 VALIDATION OF COST MODEL

In this section, several benchmark circuits are used to validate the cost model for TSV based 3-D ICs when diverse TSV aspect ratios and redundancy are considered. Furthermore, the cost between TSV and inductive link is compared for a High-Bandwidth-Memory3 (HBM3) system [22].

5.1 Cost Comparison of TSV Based 3-D ICs

TSVs are prone to defects during manufacturing. Consequently, redundant TSVs (r-TSVs) are inserted into the circuit to repair faulty signal TSVs (f-TSVs) and improve the stacking yield and, therefore, increase the total die yield. To explore the effect of the pitch and aspect ratio on the cost, four benchmark circuits are selected from ITC'99 [23] and the related information is listed in Table 3.

To estimate the cost per benchmark circuit, the wafer-fab cost $C_{w\gamma}$ for a 300 mm extremely thinned wafer is assumed to be \$300 [25] and the stacking cost per die C_s equals \$0.06 [26]. The 3-D circuits are assumed to have a 100% bonding yield ($Y_{bonding}$ = 1). The pitch of TSV is swept from 2d (diameter) to 4d with an increasing TSV yield (Y_{TSV}) from 90% to 99.99%. Assuming f-TSVs and r-TSVs have the same aspect ratio, the total chip cost based on our cost model in Section 3 is depicted as a function of TSV

Table 3: Gate-level benchmarks[24].

Benchmark	Gates	Tiers	f-TSVs	r-TSVs
b17	22,003	2	1,563	2,278
b18	67,319	2	4,286	8,517
b19	117,506	2	5,477	11,517
b22	29,027	2	2,789	3,419

aspect ratio and pitch in Table 4. As TSV yield is proportional to *pitch* [27], a tradeoff between the silicon area and the cost should be considered.

Table 4: Total cost per die as a function of TSV pitch for different TSV AR (extremely thinned wafer).

Y_{TSV}	*pitch*	AR	b17 ($)	b18 ($)	b19 ($)	b22 ($)
90%	2*d*	2:1	0.0677	0.0697	0.0711	0.0682
	2*d*	10:1	0.0673	0.0681	0.069	0.0675
95%	3*d*	2:1	0.0649	0.0681	0.0707	0.0657
	3*d*	10:1	0.0638	0.0647	0.0656	0.0639
99.99%	4*d*	2:1	0.0626	0.0678	0.0707	0.0639
	4*d*	10:1	0.0607	0.0617	0.0627	0.0609

As shown in Table 4, when TSV aspect ratio is 10:1, the cost is decreasing with the increase in *pitch* for the four circuits due to the improvement in TSV yield. TSV yield contributes more to the chip cost rather than the overhead in area due to the TSVs. However, when the TSV aspect ratio is 2:1, for the largest circuit (b19), the effect of additional overhead in area of TSVs becomes significant. When the *pitch* is increased from 3*d* to 4*d*, no cost benefit is obtained but rather more silicon area is wasted.

5.2 Cost Comparison Between TSV and Inductive Link Based 3-D ICs

The cost comparison for interfaces with/without multiplexing for TSV and inductive link based 3-D circuits is discussed as follows.

5.2.1 Interfaces without Multiplexing. A scenario of a HBM3 system with a bandwidth of 512 *Gbps* is considered [22]. To provide a baseline for the transceiver circuits, the data rate for single TSV and inductive link is set to 1 *Gbps* [6]. For either interconnection option, the number of TSVs or coils is 512 per die for two tier stacking, when there is no signal multiplexing or a double date rate scheme. When the TSV yield is swept from 0.3 to 1, the cost comparison between these two interconnection approaches is plotted versus D_{out} and the TSV process yield in Fig. 4, using the cost model for TSV and inductive link 3-D circuits presented in Sections 3 and 4, and the performance parameter setup in subsection 4.2.

As shown in Fig. 4 and the discussion in subsection 4.2, with the decrease in substrate thickness (from 50 μm to 5 μm), the inductive link that supports a specific coupling efficiency (0.2) and exhibits minimum area requires an outer diameter of 30 μm. However, the smallest inductor does not result in the best performance due to the significant drop in Q. Therefore, a careful trade off between the performance and the area occupied by the coil is required. A coil with a diameter of 80 μm (with a total chip cost of $0.911) is a

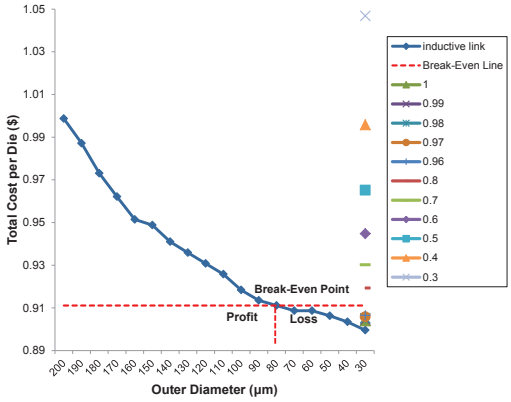


Figure 4: Cost comparison between inductive link and TSV based 3-D ICs vs coil outer diameter and TSV process yield.

superior solution for the aimed 3-D system that achieves the best combination of Q and k. Further area cost reduction below the "break-even line" can be obtained but cost has to be paid for the performance loss.

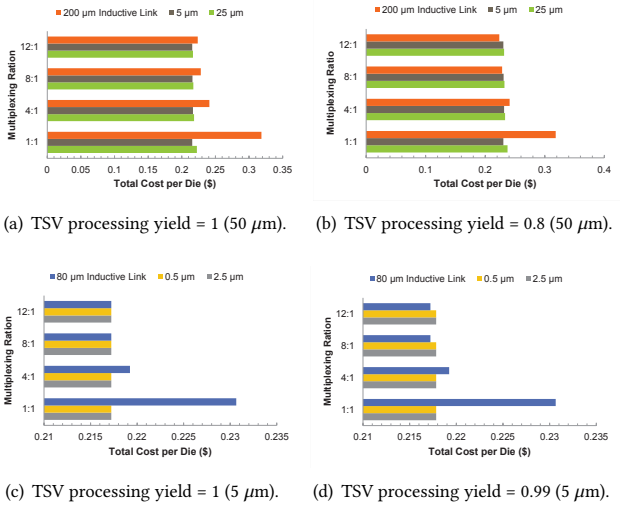
Alternatively, TSV consumes less area than an inductor, but its manufacturing process contains many yield-reducing components compared to the simpler process of an inductor. Thus when the assumed TSV yield drops to 80%, inductors even without multiplexing are more economic than TSVs for 3-D ICs with extremely thinned silicon.

5.2.2 Interfaces with Multiplexing. To further investigate the effect of the multiplexing on the cost of 3-D HBM3 system, a mux-demux circuit is adopted. The 4:1 multiplexer and 1:4 demultiplexer occupies 540 μm^2 and 1160 μm^2, respectively, which can support a multiplexing ratio up to 12:1 [21].

Due to the size of coils, multiplexing and demultiplexing circuits can be implemented under the coils, without adding more silicon area for the inductive links. However, for TSV interfaces, additional silicon area is required for the multiplexer-demultiplexer circuits. Assuming the TSV process yield is swept from 1 to 0.8, a cost comparison between TSV and the inductive link as a function of the multiplexing ratio for both thick (50 μm) and thin (5 μm) substrate is depicted in Fig. 5.

When the TSV processing yield is higher than 99%, for TSV and inductive coupling interfaces without multiplexing, inductive interfaces cost more than TSV interfaces for either substrate thickness, due to the large silicon area occupied by the coils. With multiplexing, the number of coils required for vertical communication is reduced, therefore, the cost drops. Moreover, additional die area for the mux-demux circuits is required in the TSV interface, which increases the cost for the TSV interface. Nonetheless the TSV interface is still of lower cost.

With a decrease in the TSV processing yield, the system cost is significantly affected. Therefore, the inductive link interface exhibits an economical alternative with signal multiplexing, particularly in comparison to TSV interfaces with a low processing yield, a situation that has not been presented to date. Specifically, for the 50 μm substrate, when the TSV processing yield drops to 80%, as



(a) TSV processing yield = 1 (50 μm). (b) TSV processing yield = 0.8 (50 μm).

(c) TSV processing yield = 1 (5 μm). (d) TSV processing yield = 0.99 (5 μm).

Figure 5: Cost comparison for TSV and inductive link 3-D system with different multiplexing ratio and TSV yield.

shown in Fig. 5(b), the total cost per wafer of inductive link interface is approximate 9% lower than that of the TSV interface when the multiplexing ratio increases over 8:1; for the 5 μm substrate, when the TSV processing yield drops to 99%, as shown in Fig. 5(d), the inductive links exhibit an about 0.2% lower wafer cost than TSV interfaces when the multiplexing ratio increases over 8:1.

6 CONCLUSION

In this paper, a cost comparison between TSV and inductive link based 3-D ICs is explored for the first time, considering extreme wafer thinning. A cost model for 3-D systems is used to analyze and compare the cost effectiveness of different 3-D interconnection options. The primary aspects affecting the total cost for 3-D ICs based on these two approaches are grouped into silicon area, radial yield, TSV processing yield, and bonding yield. Several benchmark circuits interconnected by TSVs and a High-Bandwidth-Memory3 (HBM3) system are utilized to demonstrate the usefulness of the cost model. For extremely thinned wafers, the TSV processing yield contributes more to the cost rather than the overhead in TSV area when the diameter is small. Furthermore, both interfaces with/without multiplexing are investigated. For circuits with extremely thinned wafer, if the TSV yield drops from 100% to 99%, inductive interfaces can exhibit a 0.2% lower cost over TSV interfaces for 3-D circuits, when the multiplexing ratio increases over 8:1. This cost improvement increases considerably with yield loss, demonstrating that contactless inductive interfaces offer a useful alternative to TSV-based 3-D integration.

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REFERENCES

[1] V. F. Pavlidis, I. Savidis, and E. G. Friedman, *Three-Dimensional integrated circuit design*, 2nd Edition, Morgan Kaufmann Publishers, 2017.
[2] W. R. Davis *et al.*, "Demystifying 3D ICs: The pros and cons of going vertical," *IEEE Design & Test of Computers*, Vol. 22, No. 6, pp. 498–510, November 2005.
[3] J. Zhao, Q. Zou, and Y. Xie, "Overview of 3-D architecture design opportunities and techniques," *IEEE Design & Test of Computers*, Vol. 34, No. 4, pp. 60–68, July 2015.
[4] P. Gu *et al.*, "Leveraging 3D technologies for hardware security: Opportunities and challenges," *Proceedings of the International Great Lakes Symposium on VLSI*, pp. 347–352, May 2016.
[5] L. Jiang, Q. Xu, and B. Eklow, "On effective TSV repair for 3D-stacked ICs," *Proceedings of the Design, Automation & Test in Europe Conference & Exhibition*, pp. 793–798, March 2012.
[6] I. A. Papistas, V. F. Pavlidis, and D. Velenis, "Fabrication cost analysis for contactless 3-D ICs," *IEEE Transactions on Circuits and Systems II: Express Briefs*, Vol. 66, No. 5, pp. 758–762, April 2019.
[7] D. Velenis *et al.*, "Cost components for 3D system integration," *Proceedings of the Electronics System-integration Technology Conference*, pp. 1–5, September 2014.
[8] Y. W. Chou *et al.*, "Cost modeling and analysis for interposer-based three-dimensional IC," *Proceedings of the IEEE VLSI Test Symposium*, pp. 108–113, April 2012.
[9] M. Liebens *et al.*, "In-line metrology for characterization and control of extreme wafer thinning of bonded wafers," *IEEE Transactions on Semiconductor Manufacturing*, Vol. 32, No. 1, pp. 54–61, December 2018.
[10] F. Inoue *et al.*, "Characterization of extreme Si thinning process for wafer-to-wafer stacking," *Proceedings of the IEEE Electronic Components and Technology Conference*, pp.2095–2102, May 2016.
[11] S. Van Huylenbroeck *et al.*, "A highly reliable 1.4 μm pitch via-last TSV module for wafer-to-wafer hybrid bonded 3D-SOC systems," *Proceedings of the IEEE Electronic Components and Technology Conference*, pp.1035–1040, May 2019.
[12] Y. Xie, J. Cong, and S. Sapatnekar, *Three-dimensional integrated circuit design*, New York: Springer, 2010.
[13] D. H. Kim *et al.*, "Through-silicon-via aware interconnect prediction and optimization for 3D stacked ICs," *Proceedings of the International Workshop on System Level Interconnect Prediction*, pp.85–92, July 2009.
[14] X. Dong, J. Zhao, and Y. Xie, " Fabrication cost analysis and cost-aware design space exploration for 3-D ICs," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 29, No. 12, pp. 1959–1972, December 2010.
[15] A. B. Kahng, S. Mantik, and D. Stroobandt, "Toward accurate models of achievable routing," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 20, No. 5, pp. 648–659, May 2001.
[16] H. B. Bakoglu, *Circuits, interconnections, and packaging for VLSI*. Reading, MA: Addison-Wesley, 1990.
[17] E. Singh, "Impact of radial defect clustering on 3D stacked IC yield from wafer to wafer stacking," *Proceedings of the IEEE International Test Conference*, pp.1–7, November 2012.
[18] A. Gupta *et al.*, "Defect analysis and yield degradation of integrated circuits," *IEEE Journal of Solid-state Circuits*, Vol. 9, No. 3, pp. 96—103, June 1974.
[19] I. Koren *et al.*, "A unified negative-binomial distribution for yield analysis of defect-tolerant circuits," *IEEE Transactions on Computers*, Vol. 42, No. 6, pp. 724—734, June 1993.
[20] I. A. Papistas and V. F. Pavlidis, "Contactless heterogeneous 3-D ICs for smart sensing systems," *Integration*, Vol. 62, pp. 329–340, June 2018.
[21] I. A. Papistas and V. F. Pavlidis, "Bandwidth-to-area comparison of through silicon vias and inductive links for 3-D ICs," *Proceedings of the European Conference on Circuit Theory and Design*, pp.1–4, August 2015.
[22] AMD high bandwidth memory website, http://www.amd.com/en-us/innovations/software-technologies/hbm.
[23] F. Corno, M. S. Reorda, and G. Squillero, "RT-level ITC'99 benchmarks and first ATPG results," *IEEE Design & Test of computers*, Vol. 17, No. 3, pp. 44—53, July/September 2000.
[24] S. Wang, K. Chakrabarty, and M. B. Tahoori, "Defect clustering-aware spare-TSV allocation in 3D ICs for yield enhancement," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 38, No. 10, pp.1928–1941, August 2018.
[25] J. H. Lau, "TSV manufacturing yield and hidden costs for 3D IC integration," *Proceedings of the Electronic Components and Technology Conference*, pp.1031–1042, June 2010.
[26] P. R. Gray *et al.*, *Analysis and design of analog integrated circuits*, 4th Edition, Wiley, 2001.
[27] M. Stucchi *et al.*, "Test structures for characterization of through-silicon vias," *IEEE Transactions on Semiconductor Manufacturing*, Vol. 25, No. 3, pp. 355—364, June 2012.