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Low-Cost InP-InGaAs PIN-HBT Based OEIC for up to 20Gb/s Optical Communication Systems

Saad. G. Muttalak¹, Ioannis Kostakis², Omar S. Abdulwahid¹, J. Sexton¹, and M. Missous¹

¹School of Electrical and Electronic Engineering, the University of Manchester, United Kingdom

²Integrated Compound Semiconductors, Manchester, United Kingdom

saad.muttalak@manchester.ac.uk

Abstract: A detailed study of the performance analysis of a low cost PIN/HBT optoelectronic integrated circuit is described. Measured f_T and f_{max} of 54 and 57GHz for $10 \times 10 \mu m^2$ HBTs were achieved for such a large emitter size. The base and collector regions of the transistor were utilized to form a PIN photodiode which has a dc responsivity and quantum efficiency of 0.5 A/W and 0.45 respectively without antireflection coating at a wavelength of $1.55 \mu m$. For both active devices, a model was realized taking all parasitic and physical-based impacts into account, for example equivalent circuit of the pads surrounding the devices and transit delay time across the collector depletion region. The simulation results of the discrete passive and active elements showed good agreement with experimental measurements. The OEIC module was implemented in Keysight-advanced design system software with a three stage preamplifier which has a transimpedance gain of $40 dB \Omega$ and a -3dB bandwidth of 18GHz. This corresponds to a transimpedance-gain product of 1.8THz. A series peaking inductor technique was used in the design, contributing to an enhancement in the opto-electrical bandwidth of >60%. The optical/electrical response offers a bandwidth of ~ 15 GHz, adequate for up to 20 Gb/s data rate operation.

1. Introduction

The dramatic increase in data traffic due to rapidly growing demands for ultra-high data rates for both telecom and datacom is driving sustained developments in cost effective, mass produced, optoelectronic integrated photoreceiver (OEIC) operating at 10Gb/s and beyond [1-3]. As an optical architecture standard, 2.5Gb/s GPON is in full deployment and the next generation 10Gb/s EPON (IEEE 802.2av, ratified September 2009) started deployment in late 2013 [4, 5]. OEICs are undisputedly the key-components in fibre optic communication systems including the front-end transimpedance amplifiers (TIAs) and PIN/avalanche photodiodes. Since their optical/electrical bandwidth and conversion gain dominate the entire characteristics of the receivers [6], improving these crucial parameters are paramount in high data rate capability of the optical systems. For photoreceiver circuits' implementations, HEMTs and HBTs transistors have been extensively

investigated by integrating PIN/avalanche photodiodes with TIAs [2, 6, 23, 24].

The requirement for extremely small HEMT gate length (typically $< 0.1 \mu m$) to achieve over 100GHz cut-off frequencies [12] in comparison with fairly relaxed emitter size of HBTs makes the heterojunction transistors attractive for low cost, volume manufacturing as they require much less stringent lithography. The exponentially increasing performance of recent HBTs, HEMTs and CMOS ICs used in optical communications links is depicted in Fig. 1. There are mainly two approaches in integrations of OEICs; monolithic and hybrid forms. The first scheme offers the ability to exploit the base-collector heterojunction layers for the formation of the photodiodes, contributing to a simple epitaxial growth process and so circumventing both regrowth and complex fabrication sequence along with packaging simplification [25, 26]. The downside of a shared layer between two different devices is that a trade-off between the collector depletion region of HBTs and carriers' transit time of photodiodes needs to be effectively balanced. The benefit from the hybrid integration scheme is to independently optimize the epitaxial layers of the photodiodes and HBTs thereby accomplishing an optimum performance for each device individually [27]. However, this approach has disadvantages including increase in epitaxial growth complexity, large IC sizes and inevitable extra parasitic elements due to bond wire connections [23, 28].

For these reasons, monolithically integrated circuits are preferred over hybrid ones for ultrahigh speed photoreceivers. Among three terminals heterojunction devices, InP/InGaAs based OEICs have been widely studied for beyond 10Gb/s data rates for operation at $1.55 \mu m$ [26, 29]. It is well-known that further increase in data rates capabilities requires minimizing the emitter mesa sizes of HBTs. Likewise; photodiodes with small window sizes/side-illuminated become indispensable for the sake of smaller

Fig. 1. Comparison of the reported optical receiver performances in terms of their bandwidth and data rates [3, 5-22].

depletion capacitance/shorter delay time across the absorption layer. The use of such technologies is at the expense of increase in manufacturing cost and difficulty of fibre optic alignments. Therefore, a surface illuminated, low cost HBT-PIN based OEICs receiver is undeniably important for high performance 10Gb/s EPON optical transmission system.

This work is concerned with the design, characterization and modelling of high speed InP/InGaAs PIN-SHBT based OEIC photoreceivers. More importantly, full-scale characterizations of the receivers using CAD tools prior to the fabricated circuits are invaluable in the prediction of prospective performances and to aid in further optimisations. The TIA circuit was designed using $10 \times 10 \mu\text{m}^2$ HBT emitter size. The photoreceiver response showed an optical bandwidth of 15GHz at a wavelength of $1.55 \mu\text{m}$, which is adequate for up to 20Gb/s optical operation. The realized module was built in advanced design system software from Keysight technologies. The passive and active components of the receiver were individually fabricated and the extraction of their equivalent circuits was carefully carried out in terms of taking all the associated parasitic elements into account. In-depth discussion and analysis related to the module are also presented here, for example TIA gain-frequency characteristics and optical response of OEIC circuit to a non-return-to zero (NRZ) 2^{15} -1 pseudo-random bit stream (PRBS) patterns.

Table I: Epi-layers for HBT sample F17D2102A grown by MBE

Layer	Material	Thickness (nm)	Doping (cm ⁻³)
cap-layer	In _{0.53} Ga _{0.47} As	150	(Si) 1.5×10^{19}
emitter ₁	In _{0.53} Ga _{0.47} As	150	(Si) 5×10^{17}
emitter ₂	InP	40	(Si) 5×10^{17}
spacer	In _{0.53} Ga _{0.4} As	5	Undoped
base	In _{0.53} Ga _{0.47} As	65	(Be) 2.5×10^{19}
collector	In _{0.53} Ga _{0.4} As	800	Undoped
sub-collector	In _{0.53} Ga _{0.4} As	500	(Si) 1×10^{19}

2. Epitaxial Structure and Fabrication process

The epitaxial layers were grown on lattice-matched semi-insulating InP substrates using Molecular Beam Epitaxy (MBE) as shown in Table I. The structure utilised a small band-gap heavily doped InGaAs top cap layer to alleviate the series resistance of the emitter contact. A 5nm spacer layer was employed to reduce the potential spike and dopant out-diffusion at the emitter-base interface, resulting in lower offset voltage in the I-V characteristics of the devices. Furthermore, the use of an undoped collector layer not only helps to increase the breakdown voltage and minimize the base-collector capacitance, but also serves as the absorption layer for the photodiode. Due to the trade-off between high-frequency performance of HBTs and responsivity of PIN-PDs, the intrinsic layer was designed to be 800nm. The process commenced with fabricating and testing both the HBTs and PINs to be integrated in the front-end receiver. The individual devices were fabricated using standard i-line photolithography and wet etching process to

first create the emitter mesa with a size of $10 \times 10 \mu\text{m}^2$. This was followed by etching away the surrounding area to the p⁺-InGaAs base layer. Since the subsequent layers are shared between the two devices, the process of the photodiodes is entirely compatible with the HBTs. Fig. 2 shows a simplified schematic of the fabricated PIN with a window size of $20 \mu\text{m}$ and HBT transistor. In the same manner, base and collector mesas were defined, allowing both devices to be completely isolated from other neighbouring devices.

Fig. 2. Schematic cross section of the fabricated devices showing PIN-PD and HBT on left and right sides respectively both sitting on a semi-insulating InP substrate. Note: the drawing is not to scale.

Next, a combination of SiO and Al₂O₃ was sputtered for passivation and interconnect routing. This dielectric layer also acts as an antireflection coating (AR) for the photodiodes, providing better responsivity performance. The final step was the interconnect metal, including ground plane, input/output RF pads, DC biasing and to form the spiral inductor, which is characterized in section 3 and also incorporated in the receiver circuit. The metallization of PINs and HBTs contacts used the non-alloyed ohmic contact scheme of Pd/Ti/Pd/Au with a total thickness of $\sim 1 \mu\text{m}$. To reduce the extrinsic series resistance of the base while maintaining high yield process, the spreading distance between the base contact and the device structure was optimized to be $1.5 \mu\text{m}$.

3. Passive and Active Elements Characterizations

The passive and active components are required for the photoreceivers' implementation. Once these elements were successfully fabricated, S-parameter measurements were performed up to 40GHz using an Anritsu 37369A vector network analyser. All the components were on-wafer contacted by a 50Ω characteristic impedance ground-signal-ground (GSG) probe. A module was realized in Keysight ADS for the discrete devices and eventually for the whole OEIC receiver.

3.1 Passive Elements

Due to the fact that the performance and reliability of the passive elements is strongly dependent on the predefined dimensions and fabrication process instead of design equations, an equivalent circuit model, in which their non-ideal nature is taken into account, is necessary. This can be reflected into avoiding substantial errors in the model, making the simulation more accurate and closer to the actual measured results. Therefore, the equivalent circuits were verified and experimentally validated using fitting approaches

with the S-parameters data to extract of RF parameters. The equivalent circuit module of the resistors and spiral inductor realized here is similar to the one reported in [30-32]. Because of their rather low temperature coefficient of resistance compared with semiconductor active layer resistors, thin film resistive metals are preferred for use in MMIC applications [33]. In this work, a NiCr resistor with various values ranging from 25 to 1k Ω was deposited on 200nm Si₃N₄ dielectric layer. A 50 $\Omega/\square$ sheet resistance was attained with a NiCr thickness of 120nm. Fig. 3 shows excellent fit between modelled and experimental results of a 100 Ω resistor. Comparable resistor values were also found from the slope of the measured I-V characteristics. An additional parasitic capacitance of 23fF was obtained from the S-parameter measurements.

A spiral peaking inductor with 3 μ m track width was fabricated and tested. The model and measured results for a 0.7nH inductor are well-matched as depicted in Fig. 4. As can be observed, S_{11} exhibits an inductive behaviour and the S_{21} response does not intersect with the centre line of the chart, from which the self-resonant frequency (SRF) is clearly higher than 40GHz. It is noteworthy to point out that such inherent phenomenon occurs due to the existence of an associated capacitive effect which in turn cancels the inductive reactance at a certain frequency. For larger inductors, measured results of a 2nH inductor led to a SRF of 21GHz. A 9 Ω track length series resistance and 47fF parasitic capacitance were extracted from the measured data. Further increase in metal thickness can decrease the series resistance of the spiral inductor. A spiral inductor with an optimum inner diameter in which the majority of the magnetic flux variation passes through a sufficiently large space would offer much less eddy current losses for higher quality factor and low noise circuit operation [32]. All the additional parasitic elements were incorporated in the model of the photoreceiver.

3.2 InP/InGaAs-HBT

Whilst maximizing f_T is predominantly controlled by optimizing the vertical device structures, f_{max} is critically dependent on both lateral HBTs process and base-collector layer design. For high f_{max} transistor, the key-driver in fabrication process is to minimise the base resistance (R_B) and base-emitter capacitance (C_{be}). Several interesting endeavours were proposed to boost f_{max} , for instance hexagonal emitter formation for less under-cut profile [34] and emitter overhang technique to separate the base-emitter contacts [6]. However, these approaches are methods to improve the poor yield of the self-aligned process for small feature HBT sizes. In this work, we used a standard non-self-aligned technique for large emitter devices. This does simplify the process in terms of depositing the contacts and interconnecting metals in a single step, offering a low cost and less time-consuming process. Due to the specific design of the InP-InGaAs epilayer structures, and considering the trade-off between high performance PIN and the heterostructure transistor, a 10 $\times$ 10 μ m² emitter mesa size HBT demonstrate an f_T and f_{max} of 54 and 57GHz respectively. These parameters are amply adequate for low

cost integrated 10Gb/s and beyond optical receivers.

Fig. 3. Real and imaginary parts of the simulated and measured results for a 100 Ω NiCr resistor (red and blue lines are for experimental and model results respectively).

Fig. 4. Measured (red) and simulated (blue) S-parameters response of 0.7nH spiral inductor in the frequency range of 0.03-40 GHz.

Further minimizing the HBT mesa area to 4 $\times$ 4 μ m² can effectively lead to over 100 GHz cut-off frequencies. Table II shows a performance comparison between the designed and measured parameters of the presented HBT and previously reported devices. The inferred unity gain cutoff frequency and the maximum frequency of oscillation of the fabricated 10 $\times$ 10 μ m² HBT device are higher than that demonstrated in [35] and comparable with the published work [26, 28]. This is due to a well-designed structure and high quality material used. Moderate values of C_{be} and C_{bc} were obtained (50 and 27fF respectively). A transistor model was built using the Keysight-HBT model, after performing a two steps de-embedding procedure with corresponding dummy structures. The large signal University of California, San Diego (UCSD) HBT model presented here takes the potential spike at the heterojunction into account and includes various other effects, such as self-heating and impact ionization effects [36]. The HBT used has a dc current gain, β of about 65 at a bias condition V_{CE} =2V and I_C =10mA and a breakdown voltage of 4.5V. The unified UCSD model for the fabricated InP/InGaAs transistor was verified for both dc and microwave characteristics with various voltage bias. The common

emitter characteristic and figure of merits f_T and f_{max} for the modeled and measured results are depicted in Fig. 5. There is a good agreement between the measured and modeled results. To avoid connecting the base and emitter electrodes, the spreading distance between the base contact and the device structure was optimized to be $1.5\mu\text{m}$. This is to achieve a high yield with not significantly degradation in unilateral power gain of the HBTs.

TABLE II: Performance comparison of this work's HBT and recently published works

Ref.	Technology	Emitter Size (μm^2)	Process	f_T/f_{max} (GHz)
[6]	InP/InGaAs	1×5	emitter-overhang self-aligned	130/220
[26]	InP/InGaAs	4×12	self-aligned	80/40
[37]	InP/InGaAs	1.6×10	T-shape emitter self-aligned	150/220
[17]	InP/InGaAs	0.8×4	self-aligned	260/320
[15]	InP/InGaAs	0.25×1	self-aligned	$\sim 400/40$
[38]	InP/InGaAs	0.5×5	transferred-substrate	280/300
This work	InP/InGaAs	10×10	standard process	54/57

3.3 PIN-Photodiode

The PIN-PDs were fabricated with the former utilizing the base and collector regions of the HBT. The measured dark current of 1.5nA was achieved for a discrete device with a $20\mu\text{m}$ optical window size. The low leakage current is attributed to the high quality of the epitaxial structure. Furthermore, the measured dc responsivity and quantum efficiency of the PIN without AR coatings were 0.5 A/W and 0.45 at $\lambda=1.55\mu\text{m}$ respectively. A single mode fibre was used for measurement with a Keysight 8703A lightwave component analyser. These parameters can improve by roughly 20% with AR coating. The well-known electrical equivalent circuit model of two terminal devices have been widely demonstrated for solid state electronic and optoelectronic devices [39, 40]. This model was first realized for unilluminated PINs, emphasizing that the fully-depleted capacitance (C_j) of 180fF was obtained at an external voltage bias (V_{fd}) of -5V . Since this voltage is strongly dominated by the depletion region thickness, a similar V_{fd} value was observed for various devices regardless of their mesa sizes. The intrinsic series resistance (R_s) and junction resistance (R_j) of the device were also extracted to be 5Ω and $>10\text{k}\Omega$ respectively. Pad parasitic (C_p) and (L_p) of 10fF and 50pH were obtained from open and short coplanar waveguide structures respectively. Fully electrical models reported in the literature do not actually provide a proper physic-based transit time capacitance for illuminated PIN-PDs [41]. This becomes much inferior with high input optical power level in which the impact of the induced-stored charge in the photodiodes is significant [42]. In this work, an opto-electrical equivalent circuit was

modeled in which both RC time constant and carrier transit time are taken into account as shown in Fig. 6.

Fig. 5. Measured and simulated characteristics of the common emitter InP/InGaAs HBT with a $10\times 10\mu\text{m}^2$ mesa size, (a) output I - V characteristic with various I_B values. (b) f_T and f_{max} at $V_{CE}=2\text{V}$ and $I_C=10\text{mA}$. Inset: photomicrograph of the fabricated HBT discrete device.

The transit delay time ($R_t C_t$) caused by transport of electron-hole pairs generates carriers with their saturation velocity in the depletion region due to drifting in a high electric field. This leads to deterioration in the speed of carriers, depending on the width of the depletion region and the electric field applied. Owing to RC time constant and delay time effects, the 3-dB electrical bandwidth can be formulated as [43]:

$$f_{3dB} = \frac{1}{\sqrt{f_t^{-2} + f_{RC}^{-2}}} \quad (1)$$

f_{RC} is given by $1/2\pi(R_L + R_s)C_j$, from the extracted equivalent circuit values, the RC limited 3-dB bandwidth was 17.7GHz . The transit time model, $R_t C_t$ was combined with a nonlinear voltage controlled current source (VCCS), whose main function is to convert the input optical signal into an ac photocurrent, $i_{ph}(\omega)$ expressed as $g_m e_o(\omega)$, where g_m is the dc transconductance [42].

Fig. 6. Small signal opto-electrical equivalent circuit of the PIN-photodiodes including both carrier transit time and RC models.

The generated photocurrent flows through the circuit elements. To theoretically estimate the term $g_m e_o(\omega)$, it was evident from the measured optical response with different PIN mesa sizes that $i_{ph(\omega)}$ can be formulated as $g_m e_o(\omega) \approx P_{ph} R_{es}(\omega)$. P_{ph} and $R_{es}(\omega)$ being the incident power of light in Watt and the frequency-dependent responsivity of the photodiode.

Fig. 7. Simulated and measured small signal response of the PIN-PD with a window size of $20\mu\text{m}$ and at a several incident optical power. Inset: photomicrograph of the fabricated PIN-PD device.

At $\omega/2\pi \ll f_{3dB}$, $g_m e_o(\omega)$ is approximately equal to the dc photocurrent of the device for a given optical power. The use of an approximated symbol with $i_{ph(\omega)}$ is due largely to the reflected/absorbed P_{ph} at the surface/in the p+-base region of the devices. By defining the optical power with the voltage generator $e_i(\omega)$ whose impedance R_{in} is 50Ω , the optical response of the circuit was derived and expressed as:

$$20\log \left| \frac{e_o(\omega)}{e_i(\omega)} \right| = 20\log \left(\sqrt{\frac{1 + \omega^2 C_t^2 R_t^2}{[1 + \omega^2 C_t^2 (R_t^2 + R_{in}^2)]}} \right) \quad (2)$$

For the sake of simplicity, $g_m e_o(\omega)$ is considered as a source for the following RC model circuit, the relative frequency response can be calculated as:

$$20\log \left| \frac{e_L(\omega)}{e_o(\omega)} \right| = 20\log \left(g_m \sqrt{\frac{1}{\omega^2 (C_P^2 + C_j^2) + \omega^4 C_P^2 C_j^2 (R_s^2 + L_P^2 \omega^5)}} \right) \quad (3)$$

The evaluation of the term $R_t C_t$ has been assessed in three steps. The actual absorption layer thickness (D) of $\sim 850\text{nm}$ was first calculated from the device respective capacitance C_j at -5V . This gives an electric field of $\sim 58\text{kV/cm}$, producing an average electron-hole drift velocity (v_s) of $\sim 0.55 \times 10^7 \text{ cm/s}$, which is reasonable for an undoped InGaAs layer and comparable with previous published papers [44]. The 3-dB carrier transit time bandwidth is represented by the physical parameter of the PIN-PD structure [43].

$$f_t \approx \frac{3.5v_s}{2\pi D} \approx \frac{1}{2\pi R_t C_t} \quad (4)$$

A calculated f_t of 36GHz gives R_t and C_t of 50Ω and 88fF respectively. This resulting f_t demonstrates that the photodiode is evidently limited by its RC time constant. All the values of circuit parameters were used in the model, so a well-matched simulated and measured data were achieved as shown in Fig. 7. A measured 3-dB bandwidth of 18GHz was obtained, considering the relatively large mesa size. This is theoretically adequate for up to 25Gb/s operation and appealing for low cost monolithically integrated photoreceiver circuit modules. The optical bandwidth is expected to be further increased with reduction in the photodiode mesa size and optimum absorption layer thickness.

4. Circuit Design and Performance

Fig. 8 shows the circuit design of the OEIC used in this work, including the front-end amplifier, series peaking inductor (L_{sp}) and integrated PIN-PD. The transimpedance amplifier configuration is composed of a three stage transistors with a feedback resistor, R_F . The common-emitter transistor, Q_1 is utilized as a gain stage, while Q_2 and Q_3 are implemented as two emitter-follower buffer stages. The use of these HBT buffers is to ensure that a 50Ω output impedance (Z_{out}) is achieved at the output port, which is matched with the standard measurement set-up ($Z_o = 50\Omega$). Furthermore, R_F provides a shunt-shunt feedback to the base of Q_3 and its values should be carefully chosen because of the trade-off between the overall gain and bandwidth of the photoreceiver. These key parameters are also affected by the biasing and mesa size of Q_1 . The challenge in designing a wide bandwidth OEICs is the presence of a relatively large capacitance of the PIN diodes, loaded on the TIA's circuit. Common-base input stage was proposed to address this

issue [45]; however, in such configuration, additional transistors are required to boost the circuit's gain. For less complexity design, the shunt feedback topology at the base node of Q_1 was exploited to lower the input impedance of the amplifier. The direct consequence is to push the dominant pole caused by PIN-PD into high frequencies for an efficient high speed operation.

Fig.8. A schematic circuit of the modeled photoreceiver showing only prime elements.

For a 3-dB bandwidth enhancement, a series spiral inductor was used to supplementary mitigate the capacitive behaviour effect on the optical response. A small L_{sp} can be mainly obtained by decreasing the intrinsic capacitance of the photodiode and input impedance of the TIA (Z_{in}). L_{sp} can be approximately given by $C_j(R_s + Z_{in})^2/2$ [46]. Since the inductance of L_{sp} is a frequency-dependent parameter, a peak resonance is introduced at a certain frequency where the capacitive and inductive effects cancel each other. The effective transimpedance gain of the TIA without photodiode is calculated from the S-parameter data [47].

$$Z_{eff} = |Z_o| \frac{|S_{21}|}{|1 - S_{11}|} \quad (5)$$

It is important to point out that the passive elements were optimized for high speed operation and all parameters used in the simulation are listed in Table III. The front-end amplifier was simulated with and without peaking inductor as shown in Fig. 9. The amplifier showed a transimpedance gain of 40dBΩ with an electrical bandwidth of 11GHz without L_{sp} . A 2nH integrated peaking inductor led to widening in the -3dB bandwidth to 18GHz, which is enhanced by >60%.

Table III Model parameters of the TIA used in this work

Parameter	V_{CC} (V)	V_{PD} (V)	I_{ph} (μA)	L_{sp} (nH)	R_{C1} (Ω)	R_F (Ω)	R_{E2} (Ω)	R_{E3} (Ω)
Value	3.3	5	41	2	100	200	450	500

Based on this, the corresponding transimpedance gain product is 1.8THz. However, the relatively large feedback resistor of 200Ω used in the model decreases the bandwidth of the circuit without the use of a peaking technique. To characterize the circuit performance, the conversion gain was calculated, which is the product of transimpedance gain and responsivity of the photodiode.

Fig.9. Simulation result of transimpedance gain response as a function of operating frequency using $10 \times 10 \mu m^2$ InP/InGaAs HBTs with and without peaking inductor.

Fig.10. Opto-electrical frequency response of the modeled photoreceiver with and without peaking inductor. The OEIC was realized with an integrated $20 \mu m$ window size PIN-PD and $10 \times 10 \mu m^2$ InP/InGaAs HBTs.

Fig.11. Simulated eye diagram of the photoreceiver with NRZ 215-1 pattern length PRBS and at a bit rate of 10Gb/s (top) and 20Gb/s (bottom).

A 50V/W conversion gain was obtained and it is expected to improve by ~20% with the addition of AR coating layer deposited on the PIN's window optical aperture. The model of the whole photoreceiver demonstrates that the circuit has an opto-electrical bandwidth of 15 and 9GHz with and without integrated inductor respectively as shown in Fig. 10. The inductor peaking design is theoretically sufficient for up to 20 Gb/s data rate operation. A channel simulator tool embedded in Keysight-ADS was used to model the receiver with a transmitted data stream. Due to a limitation in pattern generator capability of the simulator, a NRZ $2^{15}-1$ PRBS patterns were applied. Clearly open eye diagram with no inter-symbol interference (ISI) was observed for 10 and 20 Gb/s operation as depicted Fig. 11. The results show negligibly small overshoot or/and undershoot. The calculated root mean square jitter was 4ps at 20Gb/s.

5. Conclusion

The work reported here was concerned with both characterization and modeling of a TIA integrated with a PIN diode for optical receivers using an InP/InGaAs HBT. Both the photodiode and HBT were successfully fabricated, with the former utilizing the base and collector regions of the HBT. The measured dc responsivity and quantum efficiency of the PIN without AR coatings were 0.5 A/W and 0.45 respectively. The equivalent circuit of the diode was experimentally validated up to 40GHz using S-parameter measurements taking both depletion region capacitance and collector transit time effect into account. A $10 \times 10 \mu\text{m}^2$ emitter mesa size HBT achieved an f_T and f_{max} of 54 and 57GHz. The preamplifier was modeled using Keysight-ADS software and a transimpedance gain of 40dB Ω was obtained. A series peaking inductor technique was utilized and enhances the opto-electrical bandwidth by greater than 60%. The optimized circuit had an optical bandwidth of 15GHz, which is theoretically sufficient for up to 20Gb/s operation.

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